Research Article

Synchronous Current Compensator for a Self-Balanced Three-Level Neutral Point Clamped Inverter

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This paper presents a synchronous current control method for a three-level neutral point clamped inverter. Synchronous reference frame control based on two decoupled proportional-integral (PI) controllers is used to control the current in direct and quadrature axes. A phase disposition pulse width modulation (PDPWM) method in regular symmetrical sampling is used for generating the inverter switching signals. To eliminate the harmonic content with no phase errors, two first-order low pass filters (LPFs) are used for the dq currents. The simulation of closed-loop control is done in Matlab/Simulink. The Vertex-5 field programmable gate array (FPGA) in Labview/CompactRio is used for the implementation of the control algorithm. The control and switch pulse generation are done in independent parallel loops. The synchronization of both loops is achieved by controlling the length of waiting time for each loop. The simulation results are validated with experiments. The results show that the control action is reliable and efficient for the load current control.

1. Introduction

The efficient conversion of renewable energy to electrical energy is still a key area of research. All renewable energy projects require power electronics converters for interfacing with the grid and controlling the energy exchange. Most of the basic conversion strategy of renewable energy follows a two-step procedure. First step is to convert the variable AC to constant DC. Active rectifiers or passive rectifiers with DC/DC converters are the generally used methods to date. However, the main part of the conversion unit is an inverter. It is used not only for connecting to different loads, but also for providing the necessary control actions required for the load. To meet the high energy demand, conversion and integration of renewable energy sources are suggested universally. The majority of the renewable energy plants are geographically far from the load centers. The integration of this power needs a very long transmission cable to reach the point of common connection. High voltage power transmission meets better efficiency by reducing cable losses. Thereby, the

use of multilevel converters is also gone up [1]. Different conventional topologies of multilevel inverter structures are proposed in [2]. Neutral point clamped (NPC) inverter is a widely accepted topology amongst these [3–6].

In most of the applications, the performance of the voltage source inverter (VSI) depends on the quality of the applied current control strategy. It enhances the control accuracy of the instantaneous current waveform by providing the peak current protection and overload rejection and by compensating the load variation. The inverter control forces the load current to follow the reference signals. The inverter switching states are generated by comparing the reference and measured instantaneous values of phase currents. Different current control strategies are explained in [7, 8]. The linear current controllers are more attractive compared to other methods for application in low switching frequency.

The most widely used current control method uses proportional-integral (PI) controllers [9–12]. A robust synchronous reference frame (SRF) control algorithm to regulate the grid current from a three-phase two-level VSI with

FIGURE 1: (a) Three-level NPC inverter connected to R-L load and (b) three-level PDPWM signal.

an LCL input filter is presented in [13]. An NPC inverter model that allows the implementation of a simple linear feedback-control technique to keep zero-NP potential and enables decoupled control of direct and quadrature motor currents based on the relative gain-array approach is presented in [14]. Applying neutral voltage imbalance property of NPC inverter, the majority of the current control techniques are proposed for active filtering [15]. Circular hysteresis current control based on space vector modulation for three-phase NPC inverter is presented in [16]. Complete automated current control using this algorithm is computationally very complex. Additionally, the switching frequency of the VSI in hysteresis control is strongly depending on the operating conditions and load parameters. The recent prevalent predictive current control strategy is presented in [17, 18]. However, current prediction prefers a high switching frequency to reduce the prediction error. The intricacy of SRF-PI controller is the tuning of PI parameters. However, a systematic modeling of the system with software platforms for autotuning of PI controllers enables the identification of the controller parameters. The steady state and transient responses of the controller must be considered to evaluate its effectiveness. This paper presents a current controller design, simulation, and testing for a three-level neutral point clamped inverter when driving R-L load. Synchronous sampling with symmetrical pulse width modulation (PWM) method is used, which increases the bandwidth of the current controller [19]. The time synchronization of different loops and dead time of inverter switches are considered in the controller design. The

comparison results validate the performance of the proposed controller.

2. Neutral Point Clamped Inverter

The neutral point clamped (NPC) inverter is the most widely used multilevel topology. The schematic circuit of a three-phase NPC with R-L load is shown in Figure 1(a). Each leg has four switches and two clamping diodes. These diodes are connected to the capacitor neutral point (NP) for voltage clamping. Two of the four switches are always ON to provide three levels in the phase voltage waveform. When two upper switches are ON, the phase voltage is half of the DC voltage. If two middle switches are ON, the phase voltage is zero. The phase voltage is negative half of DC link voltage when two lower switches are ON. The main modulation techniques for NPC inverter can be classified as carrier pulse width modulation (CPWM) and space vector PWM (SVPWM). The different CPWM techniques for NPC converters are presented in [20]. The three main techniques are phase disposition PWM (PDPWM), alternative phase opposition disposition (APOD), and phase opposition disposition (POD) PWM. The switching state relation to NP voltage imbalance can be clearly explained with space vector PWM (SVPWM). At the same time, it increases the computational complexity. CPWM method is simpler for implementation. PDPWM method is considered in this paper.

The PDPWM technique needs two carrier signals to specify the boundaries between the voltage levels. When the

FIGURE 2: PI current controller in synchronous reference frame.

TABLE 1: Inverter voltage levels with PDPWM.

$Tr_A < V_x > Tr_B$	$S_A = 1; S_B = 1$	$V_{dc}/2$
$Tr_A > V_x > Tr_B$	$S_A = 0; S_B = 1$	0
$Tr_A > V_x < Tr_B$	$S_A = 0; S_B = 0$	$-V_{dc}/2$

reference is greater than both carriers, the inverter is switched to $V_{dc}/2$. The inverter is switched to zero voltage level when the reference is lower than the upper carrier and higher than the lower carrier signal. The inverter voltage is $-V_{dc}/2$ when the reference goes lower than both carriers. The inverter voltage levels with PDPWM strategy are given in Table 1. This modulation strategy retains lower harmonic energy in the line-line inverter output voltage compared to other CPWM methods such as APDM/POD [21]. The switching diagram for PDPWM is given in Figure 1(b).

3. System Modeling

The state space model for a three-level NPC converter with the dead time effect is given in [22]. The inverter is modeled as a saturated voltage gain in per unit with DC voltage as base value. Therefore it does not include any state variables. Since it is assumed that the two capacitor voltages in the NPC converter are self-balanced, the voltages V_{c1} and V_{c2} can be excluded from the state variables. Therefore, the only time varying quantities are the inductor current and the inverter output voltage. Constant frequency operation does not have any state variables. The inverter with R-L load can be modeled ideally as

$$\frac{d}{dt}i(t)_{abc} + \frac{R}{L}i(t)_{abc} = \frac{1}{L}v(t)_{abc}. \quad (1)$$

4. Synchronous Reference Frame (SRF) Control

The stationary PI controller for voltage source inverters is conventionally regarded as unsatisfactory due to the incapability to eliminate the steady state errors [23]. This tracking error pushes the system towards its stability limit. In contrast, the SRF controller acts on dc signals and can achieve zero steady state error [24]. Additionally it gives better transient response for the inverter. The current regulator uses the dq reference frame to convert the signals from stationary frame to synchronously rotating frame and to perform the frequency shift on the system signals [25, 26]. The first step is to transform the signal in abc frame to $\alpha\beta$ coordinates using Clark's transformation method given by (2). The zero sequence current can be excluded in a three-phase balanced system. To achieve zero steady state error, the stationary reference frame signals are converted to dq frame using Park's transformation matrix given by (2). The SRF-PI controller block diagram is shown in Figure 2. Consider

$$[x_{\alpha\beta}] = T_{\alpha\beta} [x_{abc}]; \quad T_{\alpha\beta} = \begin{bmatrix} \frac{2}{3} & \frac{-1}{3} & \frac{-1}{3} \\ 0 & \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \end{bmatrix}, \quad (2)$$

$$[x_{dq}] = T_{dq} [x_{\alpha\beta}]; \quad T_{dq} = \begin{bmatrix} \cos(\omega_0 t) & \sin(\omega_0 t) \\ -\sin(\omega_0 t) & \cos(\omega_0 t) \end{bmatrix}. \quad (3)$$

The fundamental component of any variable can be precisely controlled in dq rotating frame which modifies the dynamic equations of the system. The dq -axis currents are compared to the corresponding references and fed to the PI controller. Two decoupled PI controllers are used to control the active and reactive currents. The reference input for q -axis current determines the load power factor. The normalized output of the PI controller is subjected to the inverse Clark and Park transformation to generate the reference signals for

FIGURE 3: The effect of low pass filter time constant in ac and dc signals. (a) The RMS value of current and phase shift (θ); (b) the amplitude reduction of the harmonic current.

FIGURE 4: (a) Sampling and switching time sequence and (b) closed-loop current controller.

the PWM controller using the transformation matrices given by

$$\begin{aligned} [x_{\alpha\beta}] &= T_{dq}^{-1} [x_{dq}]; \quad T_{dq}^{-1} = \begin{bmatrix} \sin(\omega_0 t) & -\cos(\omega_0 t) \\ \cos(\omega_0 t) & \sin(\omega_0 t) \end{bmatrix}, \\ [x_{abc}] &= T_{\alpha\beta}^{-1} [x_{\alpha\beta}]; \quad T_{\alpha\beta}^{-1} = \begin{bmatrix} 1 & 0 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 0 \end{bmatrix}. \end{aligned} \quad (4)$$

The effect of LPF in current sampling and method for delay compensation is presented in [27]. However, in dq frame, the fundamental frequency component is transformed to dc quantity and all the harmonics are transformed to non- dc quantities. The effects of LPF time constant (τ) in ac and dc signals are shown in Figures 3(a) and 3(b). Two first-order low pass filters are used to eliminate the harmonics from the dq currents. It is insensitive to phase errors [28]. Therefore, it does not have any role in the frequency response characteristics of the closed-loop transfer function. Additionally, the resource requirement is reduced while using LPF for the dq currents rather than in the abc frame.

5. Closed-Loop Controller

The transfer function of a PI controller in continuous time domain can be expressed as

$$G_{PI}(s) = k_p + \frac{k_i}{s}. \quad (5)$$

Using the Laplace transform, the system transfer function can be written as

$$G(s) = \frac{1}{Ls + R}. \quad (6)$$

The high sampling frequency increases the achievable current controller bandwidth, but at the same time it increases the noise content in the input waveform. To avoid aliasing without employing a very high sampling frequency, the sampling and switching frequency must be synchronized. The sampling and PWM updates are generated as shown in Figure 4(a). The additional small time constants such as processing time of the algorithm ($T_{\mu p}$), dead time of the inverter (T_0), and time delay of feedback filter and sampling (T_{fb}) are together approximated by a first-order inertia element:

$$G(d) = \frac{1}{T_d s + 1}, \quad (7)$$

where $T_d = T_{\mu p} + T_0 + T_{fb}$.

FIGURE 5: Matlab simulation block schematic for (a) circuit diagram, (b) controller, and (c) pulse generation.

The synchronization of control and switching actions is achieved by controlling the waiting length of both loops. In the proposed control scheme, synchronous sampling with symmetrical PWM method is used, which considers only one sampling point in a switching period. That is, the controller has a delay of one switching period (T_{sw}). The controller waiting loop length is set to T_s which is equal to the switching period if there is no additional delay. However, as the internal logic in the control loop takes an additional delay T_{ad} , the effective controller processing time is equal to $T_{es} = (T_s + T_{ad})$. Since the analog-to-digital converter (ADC) delay is smaller than the sampling time, this delay is excluded. The pulse generation loop runs faster than the control loop. The maximum speed of the pulse generation loop is equal to the dead time (T_0), which in turn is equal to the minimum width of the control pulse. Currents sampled at n th instant are available for use in the following interval, practically without any delay. The results of processing of control algorithms are written into the PWM at $(n + 1)$. Therefore, $T_{fb} = 0$. The closed-loop diagram for a current controlled inverter is shown in Figure 4(b). The closed-loop transfer function is

$G_c(s)$

$$= K \left[\frac{1 + sT_i}{s^3 + ((T_d + T_L) / (T_d T_L)) s^2 + ((1 + k) / (T_d T_L)) s + K T_i} \right], \quad (8)$$

where $k = k_p k_L$, $T_i = k_p / k_i$, $T_L = L/R$, and $K = k / T_i T_d T_L$.

TABLE 2: System parameters.

Load inductance (L)	1 mH
Load resistance (R)	10 Ω
Switching period (T_{sw})	540 μs
Dead time (T_0)	22.5 μs
Waiting loop length (T_s)	539.93 μs
Additional delay	75 ns

6. Simulation Results

In this paper, three-level NPC inverter connected to a three-phase balanced load is considered. Therefore, the zero sequence terms are ignored. To achieve independent control over the direct and quadrature axes currents, decoupling terms are included. For grid connected systems, the frequency can be extracted from the grid voltages. For standalone converters, frequency is the desired speed at which the inverter feeds power to the load. In most cases, this speed is constant. Therefore, the frequency values can be stored as LUT. The complete system simulation is done in Matlab/Simulink as shown in Figure 5.

The system parameters considered for simulation and experiment are given in Table 2. The feasibility of the controller is examined through simulation. The PI regulator follows the reference for $k_p = 13$ and $k_i = 722$. The initial values of I_{dref} and I_{qref} are set at 1 A and zero, respectively. It is

FIGURE 6: (a) PI controller response for step input and (b) line-line voltage, phase voltage, and load current.

FIGURE 7: Experimental set-up using NPC prototype.

a common practice for a grid connected system to achieve current injection at unity power factor. The step response of the controller is analyzed by changing the I_{dref} to 2 A at 2.25 sec. The controller takes 0.3 sec for settling the new value. The PI controller response is given in Figure 6(a). The inverter line-line voltage, phase voltage, and load currents are given in Figure 6(b) showing the step change. For the initial value I_{dref} , the inverter modulation index is less than 0.5. During this time, the inverter output is in two voltage levels. When a step change occurs in the current reference, the controller increases the modulation index above 0.5. Thereby, the inverter output voltage has three levels.

7. Experimental Results

Three modules of SKM300MLI066TAT IGBT (insulated gate bipolar transistor) modules are used for building the three-level inverter. A dual channel concept 2SC0105T2AA0-17 driver with 2BB0108T2A0-17 evaluation board is used for driving each complementary IGBT switch. The turn-off snubber is used for protecting the device from over-voltages. Varistors are used for the overvoltage protection on the DC link. Figure 7 shows the experimental system developed in the laboratory. The current control technique is implemented on FPGA (field programmable gate array) using a Labview/CompactRio real-time module, which is plugged into a PC. Three-phase load with 2 mH inductance and 10 Ω resistance is used. The three-phase currents are

measured using hall-effect sensors and the sensor outputs are connected to a 16-bit analog-to-digital converter (ADC) module of Labview/CompactRio. The ADC has a delay of 6.5 μ s.

The complete control algorithm is implemented in two independent parallel loops as shown in Figure 8, where Figure 8(a) is the SRF control schematic and Figure 8(b) is the pulse generation loop in Labview user interface. The two loops are synchronized to provide a single value of sampled reference signal to obtain symmetrical PWM. It is achieved by setting a waiting length of the control loop such that the sum of the control loop waiting length and the additional delay in internal logic is equal to the switching time. The same values of K_p and K_i as obtained from the simulation are used for the implementation. Figure 9(a) shows the step response of the PI controller implemented in Labview. The controller takes 0.5 s for settling the new value. Figure 9(b) shows the inverter line-line voltage, phase voltage, and load currents from the experiments. The implemented controller works exactly as in the simulation.

8. Conclusion

The load current control for a three-level NPC inverter connected to three-phase balanced load is examined. The current controllers using PI compensators in synchronous reference frame are implemented. The delays associated with dead time, low pass filter, and sampling are included in the calculation of the controller parameters. The loop synchronization is done by adjusting the software loop waiting length. The simulation is validated with experimental results. The control algorithm is implemented in Labview/FPGA. It is seen from the experimental results that the controller is capable of feeding the load current corresponding to the reference value with zero steady state error.

(a)

(b)

FIGURE 8: (a) Control loop and (b) pulse generation loop in Labview.

(b)

FIGURE 9: Experimental results. (a) PI controller response for the step input, (b) the line-line voltage (y-axis: 40 V/div and x-axis: 30 ms/div), phase voltage (y-axis: 40 V/div and x-axis: 30 ms/div), and phase current (y-axis: 5 A/div and x-axis: 30 ms/div) of the inverter are shown for a step change in current demand.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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