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Research Article

Development of a New Cascade Voltage-Doubler for Voltage Multiplication

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For more than eight decades, cascade voltage-doubler circuits are used as a method to produce DC output voltage higher than the input voltage. In this paper, the topological developments of cascade voltage-doublers are reviewed. A new circuit configuration for cascade voltage-doubler is presented. This circuit can produce a higher value of the DC output voltage and better output quality compared to the conventional cascade voltage-doubler circuits, with the same number of stages.

1. Introduction

Due to various types of applications, there is always a demand for much higher voltage level. However, based on the energy sources or insulation limits, subsisted power supplies could produce voltages lower than their requisite. Therefore, many attempts have been made to discover ways to generate a voltage, higher than the supply voltage. Many methods have been utilized to do this task. Some of the most commonly applied methods for producing a voltage larger than the power supply voltage include step-up transformers [1], voltage-doubler [2, 3], multiplier circuits [4–6], charge pump circuits [7], switched-capacitor circuits [8, 9], and boost or step-up converters [10–13]. Among these methods, diode-capacitor topologies are more suitable. One of the most popular diode-capacitor topologies for doing this purpose is the Villard voltage-doubler [2]. It was also called "Greinacher voltage-doubler" first presented by Heinrich Greinacher between 1919 and 1921 [14]. This circuit was a simple combination of the clamper [15] and peak holder circuit [16] which is shown in Figure 1.

In this circuit, the voltage clamper can shift the DC offset of the input AC voltage from zero to the peak value of the $\widehat{V}_{\text{in}}$ volts. Therefore, the output from the voltage clamper circuit is oscillating between zero and $2\widehat{V}_{\text{in}}$. Finally, the peak holder circuit captures the peak of its input voltage and holds the DC value of $2\widehat{V}_{\text{in}}$ in its output. In other words, the presented circuit in Figure 1 can convert an input AC voltage to a doubled DC voltage across its output.

In 1932, Cockcroft and Walton introduced a complex cascade voltage-doubler that is shown in Figure 2 [4] and they received the Nobel Prize in 1951 for this work [17]. This circuit could produce a steady potential of about 700 kV that was three times greater than the applied input voltage. However, due to existence of series connected coupling capacitances, the high coupling voltage drop happens in this configuration. This phenomenon causes a small voltage gain for the circuit of Figure 2. Furthermore, series connected output capacitor causes a low output capacitance. In this circuit, except C_{s1}, other output capacitors were holding a floating voltage. Therefore, employing the stored electrical charge in each capacitor, individually, for other applications was complex.

In 1976, Dickson proposed a cascade diode-capacitor circuit, which was an improvement for the Cockcroft-Walton circuit (Figure 2) [7]. This circuit configuration, known as "charge pump," required clock pulses as the input of the coupling capacitors. The presented topology of the Dickson circuit was simpler than the Cockcroft-Walton circuit. However, requiring the clock pulses can limit utilizing this circuit for high-voltage applications. Figure 3 shows the Dickson charge pump, which is a kind of cascade voltage-doubler.

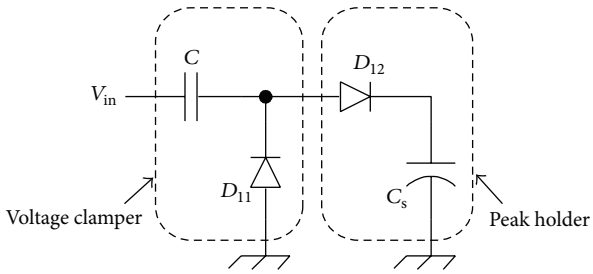

Figure 1: Voltage-doubler [2].

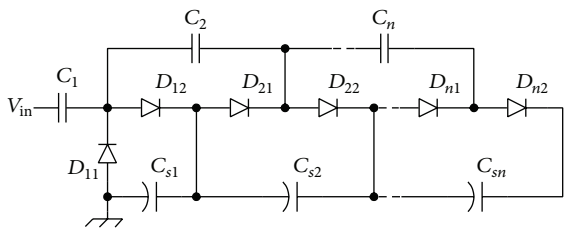

Figure 2: Cockcroft-Walton cascade voltage-doubler circuit [4].

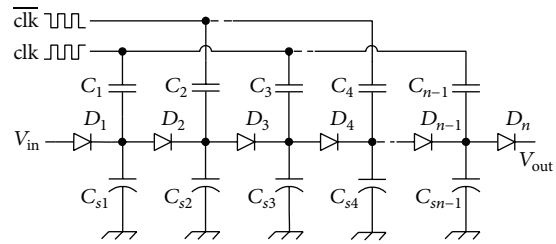

Figure 3: Dickson charge pump circuit [7].

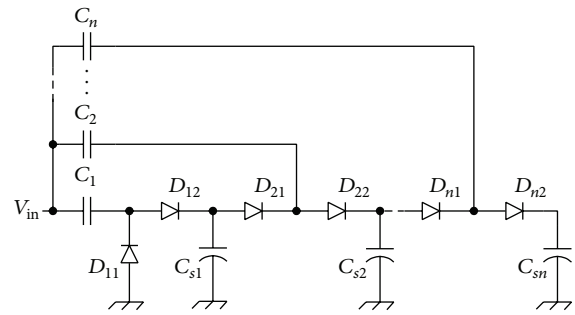

Figure 4: Karthaus-Fischer cascade voltage-doubler circuit [5].

In 2003, Karthaus and Fischer [5] have simplified and improved circuit of the Cockcroft-Walton [4] (Figure 2) as shown in Figure 4. This improved circuit configuration was modifying the Dickson circuit [7] transformation. However, in Karthaus-Fischer cascade voltage-doubler [5], the clock pulses were eliminated, as the numbers of coupling and stray capacitors were reduced. Therefore, the essential requirements of the circuit became less than the Dickson circuit (Figure 3) [18]. Based on the achievement, the Karthaus-Fischer circuit [5] can even be utilized for high-voltage applications. In addition, the input impedance of the Cockcroft-Walton circuit [4] was reduced by changing the connection of the coupling capacitors, and its output capacitance is increased by using an independent grounded stray capacitor for each stage, in Karthaus-Fischer circuit (Figure 4) [5].

Based on the review, the existing cascade voltage-doublers can produce an output voltage higher than the applied input voltage. However, a new circuit configuration that can provide a higher DC output voltage with lower ripple and faster output settling-time is in demand. This high DC voltage must be produced by employing the same number of stages as the conventional cascade voltage-doublers (Figures 2 and 4).

The paper presents a new cascade voltage-doubler circuit configuration. The proposed circuit is verified by simulation and comparing its output results with the previous cascade voltage-doubler circuits (Figures 2 and 4).

2. Methodology

Based on the approach of Karthaus-Fischer (Figure 4) [5], we proposed the new developed circuit configuration which is shown in Figure 5. The considerable difference between the proposed circuit and the Karthaus-Fischer circuit (Figure 4) is that the Karthaus and Fischer circuit used only one source to feed the circuit, but in the proposed circuit configuration (Figure 5), each coupling capacitor is supplied through an individual input power supply where the amplitude of its voltage in each stage is the number of that stage times the amplitude of the input voltage in the first stage. This is to attain a higher value of DC voltage compared to the conventional Cockcroft-Walton (Figure 2) and Karthaus-Fischer (Figure 4) circuits.

On the other hand, unlike the Cockcroft-Walton circuit (Figure 2) which was used as a double anti-ladder topology and Karthaus-Fischer circuit (Figure 4) which was an unbalanced ladder topology, the proposed cascade voltage-doubler circuit configuration (Figure 5) is a modified unbalanced ladder topology. In other words, this topology (Figure 5) is an open unbalanced ladder which is a cascade biased tee topologies. A bias tee is a three-port network employed for mounting the DC bias point at each stage without disturbing other stages. Moreover, the output of each biased tee is connected to a grounded capacitor.

In this paper, we have simulated the SPICE NetList for the three circuits of Figures 2, 4, and 5, in five stages. In the NetList file, the actual model for each electronic component was used. In this simulation, the input voltage source, V_{in}, is a sinusoidal wave with the peak value of 100 V. The purpose of choosing this voltage value is to diminish the uncertain voltage drop effects in the final output voltage. This can only be attained where the selected input voltage is much greater than the diode's voltage drop. All circuits have achieved higher output voltage at the optimal operation frequency of about 50 kHz [19]. Hence, this frequency is used for the input power supply. Both coupling, C_n, and stray capacitance, C_{sn}, are 100 nF. The diodes, D_{n1} and D_{n2}, are ultrafast avalanche sinter-glass diodes with very low switching losses and operating capability at high-frequency.

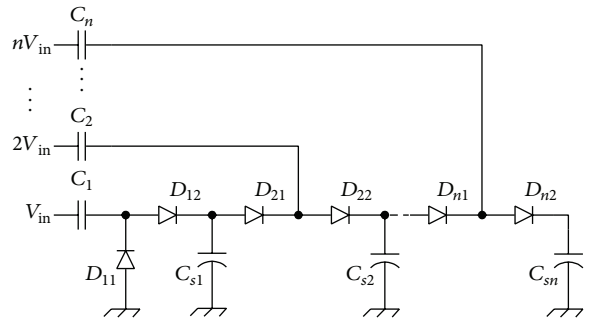

FIGURE 5: Proposed cascade voltage-doubler circuit configuration.

In all simulated circuits, the output voltage of each stage is measured and compared with other circuits (Figures 2 and 4). Moreover, the rate of the output voltage improvement, in time-domain, for the new topology of the cascade voltage-doubler, compared with the old circuit configuration, is calculated. Thus, the improvement rate function is defined as

$$\nu(t) = 20\log_{10}\left(\frac{V_{\text{out,new}}(t)}{V_{\text{out,old}}(t)}\right), \quad (1)$$

where ν is the output voltage improvement rate in decibel, dB, $V_{\text{out,new}}$ is the output voltage of the newer topology, and $V_{\text{out,old}}$ is the output voltage of the previous circuit configuration.

The output voltage in time-domain has two components of transient and steady state. By knowing the transient and steady state of the waveform and their correlations with other parameters of the output, the quality of the produced output voltage can be specified. However, a shorter transient-time or faster settling-time and higher DC voltage with a lower value of the ripple are desirable. In this paper, the settling-time of 3% error with the steady state output voltage is used to distinguish between the transient and steady state of the output voltage in each stage. Both values of the output DC voltage and the ripple are measured in the steady state.

3. Results and Discussions

Results of the output voltage (at fifth stage) for different cascade voltage-doubler topologies are shown in Figure 6. Based on this result, in Cockcroft-Walton circuit (Figure 2), the output voltage across the series connected capacitors, C_{s1}, C_{s2}, C_{s3}, C_{s4}, and C_{s5}, has a long transient-time of 4.74 ms. Moreover, a notable ripple occurred during the transient-time, but this ripple diminished to a very small amount, during the steady state. The highest value of the output DC voltage in steady state is 978.8 V. In Karthaus-Fischer circuit (Figure 4), the transient duration is significantly improved to 2.68 ms, which is about 1.8 times less than the duration in Cockcroft-Walton circuit (Figure 2), with a very small ripple. However, the amount of the produced output DC voltage, in Karthaus-Fischer circuit (Figure 4), is increased only about 10 V and reached the maximum value of 989.1 V which is a bit higher than the value in Cockcroft-Walton circuit (Figure 2). It shows that, by changing the connection of the coupling capacitors, the input impedance of the cascade

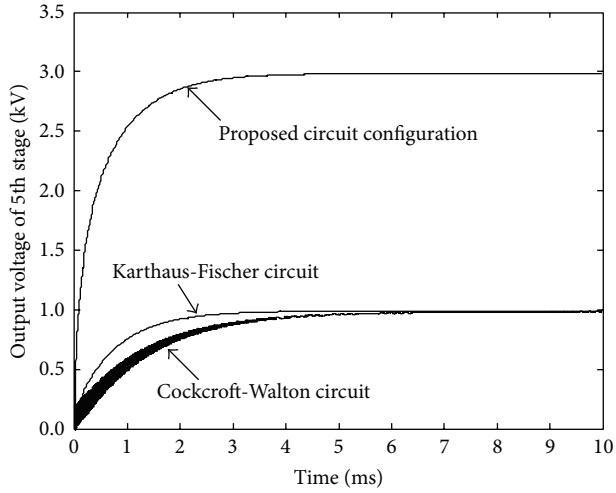

FIGURE 6: The fifth stage output voltage of different cascade voltage-doubler topologies; Cockcroft-Walton circuit (Figure 2), Karthaus-Fischer circuit (Figure 4), and the proposed circuit configuration (Figure 5).

voltage-doubler topology of Figure 4 is reduced to a lower value in comparison with the earlier topology of Figure 2. This leads to achieve a better performance in terms of the rise-time and smaller voltage drop. Thus, Karthaus-Fischer circuit (Figure 4) is improved further when the connection of the coupling capacitors is transformed to the proposed circuit configuration of Figure 5 with additional input sources which are added to the circuit. In the proposed circuit configuration, the transient duration is reduced to 2.30 ms, which is 380 μs less than this time in Karthaus-Fischer circuit (Figure 4). The value of the produced output DC voltage in the stray capacitor in the fifth stage, C_{s5}, is 2984.9 V which is about three times more than the produced output DC voltage of Figures 2 and 4 circuits.

By using (1), the output voltage improvement rate as a function of time is calculated and results are shown in Figure 7. Based on the results, the output voltage of the Karthaus-Fischer circuit (V_{KF}) is significantly (maximum 60.4 dB) improved in comparison with the produced output voltage of the Cockcroft-Walton circuit (V_{CW}) during the rise-time, but this improvement rate after the settling-time is damped to the nearby zero. The result of this ratio for the output voltage of the proposed circuit configuration (V_{New}) compared with the V_{KF} is different. The new proposed circuit shows an improvement of maximum 14.3 dB in the beginning, but this ratio is reduced to 9.7 dB at the settling-time, but this value does not change much during the steady state and reaches the minimum of 9.6 dB. These results show that the proposed circuit configuration performs significantly better than the earlier cascade voltage-doublers (Figures 2 and 4).

Results of the DC output voltage (steady state) in each stage are shown in Figure 8. It is observed that the produced output DC voltages in the conventional cascade voltage-doubler of Cockcroft-Walton (Figure 2) and

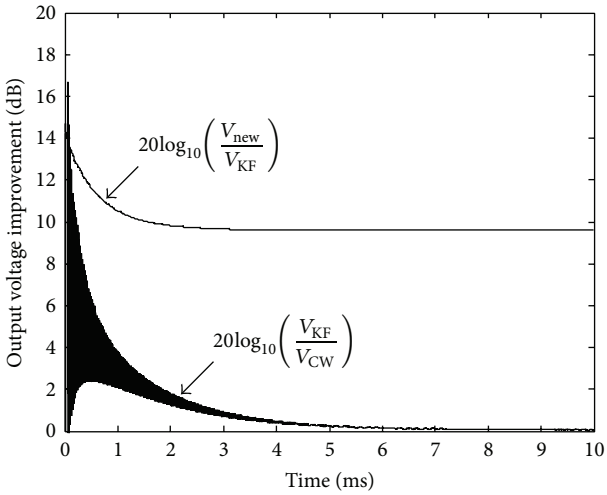

Figure 7: Rate of the output voltage improvement.

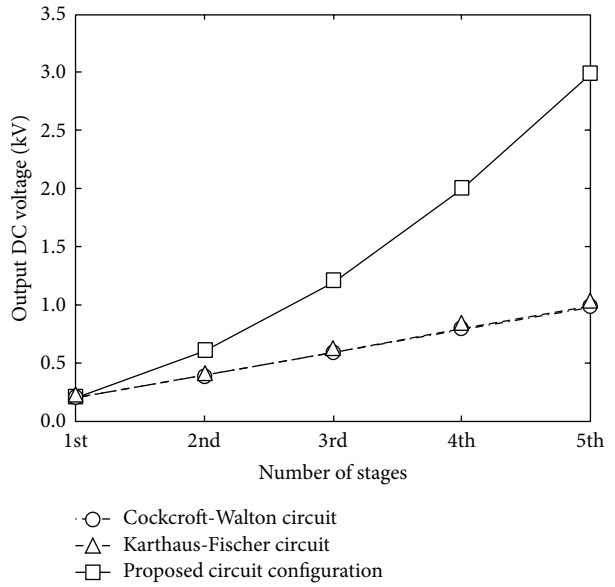

Figure 8: Output DC voltage in each stage.

Karthaus-Fischer (Figure 4) are very close and increases linearly when the number of stages increases. In other words, if an ac voltage waveform such as

$$V_{\text{in}}(t) = \widehat{V}\sin(\omega t - \varphi) + k \tag{2}$$

is applied to the Cockcroft-Walton (Figure 2) or Karthaus-Fischer circuit (Figure 4), the relationship of the DC output voltage with the number of stages, n, and applied input voltage, V_{in}, can be defined as

$$V_{\text{DC}}(n, V_{\text{in}}) = 2n\widehat{V} - \Delta(n), \tag{3}$$

where Δ is the voltage drop as a function of the number of stages and can be expanded as

$$\Delta(n) = \delta V_C(n) + \delta V_D(n) + \delta_0(n), \tag{4}$$

where δV_C is the voltage drop across the coupling capacitors and δV_D is the voltage drop on diodes. The amount of these voltage drops directly depends on the number of stages. However, during simulation and experimental processes, some undesirable errors can appear in final results. These errors are including the input uncertainty due to some input parameters which were not well defined; model uncertainty because of alternative model formulations, structure, or implementation; numerical uncertainty results from the influence of discretization and iterative convergence errors; and various experimental uncertainties which can happen due to the natural characteristic of manufacturing different electrical components. Superposition of these errors sometimes can be significantly big. These error uncertainties are integrated and shown as δ_0 in (4). Minimizing mentioned error uncertainties during the simulation or experimental process can significantly reduce the effect of δ_0 and make the theoretical, simulation, and experimental results almost similar.

On the other hand, the produced DC output voltage of the proposed circuit configuration versus the number of stages is a parabolic curve. Therefore, the DC output voltage of the proposed circuit configuration (Figure 5) as a function of number of stages, n, and applied input voltage, V_{in}, can be outlined via the following proposed equation:

$$V_{\text{DC}}(n, V_{\text{in}}) = n(n+1)\widehat{V} - \Delta(n). \tag{5}$$

Results for the rate of the ripple to the output DC voltage (steady state) in each stage are shown in Figure 9. In all cascade voltage-doublers, which are simulated in this paper, the ratio is less than 1%. It means that the produced voltage quality in steady state is good. However, the proposed circuit configuration (Figure 5) and Karthaus-Fischer circuit (Figure 4) have shown better quality compared with the Cockcroft-Walton (Figure 2). It must be noted that the ratio of the ripple to the output DC voltage, in the first to the third stages, was better in Karthaus-Fischer circuit (Figure 4) in comparison to the proposed circuit configuration (Figure 5), but it becomes closer by increasing the number of stages.

In the presented circuits, the value of the settling-time is a very important issue. Of course, the smaller value would be more desirable. It means that by minimizing the settling-time, the circuit can produce the expected amount of the DC voltage faster. Results for the settling-time of the output voltage in each stage are shown in Figure 10. Although the difference between these times in all circuits was not much in the first stage, by increasing the number of stages this difference is becoming more significant. In all stages the proposed circuit configuration and Karthaus-Fischer circuit (Figure 4) have shown shorter settling-time compared with the Cockcroft-Walton (Figure 2). The value of the settling-time of Karthaus-Fischer circuit (Figure 4) does not change much by changing the number of stages, but this value became smaller when the number of stages increased in the proposed circuit configuration (Figure 5).

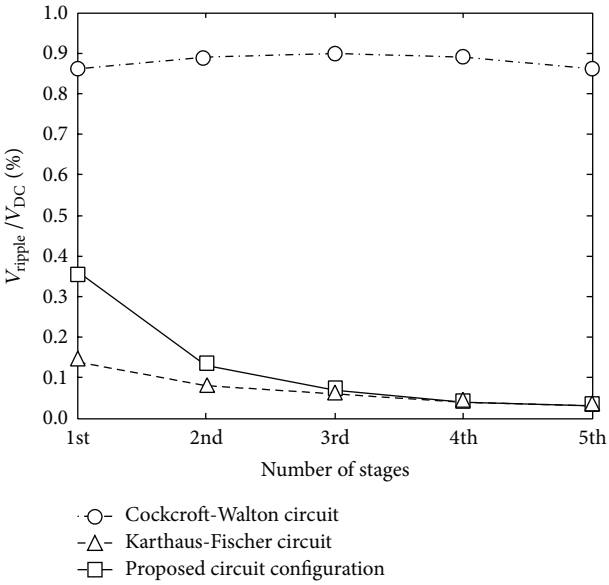

Figure 9: Rate of the ripple to the output DC voltage in each stage.

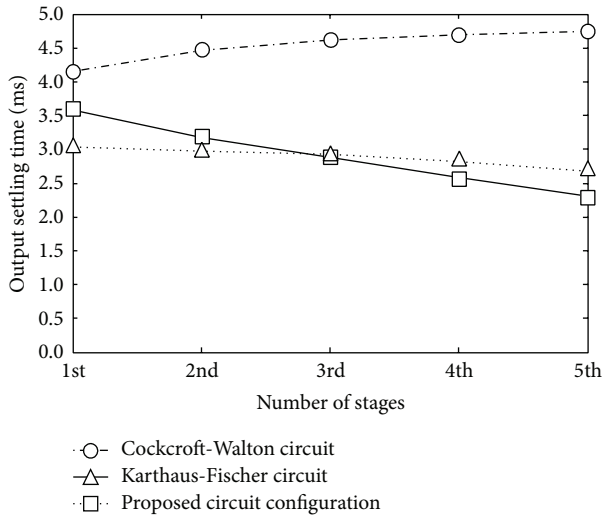

Figure 10: Settling-time of the output voltage in each stage.

Finally, comparison of conventional cascade voltage-doublers (Figures 2 and 4) with the proposed circuit configuration (Figure 5) proves that higher-voltage capability, low coupling voltage drop, requiring fewer numbers of stages, and big voltage gain are significant advantages of this configuration. Besides, the proposed circuit needs a multi-input supply which is the limitation of this configuration.

4. Conclusion

In this paper, a new developed topology of cascade voltage doubler was proposed (Figure 5). Two of the conventional cascade voltage-doublers [4, 5] and proposed circuit configurations (Figure 5) were simulated. The five-stage proposed cascade voltage-doubler used multiplies of 100 V as its input supplies at the frequency of 50 kHz to generate about 3 kV DC voltage at its output. However, the conventional cascade voltage-doublers were able to generate a maximum of about 1 kV with the same number of stages. The output voltages of these cascade voltage doublers at the fifth stage in time-domain were compared and presented. The output voltage improvement rate as a function of time was calculated and the results were demonstrated and discussed. Settling-time for the output voltage, output DC voltage, and ratio of the ripple to the output DC voltage (steady state) in each stage were defined, compared, and discussed. The relationship between the output voltage, applied input voltage and the number of stages was carried out and (5) for calculating the output voltage of the proposed circuit configuration was suggested. This suggested equation includes the effect of the voltage drops, Δ. In all reported cases, the proposed circuit configuration has shown a better performance compared to the other conventional cascade voltage-doublers [4, 5]. Moreover, Table 1 briefs a comparison between the cascade voltage-doublers, which were mentioned in this paper. In comparison with conventional circuits (Figures 2 and 4), it shows that the cascade input supply topology has made an unwanted complexity for understanding the performance of the proposed circuit (Figure 5). However, considering the advantage of producing higher output voltage compared to the conventional circuits, the disadvantage of multi-input supply's complexity can be neglected. Finally, the proposed new circuit configuration can be suggested for applications

Table 1: Comparing the different topologies of the cascade voltage-doublers.

Circuit	Advantages	Disadvantages
CW [4], Figure 2	(i) Single input supply (ii) High-voltage capability	(i) High coupling voltage drop (ii) Low output capacitance (iii) Floating output capacitor (iv) Small voltage gain
Dk [7], Figure 3	(i) DC input supply (ii) Low coupling voltage drop	(i) Low-voltage application (ii) Needs clock pulses (iii) Small voltage gain
KF [5], Figure 4	(i) Single input supply (ii) High-voltage capability (iii) Low coupling voltage drop	(i) Needs many stages (ii) Small voltage gain
New, Figure 5	(i) Higher-voltage capability (ii) Low coupling voltage drop (iii) Requires fewer numbers of stages (iv) Big voltage gain	(i) Multi-input supply

CW: Cockcroft-Walton circuit. Dk: Dickson circuit. KF: Karthaus-Fischer circuit. New: proposed circuit configuration.

where a high amount of output voltage is needed. By distributing the input voltage to a cascaded input supply, which is feeding each voltage doubler separately, it can avoid the limitation of the insulation breakdown voltage which is found in conventional circuit configurations.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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