

Research Article

Self-Passivation by Fluorine Plasma Treatment and Low-Temperature Annealing in SiGe Nanowires for Biochemical Sensors

Kow-Ming Chang,¹ Chiung-Hui Lai,² Chu-Feng Chen,¹ Po-Shen Kuo,¹ Yi-Ming Chen,¹ Tai-Yuan Chang,¹ Allen Jong-Woei Whang,³ Yi-Lung Lai,³ Huai-Yi Chen,⁴ and Ing-Jar Hsieh⁵

¹ Department of Electrical Engineering and Institute of Electronics, National Chiao Tung University, No. 1001, University Road, Hsinchu 300, Taiwan

² Department of Electronics Engineering, Chung Hua University, No. 707, Sec. 2, WuFu Road, Hsinchu 300, Taiwan

³ Department of Electronic and Computer Engineering, National Taiwan University of Science and Technology, Taipei 106, Taiwan

⁴ Department of Electronic Engineering, Huaan University, New Taipei City 223, Taiwan

⁵ Department of Electrical Engineering, Chung Hua University, No. 707, Sec. 2, WuFu Road, Hsinchu 300, Taiwan

Correspondence should be addressed to Chu-Feng Chen; grapechen@gmail.com

Received 1 March 2014; Revised 14 May 2014; Accepted 15 May 2014; Published 11 June 2014

Academic Editor: Oleg I. Lupan

Copyright © 2014 Kow-Ming Chang et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Nanowires are widely used as highly sensitive sensors for electrical detection of biological and chemical species. Modifying the band structure of strained-Si metal-oxide-semiconductor field-effect transistors by applying the in-plane tensile strain reportedly improves electron and hole mobility. The oxidation-induced Ge condensation increases the Ge fraction in a SiGe-on-insulator (SGOI) and substantially increases hole mobility. However, oxidation increases the number of surface states, resulting in hole mobility degradation. In this work, 3-aminopropyltrimethoxysilane (APTMS) was used as a biochemical reagent. The hydroxyl molecule on the oxide surface was replaced by the methoxy groups of the APTMS molecule. We proposed a surface plasma treatment to improve the electrical properties of SiGe nanowires. Fluorine plasma treatment can result in enhanced rates of thermal oxidation and speed up the formation of a self-passivation oxide layer. Like a capping oxide layer, the self-passivation oxide layer reduces the rate of follow-up oxidation. Preoxidation treatment also improved the sensitivity of SiGe nanowires because the Si-F binding was held at a more stable interface state compared to bare nanowire on the SiGe surface. Additionally, the sensitivity can be further improved by either the N₂ plasma posttreatment or the low-temperature postannealing due to the suppression of outdiffusion of Ge and F atoms from the SiGe nanowire surface.

1. Introduction

One-dimensional (1D) nanostructures, such as Si nanowires and ZnO nanorods, have been demonstrated as good candidates for ultrasensitive, miniaturized molecule sensors in biological, chemical, and optical applications [1–7]. The physical properties of biosensor devices fabricated from silicon depend on biochemical/molecular sensitivity. Nanoscale semiconductor processes can be used to improve chemical detection sensitivity. A basic phenomenon associated with

the planar semiconductor process that can be exploited in biological sensors is surface potential modification. An important feature of nanowires is their ultrahigh surface-to-volume ratio, which is essential for ultrasensitive detection of chemical or biomolecular species. Since the conductivity of nanowires depends on the surface charges around their surfaces, one way to improve the sensitivity of the nanowire sensor is to use various biomolecular coatings for detecting viruses, proteins, ions, and DNA [8–10]. Strained silicon MOSFETs can be used to increase their electron and hole

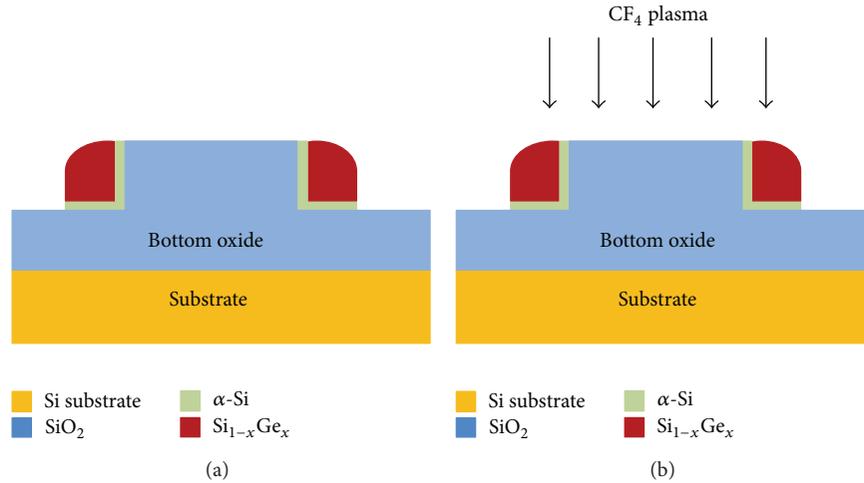


FIGURE 1: The schematics of different SiGe nanowire surface treatment processes: (a) the “bare” SiGe nanowire without any plasma treatment and (b) the SiGe nanowire with fluorine plasma treatment.

mobility. To maximize hole mobility, the fraction x of $\text{Si}_{1-x}\text{Ge}_x$ should be approximately 0.3 [11]. The SiGe-on-insulator (SGOI) process [12] has great potential for fabricating high-sensitivity nanowire sensors. Using Ge condensation to induce formation of SiGe-on-insulator (SGOI) nanowires, enhances conductance by increasing hole carrier mobility. During the Ge condensation process used to fabricate ultrathin SiGe-on-insulators with a high Ge fraction, Ge pile-up occurs at the SiO_2/SiGe interface. However, oxidation increases the trap density at the SiO_2/SiGe interfaces by approximately 10^{12} cm^{-2} [13]. At its free surface, Si generally has an interface state approximating $10^{15} \text{ cm}^{-2} \text{ eV}^{-1}$. The stability of this surface state can be increased by deposition of a thermal SiO_2 passivation layer to reduce the interface state of the SGOI nanowire surface to less than $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ [14]. Plasma fluorination process also reduces defects at the SiO_2/Si interface during the VLSI process [15, 16]. Since fluorine atoms enhance the thermal oxidation rate [17], the enhanced thermal oxidation rate accelerates the formation of a thermal oxide layer, which, like a capping oxide layer, reduces the rate of follow-up oxidation. Otherwise, F atoms terminate Si dangling bonds and replace weak Si-H bonds to prevent the defects and dangling bonds from reducing the conductivity of transport carriers. This study compared the effects of surface state on biochemical detection sensitivity in boron-doped SiGe nanowires with and without surface treatment.

2. Experimental Procedure

Strategies typically used to fabricate nanowires can be classified as bottom-up methods (e.g., thermal evaporation [18], laser ablation, and the vapor-liquid-solid methods (VLS) [19]) or top-down methods (e.g., advanced photoemission approaches, including EUV to X-ray [20], AFM [21], nanoimprinting [22], and methods that use side-wall spacers [23]). The side-wall spacer technique is the cheapest and easiest method of fabricating a nanowire sensor. Accordingly,

the nanowire samples in this study were fabricated by a side-wall spacer process. A p-type (boron-doped) Si substrate (100) with a resistance of 8~10 ohm-cm was used. After an initial standard RCA cleaning, the 500 nm thick oxide was grown on the Si substrate by wet oxidation at 980°C for seven hours. Then, the oxide layer was patterned by optical lithography and dry etching. The thickness of the remaining oxide is around 300 nm. This 300 nm thick oxide layer served as the bottom oxide in side-wall spacer etching. A 20 nm thick amorphous Si ($\alpha\text{-Si}$) layer was deposited by LPCVD at 650°C , and a 200 nm thick $\text{Si}_{0.86}\text{Ge}_{0.14}$ layer was deposited by UHV-CVD at 655°C after RCA cleaning of the wafer. The side-wall-spacer nanowires were formed by self-aligned etching. Figure 1 schematically depicts two SiGe nanowire samples with and without surface plasma treatment. Figure 1(a) shows a bare SiGe nanowire without surface treatment, and Figure 1(b) shows a SiGe nanowire after fluorine plasma treatment. After formation of the $\alpha\text{-Si}/\text{SiGe}$ layer, the samples were treated in a diluted O_2 gas ambient environment for 3 min. The nanowires were then annealed for 180 s in N_2 gas. After oxidation and N_2 gas annealing, the nanowires were implanted with $3 \times 10^{15} \text{ ions/cm}^2$ of BF_2 to form p-type nanowires. The final metallization process was deposition of a 500 nm thick layer of aluminum followed by Al sintering at 400°C . Finally, the electrodes were defined by mask process. The $\alpha\text{-Si}/\text{SiGe}$ nanowires were functionalized by using 3-aminopropyltrimethoxysilane (APTMS) to modify the silicon oxide surfaces surrounding the nanowires. A hydroxyl functional group on the oxide surface was replaced by methoxy groups of APTMS modules, and the nanowire surfaces were simultaneously terminated by amine groups. When the surface charges of the proposed SiGe nanowires were modified by APTMS, pronounced conductance changes were observed, leading to high sensitivity for chemical/biochemical sensing. The proposed SiGe nanowire was one-time usable and its response time after APTMS dripped on nanowire was around 10~30 s. A Hewlett Packard HP 4156A was used to measure the

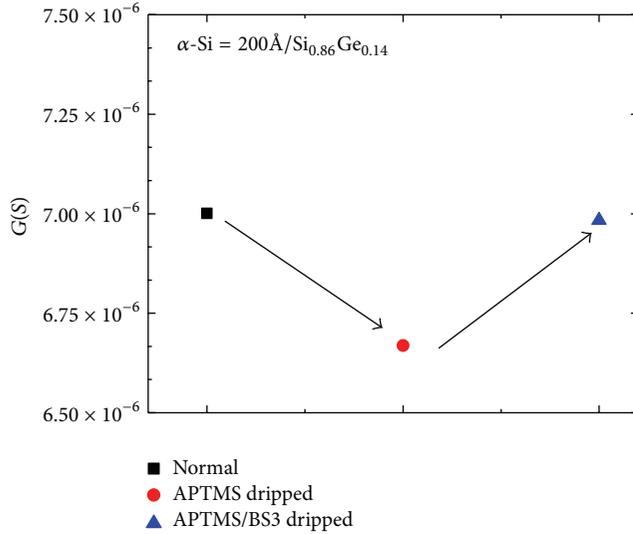


FIGURE 2: The functionalization of the 20 nm α -Si/Si_{0.86}Ge_{0.14} nanowire after APTMS and BS3 dripping.

electrical characteristics of the nanowire sensor. The drain voltage (VD) was varied from -10 to 10 V in steps of 500 mV, and the back gate voltage was fixed at 0 V. The electrical characteristics were measured at each stage of the surface modification, and the average conductance was then extracted from the ID-VD characteristics for a $VD = 3\sim 6$ V. The sensitivity (S) of a nanowire-based sensor was defined as the ratio of the magnitude of the change in conductance to the baseline conductance:

$$S = \frac{|G - G_0|}{G_0} = \frac{\Delta G}{G_0}, \quad (1)$$

where G_0 represents the conductance before capture of a molecule; G is the conductance after capture of a molecule, and ΔG is the difference between G and G_0 .

3. Results and Discussion

The SiGe nanowires were functionalized by using APTMS to modify their surrounding silicon oxide surfaces. The hydroxyl functional group on the oxide surface was replaced by the methoxy groups of the APTMS molecule, and the nanowire surface was simultaneously terminated by amine groups. Next, bis (3-sulfo-N-hydroxysuccinimide ester) sodium salt (BS3) was used to link the APTMS with the IgG antibody. Figure 2 presents the conductance characteristics of a nanowire after APTMS and BS3 were dripped onto the nanowire surfaces. Conductance was decreased in nanowires treated by drip application of APTMS on their surfaces. The APTMS tended to become positively charged, as reflected in the decrease of the conductance when hole carriers were depleted from the surface of the p-type nanowire. The conductance of the APTMS-modified nanowire increased after drip application of BS3. These experimental results indicate that the BS3 reduced the surface potential and caused hole carriers to accumulate at the nanowire surface.

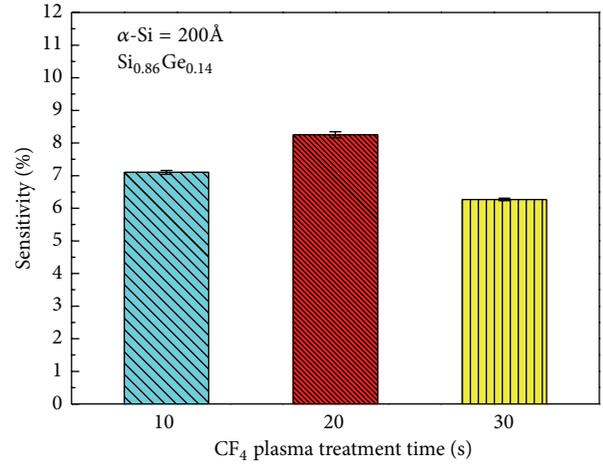


FIGURE 3: The sensitivity of Si_{0.86}Ge_{0.14} nanowire with period of treatment by CF₄ treatment.

The functionalization was consistent with the results of our previous experiments in n-type SiGe nanowire [24]. The hydroxyl molecules were replaced by the methoxy sides of the APTMS molecules, which caused the surface potential of the nanowire to become positive and deplete the hole carriers. As the BS3 molecules released sodium ions or broke the single bonds between the carbon atoms and the oxygen atoms, the accumulation of the hole carriers changed the surface potential from positive to negative. Figure 3 depicts the sensitivity of Si_{0.86}Ge_{0.14} nanowires by different CF₄ plasma treatment times. There were 8 tested samples for production of error bars. The results show that the sensitivity of the sample by plasma treatment time of 20 s is better. It can be speculated that the oxidation rate becomes slow because oxygen needs to diffuse through the capping layer. The oxidation rate in the samples capped with an oxidation layer is reduced, further suppressing the formation of surface defects. The free surface of a semiconductor is well known to have high surface state as a result of its dangling bonds. Accumulation of Ge at the nanowire surface during the Ge condensation process also causes interface defects. Thus, a SiGe nanowire without an oxide capping layer should have a lower conductance compared to one with an oxide-capped sample. The oxide cap was exploited to increase the biochemical sensitivity of SiGe nanowires [25]. Since fluorine atoms enhance thermal oxidation [17], the enhanced thermal oxidation rate assumedly causes a thermal oxide layer to form rapidly. Like a capping oxide layer, the thermal oxide layer reduces the rate of follow-up oxidation. This self-passivation effect was verified in a control sample of p-type wafers that had received varying durations of fluorine plasma treatment. The oxide thickness was measured with an ellipsometer. Figure 4 plots the oxide thickness after varying durations of CF₄ plasma treatment. The sample by plasma treatment time of 20 s obtained the lowest passive oxide thickness. Although nanowire samples that received a longer treatment had a thicker oxide layer and a lower oxidation rate, fewer O₂ atoms passed through their thick oxide layers,

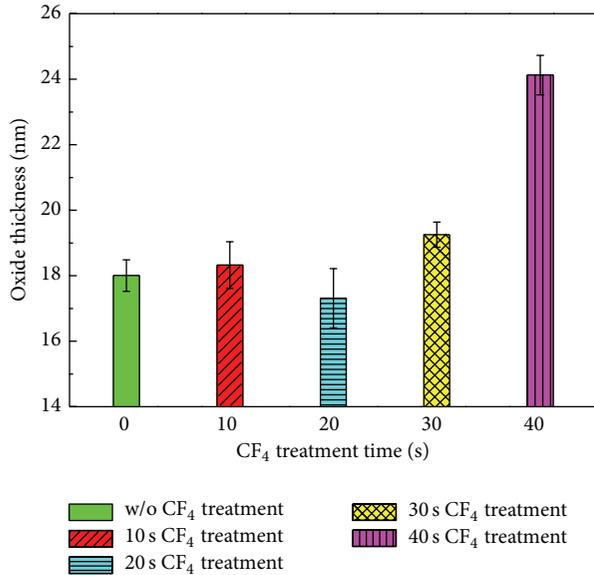


FIGURE 4: The oxide thickness after varying durations of CF₄ plasma treatment time.

which minimized the Ge pile-up effect. The long duration of fluorine treatment also degraded sensitivity [26, 27]. Hanrath and Korgel reported that [28], in Ge nanowires with p-type behavior, Ge tends to accumulate holes at the nanowire surfaces owing to a trapped negative surface charge. Hence, the bare SiGe nanowire sample should have had a higher conductance compared to other SiGe nanowire samples. This difference resulted from enhanced surface doping; therefore, carrier scattering caused by ionized impurities and surface scattering are major concerns with respect to sensitivity variation [29, 30]. Several recent studies have used fluorine to improve the quality of the interfacial layer at a high- κ /Si interface. The strong Si-F bond (5.73 eV) replaces the weak Si-H bond (3.18 eV) [31, 32] which increases the sensitivity of the nanowire upon plasma fluorination by suppressing the formation of dangling bonds in Ge condensation process.

The effects of the posttreatment were also examined. Figure 5 schematically depicts two SiGe nanowire samples that received different plasma posttreatment after fluorine plasma pretreatment. Figure 5(a) shows a SiGe nanowire that received the N₂ plasma posttreatment, and Figure 5(b) shows a SiGe nanowire that received the NH₃ plasma posttreatment. Figure 6 displays the effect of the posttreatment of SiGe nanowire after fluorine plasma treatment. The sensitivity of the nanowire sample posttreated with N₂ is higher than those of nanowire samples posttreated with NH₃ and those that did not receive treatment. Several studies have reported the successful incorporation of nitrogen into the interfacial layer (IL) and dielectric layer of high- κ material [33–36]. Hence, plasma treatment was effective for incorporating nitrogen on the SiGe nanowire surface. Compared to the NH₃-treated sample, the N₂-treated sample has a higher conductance because it incorporates more N atoms. Weak Si-H bonds are easily broken in the following annealing process at high temperature, which causes dangling bonds to reappear. In

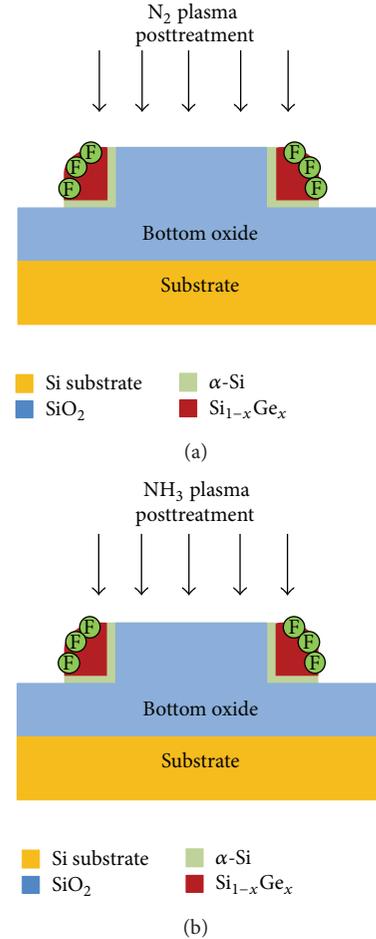


FIGURE 5: The schematics of different post-plasma treatment processes: (a) the N₂ plasma posttreatment and (b) the NH₃ plasma posttreatment.

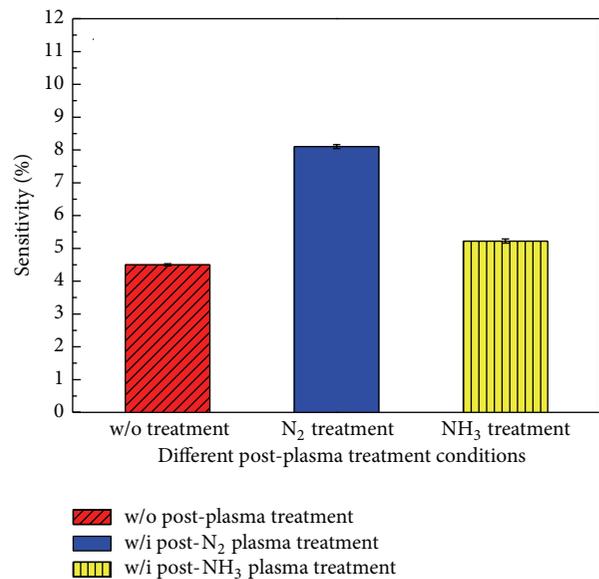


FIGURE 6: The effect of the plasma posttreatment of SiGe nanowire after fluorine plasma treatment.

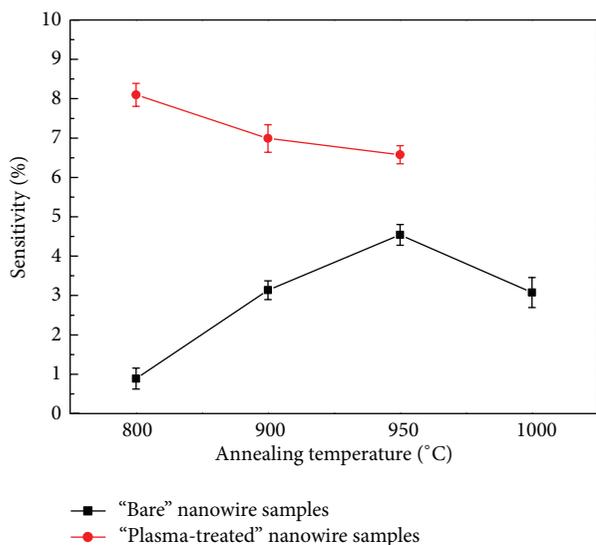


FIGURE 7: The sensitivity of SiGe nanowire samples (w/i and w/o plasma treatment) is in different annealing temperature conditions.

the NH_3 -treated sample, because of these dangling bond traps the conduction carriers are trapped in n-type traps [37–40], reducing its sensitivity. Figure 7 shows the sensitivity of SiGe nanowire samples with and without plasma treatment under different annealing temperatures. The change in the sensitivity of the plasma-treated nanowire is opposite that of the bare nanowire in the temperature region 800~950°C. At 1000°C, the sensitivity of the bare nanowire sample decreases. According to the literature, temperature has an important effect on the SGOI structure [41–43]. It is observed that the raise of the sensitivity of “bare” SiGe nanowire is more obvious at temperature of 950°C due to better concentration and enough energy to recrystallize. A suitable thermal budget can recrystallize the interface between the oxide and SiGe, which reduces the number of dislocations and interior defects. Therefore, sensitivity decreased as annealing temperature increased to 1000°C owing to the diffusion of the Ge, which had originally piled up at the nanowire surface, into the SiGe/SiO₂ interface. The sensitivity was reduced because Ge diffusion decreased the Ge fraction at the surface. In preoxidation treatment, fluorine atoms eliminated most of the defects in the plasma-treated nanowire sample. Furthermore, Ge atoms did not diffuse into the amorphous Si/buried oxide interface. Hence, the average sensitivity of plasma-treated SiGe nanowires exceeded that of bare samples after annealing at various temperatures and increased as annealing temperature decreased. Figure 8 summarizes the sensitivity of the SiGe nanowire after fluorine/nitrogen plasma treatment for different postannealing conditions. The rate of increase in conductance of the plasma-treated samples declined with increasing temperature. It can be attributed to the fact that the SiGe nanowire surface lost fluorine atoms when annealing temperature exceeded 700°C. According to the literature [43, 44], most fluorine is retained at an annealing temperature of 600°C. When annealing temperature reaches 700°C, the retained dose substantially decreases. In

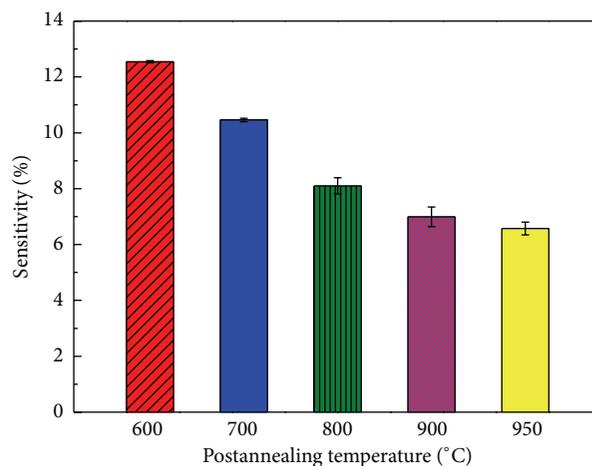


FIGURE 8: The effect of the postannealing of SiGe nanowire after fluorine/nitrogen plasma treatment.

preoxidation treatment, fluorine atoms eliminated most of the defects in the plasma-treated nanowire sample. Hence, the reduced sensitivity of the SiGe nanowire resulting from defects was reproduced by the loss of fluorine atoms in SiGe nanowire surfaces exposed to higher postannealing temperature.

4. Conclusion

This study examined the use of self-passivation and dual plasma methods for increasing the sensitivity of SiGe nanowires in the Ge condensation process. A self-passivation capping oxide layer formed on SiGe nanowire by fluorine enhanced-oxidation reduced the oxidation rate, which suppressed defect formation during the Ge condensation process. Fluorine plasma treatment also efficiently enhanced the sensitivity of SiGe nanowires by increasing the strength of Si–F bonds, which then increased the stability of the interface state on SiGe surface. Accordingly, F atoms can eliminate the dangling bonds in the Ge condensation process in a SiGe nanowire with a high fraction of Ge, which improves its conductance. Plasma posttreatment in N₂ ambient is better than that in NH₃ because the H atoms are more easily dissolved by subsequent annealing at high temperature. Sensitivity can also be improved by adjusting postannealing temperature. A suitable thermal budget not only prevents Ge redistribution, but also retains the highest fluorine dose at the SiGe nanowire surface, which provides a high sensitivity and conductance.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

The authors would like to thank the staff of the National Nano Device Laboratory for their technical help. They also

acknowledge the financial support of the National Science Council (NSC) under Contract no. NSC 98-2221-E-009-174 MY3.

References

- [1] Y. Cui, Q. Wei, H. Park, and C. M. Lieber, "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species," *Science*, vol. 293, no. 5533, pp. 1289–1292, 2001.
- [2] G. Brambilla, F. Xu, and X. Feng, "Fabrication of optical fibre nanowires and their optical and mechanical characterisation," *Electronics Letters*, vol. 42, no. 9, pp. 517–519, 2006.
- [3] Y. K. Mishra, V. S. K. Chakravadhanula, V. Hrkac et al., "Crystal growth behaviour in Au-ZnO nanocomposite under different annealing environments and photoswitchability," *Journal of Applied Physics*, vol. 112, no. 6, Article ID 064308, 2012.
- [4] S. Jebril, H. Kuhlmann, S. Müller et al., "Epitactically interpenetrated high quality ZnO nanostructured junctions on microchips grown by the vapor-liquid-solid method," *Crystal Growth and Design*, vol. 10, no. 7, pp. 2842–2846, 2010.
- [5] D. Gedamu, S. Jebril, A. Schuchardt et al., "Examples for the integration of self-organized nanowires for functional devices by a fracture approach," *Physica Status Solidi B: Basic Research*, vol. 247, no. 10, pp. 2571–2580, 2010.
- [6] Y. K. Mishra, S. Kaps, A. Schuchardt et al., "Fabrication of macroscopically flexible and highly porous 3D semiconductor networks from interpenetrating nanostructures by a simple flame transport approach," *Particle and Particle Systems Characterization*, vol. 30, pp. 775–783, 2013.
- [7] D. Gedamu, I. Paulowicz, S. Kaps et al., "Rapid fabrication technique for interpenetrated ZnO nanotetrapod networks for fast UV sensor," *Advanced Materials*, vol. 26, pp. 1541–1550, 2014.
- [8] F. Patolsky, G. Zheng, O. Hayden, M. Lakadamyali, X. Zhuang, and C. M. Lieber, "Electrical detection of single viruses," *Proceedings of the National Academy of Sciences of the United States of America*, vol. 101, no. 39, pp. 14017–14022, 2004.
- [9] Z. Li, Y. Chen, X. Li, T. I. Kamins, K. Nauka, and R. S. Williams, "Sequence-specific label-free DNA sensors based on silicon nanowires," *Nano Letters*, vol. 4, no. 2, pp. 245–247, 2004.
- [10] Z. Gao, A. Agarwal, A. D. Trigg et al., "Silicon nanowire arrays for label-free detection of DNA," *Analytical Chemistry*, vol. 79, no. 9, pp. 3291–3297, 2007.
- [11] T. Tezuka, N. Sugiyama, and S. Takagi, "Fabrication of strained Si on an ultrathin SiGe-on-insulator virtual substrate with a high-Ge fraction," *Applied Physics Letters*, vol. 79, no. 12, pp. 1798–1800, 2001.
- [12] S. Balakumar, S. Peng, K. M. Hoe et al., "SiGeO layer formation mechanism at the SiGe/oxide interfaces during Ge condensation," *Applied Physics Letters*, vol. 90, no. 3, Article ID 032111, 2007.
- [13] F. K. LeGoues, R. Rosenberg, T. Nguyen, F. Himpsel, and B. S. Meyerson, "Oxidation studies of SiGe," *Journal of Applied Physics*, vol. 65, no. 4, pp. 1724–1728, 1989.
- [14] H. Yang, D. Wang, H. Nakashima et al., "Influence of top surface passivation on bottom-channel hole mobility of ultrathin SiGe and Ge-on-insulator," *Applied Physics Letters*, vol. 93, no. 7, Article ID 072104, 2008.
- [15] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," *Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures*, vol. 18, no. 3, pp. 1785–1791, 2000.
- [16] K. R. Olasupo and M. K. Hatalis, "Leakage current mechanism in sub-micron polysilicon thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 43, no. 8, pp. 1218–1223, 1996.
- [17] M. Morita, S. Aritome, M. Tsukude, and M. Hirose, "A new SiO₂ growth by fluorine-enhanced thermal oxidation," in *Proceedings of the International Electron Devices Meeting (IEDM '84)*, vol. 30, 1984.
- [18] P. Mohanty, I. Yoon, T. Kang et al., "Simple vapor-phase synthesis of single-crystalline Ag nanowires and single-nanowire surface-enhanced raman scattering," *Journal of the American Chemical Society*, vol. 129, no. 31, pp. 9576–9577, 2007.
- [19] C. Li, D. Zhang, S. Han, X. Liu, T. Tang, and C. Zhou, "Diameter-controlled growth of single-crystalline In₂O₃ nanowires and their electronic properties," *Advanced Materials*, vol. 15, no. 2, pp. 143–146, 2003.
- [20] H. H. Solak, D. He, W. Li et al., "Exposure of 38 nm period grating patterns with extreme ultraviolet interferometric lithography," *Applied Physics Letters*, vol. 75, no. 15, pp. 2328–2330, 1999.
- [21] R. Nemetudi, N. J. Curson, N. J. Appleyard, D. A. Ritchie, and G. A. C. Jones, "Modification of a shallow 2DEG by AFM lithography," *Microelectronic Engineering*, vol. 57–58, pp. 967–973, 2001.
- [22] X.-M. Yan, S. Kwon, A. M. Centreras, J. Bokor, and G. A. Somorjai, "Fabrication of large number density platinum nanowire arrays by size reduction lithography and nanoimprint lithography," *Nano Letters*, vol. 5, no. 4, pp. 745–748, 2005.
- [23] Y.-K. Choi, T.-J. King, and C. Hu, "A spacer patterning technology for nanoscale CMOS," *IEEE Transactions on Electron Devices*, vol. 49, no. 3, pp. 436–441, 2002.
- [24] K.-M. Chang, J.-M. Kuo, W.-C. Chao et al., "The Ge enhance the sensitivity for bio-sensor," in *Proceedings of the 2nd IEEE International Nanoelectronics Conference (INEC '08)*, pp. 811–814, March 2008.
- [25] C.-H. Lai, K.-M. Chang, C.-F. Chen et al., "Sensitivity enhancement in SiGe-on-insulator nanowire biosensor fabricated by top surface passivation," *Micro and Nano Letters*, vol. 7, no. 8, pp. 729–732, 2012.
- [26] C. C. Chen, H. C. Lin, C. Y. Chang et al., "Improved plasma charging immunity in ultra-thin gate oxide with fluorine and nitrogen implantation," in *Proceedings of the 5th International Symposium on Plasma Process-Induced Damage*, pp. 121–124, May 2000.
- [27] M. L. Green, E. P. Gusev, R. Degraeve, and E. L. Garfunkel, "Ultrathin (< 4 nm) and Si-O-N gate dielectric layers for silicon microelectronics: understanding the processing, structure, and physical and electrical limits," *Journal of Applied Physics*, vol. 95, p. 2057, 2001.
- [28] T. Hanrath and B. A. Korgel, "Influence of surface states on electron transport through intrinsic Ge nanowires," *Journal of Physical Chemistry B*, vol. 109, no. 12, pp. 5518–5524, 2005.
- [29] H. Yang, D. Wang, H. Nakashima et al., "Influence of top surface passivation on bottom-channel hole mobility of ultrathin SiGe and Ge-on-insulator," *Applied Physics Letters*, vol. 93, no. 7, Article ID 072104, 2008.
- [30] S. Zhang, E. R. Hemesath, D. E. Perea, E. Wijaya, J. L. Lensch-Falk, and L. J. Lauhon, "Relative influence of surface states and bulk impurities on the electrical properties of ge nanowires," *Nano Letters*, vol. 9, no. 9, pp. 3268–3274, 2009.

- [31] P. Chowdhury, A. I. Chou, K. Kumar, C. Lin, and J. C. Lee, "Improvement of ultrathin gate oxide and oxynitride integrity using fluorine implantation technique," *Applied Physics Letters*, vol. 70, no. 1, pp. 37–39, 1997.
- [32] S.-D. Wang, W.-H. Lo, and T.-F. Lei, "CF₄ plasma treatment for fabricating high-performance and reliable solid-phase-crystallized poly-Si TFTs," *Journal of the Electrochemical Society*, vol. 152, no. 9, pp. G703–G706, 2005.
- [33] G. Shang, P. W. Peacock, and J. Robertson, "Stability and band offsets of nitrogenated high-dielectric-constant gate oxides," *Applied Physics Letters*, vol. 84, no. 1, pp. 106–108, 2004.
- [34] K. Tse and J. Robertson, "Defect passivation in HfO₂ gate oxide by fluorine," *Applied Physics Letters*, vol. 89, no. 14, Article ID 142914, 2006.
- [35] C. S. Lai, W. C. Wu, K. M. Fan, J. C. Wang, and S. J. Lin, "Effects of post CF₄ plasma treatment on the HfO₂ thin film," *Japanese Journal of Applied Physics 1: Regular Papers and Short Notes and Review Papers B*, vol. 44, no. 4, pp. 2307–2310, 2005.
- [36] K. M. Chang, B. N. Chen, and S. M. Huang, "The effects of plasma treatment on the thermal stability of HfO₂ thin films," *Applied Surface Science*, vol. 254, no. 19, pp. 6116–6118, 2008.
- [37] M. L. Green, E. P. Gusev, R. Degraeve, and E. L. Garfunkel, "Ultrathin (<4 nm) SiO₂ and Si-O-N gate dielectric layers for silicon microelectronics: understanding the processing, structure, and physical and electrical limits," *Journal of Applied Physics*, vol. 90, no. 5, pp. 2057–2121, 2001.
- [38] T. Hori, *Gate Dielectrics and MOS ULSIs: Principles, Technologies, and Applications*, vol. 34, Springer, New York, NY, USA, 1997.
- [39] L. D. Thanh, P. Balk, L. D. Thanh, and P. Balk, "Elimination and generation of Si-SiO₂ interface traps by low temperature hydrogen annealing," *Journal of The Electrochemical Society*, vol. 135, p. 1797, 1998.
- [40] R. Perera, A. Ikeda, R. Hattori, and Y. Kuroki, "Anomalous leakage current in silicon oxynitride thin films grown by microwave excited nitrogen plasma nitridation," in *Proceedings of the 7th International Conference on Properties and Applications of Dielectric Materials*, pp. 1084–1087, June 2003.
- [41] N. Sugiyama, T. Tezuka, T. Mizuno et al., "Temperature effects on Ge condensation by thermal oxidation of SiGe-on-insulator structures," *Journal of Applied Physics*, vol. 95, no. 8, pp. 4007–4011, 2004.
- [42] S. Balakumar, T. Jun Wei, C. H. Tung et al., "Fabrication of high Ge content SiGe layer on Si by Ge condensation technique," in *Proceedings of the 13th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA '06)*, pp. 301–305, July 2006.
- [43] S. Balakumar, C. S. Ong, C. H. Tung et al., "Effects of annealing and temperature on SGOI fabrication using Ge condensation," in *Proceedings of the 13th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA '06)*, pp. 150–153, July 2006.
- [44] S.-P. Jeng, T.-P. Ma, R. Canteri, M. Anderle, and G. W. Rubloff, "Anomalous diffusion of fluorine in silicon," *Applied Physics Letters*, vol. 61, no. 11, pp. 1310–1312, 1992.



Hindawi

Submit your manuscripts at
<http://www.hindawi.com>

