Research Article

Reconfigurable CPLAG and Modified PFAL Adiabatic Logic Circuits

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Received 30 September 2014; Revised 25 December 2014; Accepted 25 December 2014

Academic Editor: Meiyong Liao

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Previously, authors have proposed CPLAG and MCPLAG circuits extracting benefits of CPL family implemented based upon semiadiabatic logic for low power VLSI circuit design along with gating concept. Also authors have communicated RCPLAG circuits adding another dimension of reconfigurability into CPLAG/MCPLAG circuits. Moving ahead, in this paper, authors have implemented/reconfigured RCPLAG universal Nand/And gate and universal Nor/Or gate for extracting behavior of dynamic positive edge triggered DFF. Authors have also implemented Adder/Subtractor circuit using different techniques. Authors have also reported modification in PFAL semiadiabatic circuit family to further reduce the power dissipation. Functionality of these is verified and found to be satisfactory. Further these are examined rigorously with voltage, C_{load} , temperature, and transistor size variation. Performance of these is examined with these variations with power dissipation, delays, rise, and fall times associated. From the analysis it is found that best operating condition for DFF based upon RCPLAG universal gate can be achieved at supply voltage lower than 3 V which can be used for different transistor size up to 36 μm . Average power dissipation is 0.2 μW at 1 V and 30 μW at 2 V at 100 ff C_{load} 25°C approximately. Average power dissipated by CPLAG Adder/Subtractor is 58 μW . Modified PFAL circuit reduces average power by 9% approximately.

1. Introduction

Previously electronic products released by the companies used to drive the electronic market needs. But with the advances in technologies, competition, and conscious customer behavior now people/clients compel companies to design products according to their desired wish list. The ever increase in demand of more and more functionalities in lesser area is well accomplished with technological upgradation in different VLSI circuit design stages. But with reducing chip area, power dissipation per unit area has increased enormously. Heat dissipation has become comparable to the temperature ranges, unit area in nuclear reactors, turbines, and even sun's surface temperature, in many high end complex integrated circuit chips. Removal of this volcanic heat is essential for correct functionality, which, otherwise,

would damage the chip. Because of different constraints in present technologies and scientific theories, the power equations are reaching their boundaries. This has forced researchers, designers, globally, to conceive some alternative circuit implementation methodologies targeting high performance with low power dissipation. Adoptions of adiabatic logic concept in VLSI circuit design mechanisms have shown lucrative options. Two primary rules need to be taken care of while implementing adiabatic circuits. These rules are as follows.

- (i) Never "Switch On" the transistor when there is potential difference across its two terminals.
- (ii) Never "Turn Off" the switch when a current is flowing through it.

These factors decide the adiabatic and nonadiabatic power loss in the circuit. Adiabatic power loss is inherent energy loss, even after above-stated prerequisites are completely followed. On the other hand nonadiabatic power loss involves some degree of violation in these rules which lead to power loss in access to the adiabatic loss. Depending upon these adiabatic circuits can be broadly classified into full-adiabatic circuits and semi-adiabatic circuits, respectively. Full-adiabatic circuits are ideal cases which are very difficult to comply with [1–6].

The fundamental concept behind adiabatic circuit is to reduce the charge transfer rate leading to reduction in power dissipated by the circuit. Equation (1) shows the power dissipation relationship for adiabatic circuits. It is evident from this that energy can be reduced by slowing down the charge transfer rate. Hence adiabatic circuits are inherently slower in their operating ranges as compared to traditional SCMOS circuits. This proves to be a major drawback for adiabatic circuits in the era of high computing. The usage of CPL based circuit implementation, embedded with adiabatic principles, has been reported in prior art [7, 8]. Authors have also proposed use of CPL based circuit implementation based upon the adiabatic concept [9–11]. The inherent speed advantage in CPL compensates the operating speed tradeoff with the power involved in favor of adiabatic circuits. Authors also proposed the use of gated signal in said CPL adiabatic circuit topologies. The gated signals enable smooth inter-stages and intra-stages integration reducing the efforts involved in meeting the timing constraints involved. In previous work authors have shown good results with integration of said concepts. This is further appreciated with the use of reconfigurability in implementing adiabatic circuits based upon CPL functionality with gated signals:

$$E = \int_0^T R \frac{C^2 V_{DD}^2}{T^2} dt = \frac{RC}{T} C V_{DD}^2. \quad (1)$$

Positive Feedback Adiabatic Logic (PFAL) was introduced by Vetali in 1996 which uses dual rail logic implementation strategy. It involves realization of function (F) and complement-function (F_{bar}) needing prime and unprime inputs simultaneously. It consists of cross-coupled inverter stages maintaining the output terminals. The logic blocks are implemented with NMOS transistors only. Authors have proposed addition of extra transistor in Vetali's PFAL structure trading the area in favor of power diminution.

Section 2 discusses the circuit implementation for DFF, Adder/Subtractor with different techniques. Modified PFAL circuit is also discussed here. Results are discussed in Section 3. Finally the work is concluded in the Conclusion section.

2. Circuit Implementation

A time varying power source is used having 4 phases as depicted in Figure 1, having different circuit operation in these 4 phases. During “Evaluation phase,” the circuit functionality is evaluated depending upon the supplied input

FIGURE 1: Four-phase power clock P_{clk} .

FIGURE 2: Proposed RCPLAG Nand/Nor universal gate.

signals. In “Hold phase,” the computed functional value levels are retained at the output terminals for proper latching in the subsequent stages. The charge stored in the circuit nodes is recovered back during “Recovery phase.” In “Idle phase,” the circuit remains idle and next input signal permutation may be applied into the circuit. The circuit implementation parameters are listed in Table 1.

2.1. RCPLAG Universal Gate Reconfiguration for Dynamic PET D FF. The circuit topology for the RCPLAG Nand/Nor universal gate implementation is shown in Figure 2 [12]. Control signal reconfigures the circuit to work as Nand/And or Nor/Or functionality. The circuit takes both primed and unprimed inputs and evaluates functionality. It produces primed and unprimed output with the help of traditional inverter pair driven by the power clock P_{clk} . The output signal integrity is well maintained with proper levels. This enables the circuit to drive the next stage logic with ease. This RCPLAG circuit can also be reconfigured to implement the functionality of dynamic positive edge triggered D FF. The power source P_{clk} is also used as clock signal required. The PMOS transistor at input latching may be replaced with NMOS transistor with primed signal levels accordingly.

TABLE 1: Simulation parameters.

Simulation parameters			
Technology	Value	Simulation	Value
Channel length	0.180 μm	Power clock	Pulse type with Trise and Tfall
Min. width	0.180 μm	Input signal	Bit type
Max. width	36 microns	Delay calculation	50% points
Vton	0.3932664	Data sequence	8 cycles
TOX	4.10E-09	Power clock time period	40 μs
MOS Gate Capacitance Model:			
capmod = 0			
Conditions:			
Voltage	1 V to 5 V (+0.5 V)		
Temperature	25, 30, 40, 70, 100, 200

FIGURE 3: Simulation waveform for RCPLAG-Nand functionality.

FIGURE 4: Output waveform for RCPLAG-Nor functionality.

This can further optimize the associated area and speed equations. The simulation waveform for Nand, Nor, and DFF functionalities using RCPLAG universal gate implementation

strategy is shown in Figures 3, 4, 5, and 6. The respective power comparison values for the implemented circuits are tabulated in Tables 2, 3, and 4.

TABLE 2: Power utilization for And/Nand.

AND CKT. IMP.	Pavg_Vpuls (W)
PFAL	13.58 μ
ECRL	6.91 μ
RCPLAG	12 n

TABLE 3: Power utilization for Or/Nor.

NOR CKT. IMP.	Pavg_Vpuls (W)
PFAL	13.46 μ
ECRL	7.007 μ
RCPLAG	2.5 μ

TABLE 4: Power utilization for DFF.

AND CKT. IMP.	Pavg_Vpuls (W)
PFAL	74.7 μ
ECRL	59.1 μ
RCPLAG	39.8 μ

TABLE 5: Power utilization for Adder/Subtractor.

ADDER CKT. IMP.	Pavg_Vpuls (W)
CPL	6.11E - 04
CPL_PCLK	2.22E - 04
CPLAG PCLK	5.87E - 05
CPLAG VDD	6.18E - 05

FIGURE 5: Output waveform for DFF @ RCPLAG universal Nand gate.

2.2. Adder/Subtractor Circuit. Addition is a major functionality in system data-path used in various components like multiplication, division filters, and so forth. Adder circuit is implemented with CPL techniques, with four different methodologies, namely, (i) CPL technique [13–15], (ii) CPL Adder circuit with power clock as driver, (iii) CPLAG technique [10], and (iv) CPLAG with constant power supply. These circuits are shown in Figures 7 and 8. The circuits are verified with different input combinations and permutations. Simulation waveform for CPLAG Adder with P_{clk} is shown in Figure 9. The power results are tabulated in Table 5.

FIGURE 6: Output waveform for DFF @ RCPLAG Nor universal gate.

2.3. Modified PFAL Circuit. The circuit diagram for modified PFAL adiabatic circuit is shown in Figure 10. It implements basic Inverter/Buffer functionality. It uses an additional drain gate connected NMOS transistor, in between the source and ground terminal of PFAL cross-coupled inverters. Figure 11 shows simulation result for modified PFAL based inverter.

TABLE 6: Power utilization for PFAL versus modified PFAL.

(W)	Modified PFAL inverter	PFAL inverter	% reduction	Total reduction
Pavg_Vpuls	$1.58E - 11$	$6.60E - 10$	$9.76E + 01$	
Pavg_Vin	$4.59E - 11$	$4.57E - 11$	$-4.44E - 01$	$9.80E + 01$
Pavg_Vinb	$2.29E - 10$	$2.31E - 10$	$8.76E - 01$

FIGURE 7: CPL Adder circuit implementation.

FIGURE 8: CPLAG Adder circuit implementation.

Table 6 tabulates the power comparison for PFAL and modified PFAL inverter circuit implementation.

3. Result Discussion

The average power consumption variation with respect to supply voltage variation for RCPLAG Nand based D FF is shown in Figure 12. As expected the power dissipation with respect to power source P_{clk}/V_{puls} increases with increase in voltage level of the source. For the range of 1V to 2.5V the variation can be linearly approximated. For voltage levels above 2.5V the rate of increment in the power dissipation is varying exponentially. Hence it can be inferred that, for best case power equations, the circuit should be operated with voltage levels less than 2.5V. The power dissipation at 3V is 0.2mW approximately. For extreme cases one may also consider operating 3V supply.

The input signal strength required for driving the circuit and evaluating its functionality varies linearly approximately with respect to voltage level as shown in Figure 13. For

a supply voltage range up to 3V the power required is less than 3nW approximately. Hence a small rating input source for V_b and V_a would work fine to actuate and evaluate the circuit functionality. For signal V_a the signal power requirement is around 10pW as shown in Figure 14, for 2V voltage supply. On the other hand, the input signal power requirement for V_{bb} varies parabolically with respect to voltage. At its base lines up to 3V power voltage supply the variation may be interpolated linearly but beyond this the rate of increase in power with respect to V_{bb} increases sharply with voltage levels, but still this rate is less as compared to signals V_a, V_b .

Circuit is operated for a maximum load of 1nF with average power dissipation of 0.1mW at 2V trapezoidal power supply. The average power dissipation with respect to C_{load} is shown in Figure 15. Till C_{load} of 0.1nf the power dissipation from the circuit is constant, approximately equal to 40μW. As the C_{load} is increased beyond 0.1nf the circuit dissipates comparatively very large power, because of the energy required to charge the large capacitance which is

FIGURE 9: Output waveform for CPLAG Adder with P_{clk} .

FIGURE 10: Modified PFAL circuit implementation @ inverter.

directly proportional to incremental power dissipation. The quantum of effort required to charge the C_{load} up to 0.1 nF is more or less the same, dissipating approximately same power from the power source. The average power variation with power clock source, for DFF using RCPLAG Nand with respect to C_{load} , is shown in Figure 16.

FIGURE 11: Output waveform for modified PFAL inverter gate.

The signal strength required for input signal is quite independent with the variation of C_{load} as depicted in Figure 17. The variant capacitive loading has no effect on the signal which is approximately 5.8 nW and 1.44 nW for V_{bb} and V_b signal approximately.

With rise in temperature the input resistance for input terminal V_{bb} decreases with constant slope proportional to

FIGURE 12: V_{plus} P_{avg} variation for DFF @ RCPLAG Nand with respect to supplied voltage level.

FIGURE 13: Avg. input power required for V_b for DFF @RCPLAG Nand.

FIGURE 14: Avg. input power required for V_a for DFF @RCPLAG Nand.

temperature coefficient concerned as shown in Figure 18. The input signal V_b has approximately constant input resistance, with very small rate of decrease, with respect to temperature increase.

Similarly as shown in Figure 19 the output resistance decreases with increase in temperature. This is because of more availability of charge carriers at high temperature giving rise in current associated and hence reduction in resistance associated. At 25°C the Output resistance is $3.5 \times 10^9 \Omega$ which reduces to $2.5 \times 10^8 \Omega$ approximately at

FIGURE 15: Avg. input power required for V_{bb} for DFF @RCPLAG Nand.

FIGURE 16: V_{plus} P_{avg} variation for DFF @RCPLAG Nand with respect to C_{load} .

FIGURE 17: Signal power requirement with respect to C_{load} .

100°C . The average power dissipation reduces linearly with a constant slope with temperature variation as shown in Figure 20. The power dissipation varies from 45 nW to 30 nW from room temperature 25°C to 100°C .

The average power dissipation by D FF circuit using Nor RCPLAG universal gate is shown in Figure 21 with respect to C_{load} . As with Nand based implementation the average power is constant approximately up to a loading of 0.1 nF

FIGURE 18: Input resistance variation wrt temperature.

FIGURE 19: Output resistance variation wrt temperature.

and increases greatly for further increase in loading. Also the average power required for input signal for successfully actuating the circuit is independent of loading as shown in Figure 22.

The PDP distribution for 20 different transistor sizes is shown in Figure 23. The transistor size is varied from $1.8 \mu\text{m}$ to $36 \mu\text{m}$. This PDP is examined for 9 different voltage levels as shown. Up to a voltage level of 3 V and $12.6 \mu\text{m}$ transistor size, PDP shows a linear behavior. For higher transistor size the PDP variation increases parabolically with supply voltage. Similarly for high voltage the rate of increase in PDP with respect to transistor size varies parabolically, but the quantum rate is comparatively less. For the permutation of high transistor size and voltage level the PDP factor increases rapidly indicating inefficient functional operation for the circuit. It can be inferred that for a voltage level of 3 V

FIGURE 20: V_{puls} avg. power consumed with respect to temperature variation. FIGURE 21: Avg. power dissipation for DFF @RCPLAG Nor gate with respect to C_{load} .

the circuit can be operated with constant PDP with different transistor sizes till $36 \mu\text{m}$.

Hence with the voltage range of up to 3 V with $23.4 \mu\text{m}$ transistor size the circuit can be operated in best PDP scenario. The average power distribution with voltage and transistor size is shown in Figure 24. Normalized power drawn and feedback to the source are shown in Figure 25. Up to 2.5 V voltage supply the power feedback shown negative axes are approximately constant. As circuit is based upon CPL family, a good amount of circuit transistors is driven by the input signals as shown in positive axes in the figure. Majority of the power drawn from the source is feedback. The variation in the power drawn and feedback is quite similar for different transistor sizes as shown in Figure 25. The cone point behavior is shown whose base point reduces a small

FIGURE 22: Input signal power requirement with respect to C_{load} .

FIGURE 23: PDP variation with respect to voltage and transistor size.

value with increase in transistor size retaining the behavior variation.

4. Conclusion

In this paper authors have implemented dynamic positive edge triggered D FF configured from reconfigurable complementary pass transistor adiabatic logic gated (RCPLAG) Nand/And and Nor/or universal gates. Authors have also implemented Adder/Subtractor circuit with 4 different techniques. Authors have also reported modification in PFAL

FIGURE 24: Avg. power distribution with respect to voltage and transistor size.

FIGURE 25: Normalized power drawn and feedback to power source.

adiabatic techniques for further optimizing of the power equations. These circuits implemented are functionally verified and found to work to a good level of satisfaction. These circuits are examined for power dissipation, timings, and

PDP for 20 different transistor sizes and 9 different voltage levels and 9 different temperature values.

From the analysis it is found that the best operating condition for the D FF based upon RCPLAG universal gate can be achieved at supply voltage lower than 3 V which can be used for different transistor size up to 36 μm . The average power dissipation is 0.2 μW at 1 V and 30 μW at 2 V at 100 ff C_{load} 25°C approximately. For C_{load} less than 0.1 nf the average power dissipation remains constant. Also smaller strength input signal can successfully actuate the circuit and evaluate its functionality. The input resistance is independent of the temperature variation. The circuits work fine for a wider range of temperature. Majority of the power drawn from the power source is feedback after circuit evaluation in the Recovery phase of power clock to the voltage source. This assists in reutilization of the energy and helps in reducing the amount of power drawn from the source. The average power dissipated by CPLAG Adder/Subtractor is the least as compared to other implementations, which is 58 μW at 2 V trapezoidal power source. The modified PFAL circuit successfully reduces the average power by 9% approximately as compared to PFAL circuit.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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