Research Article

Design of a Novel W-Sinker RF LDMOS

Xiangming Xu,^{1,2} Han Yu,² Jingfeng Huang,² Chun Wang,² Wei Ji,² Zhengliang Zhou,² Ying Cai,² Yong Wang,¹ Pingliang Li,^{1,2} Peng-Fei Wang,¹ and David Wei Zhang¹

¹State Key Laboratory of ASIC and System, School of Microelectronics, Fudan University, Shanghai 200433, China

²Huahong Grace Semiconductor Manufacturing Corporation, Shanghai 201206, China

Correspondence should be addressed to David Wei Zhang; dwzhang@fudan.edu.cn

Received 13 November 2014; Accepted 26 November 2014

Academic Editor: Rui Zhang

Copyright © 2015 Xiangming Xu et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

A novel RF LDMOS device structure and corresponding manufacturing process are presented in this paper. Deep trench W-sinker (tungsten sinker) is employed in this technology to replace the traditional heavily doped diffusion sinker which can shrink chip size of the LDMOS transistor by more than 30% and improve power density. Furthermore, the W-sinker structure reduces the parasitic resistance and inductance and improves thermal conductivity of the device as well. Combined with the adoption of the techniques, like grounded shield, step gate oxide, LDD optimization, and so forth, an advanced technology for RF LDMOS based on conventional 0.35 μm CMOS technology is well established. An $F + A$ power amplifier product with frequency range of 1.8–2.1 GHz is developed for the application of 4G LTE base station and industry leading performance is achieved. The qualification results show that the device reliability and ruggedness can also meet requirement of the application.

1. Introduction

Laterally diffused metal-oxide-semiconductor (LDMOS) technologies have been the first choice in wireless base station applications for nearly the last 20 years due to their high gain, high efficiency, superior linearity [1, 2], and being easy to integrate with CMOS technology [3, 4]. RFLDMOS provides the most cost-effective solution for the base station system applications because it can be fabricated with low-cost and mature Si process compared with GaAs and GaN technology. Moreover, LDMOS transistors can be used at high frequencies to achieve a high continuous peak power [5, 6]. Because of these merits, RF LDMOS can also be used in a wide range of applications requiring radio frequency power amplifier like broadcast, pulsed radar, ISM (industrial, scientific, and medical) applications, and so forth [7–9].

In this study, a novel RF LDMOS device structure and corresponding manufacturing process are proposed and developed based on conventional 0.35 μm CMOS technology, and deep trench W-sinker (tungsten sinker) is employed in this technology to replace the traditional heavily doped diffusion sinker to realize an effective connection from source to the back side of the substrate, which reduces chip size and

also improves power density of the device greatly. Combined with the adoption of the techniques like G-shield (grounded shield), step gate oxide, LDD optimization, and so forth, an advanced technology for RF LDMOS is well established. An $F + A$ power amplifier product with frequency range of 1.8–2.1 GHz is developed for the application of 4G LTE base station. Both DC and RF performance of the device are evaluated and the results show that industry leading performance is achieved. Besides, the qualification results show the device reliability and ruggedness can also meet requirement of the application.

This paper is organized as follows. Section 2 describes the design of the proposed W-sinker RF LDMOS device structure and corresponding manufacturing process. In Section 3, device measurement results are presented including DC, RF, and ruggedness. In Section 4, conclusion is given.

2. The Proposed Device Structure and Process Features

The cross-sectional view of the proposed device, shown in Figure 1, is based on conventional 0.35 μm CMOS technology, which consists of drain, source, gate, N-LDD (lightly doped

FIGURE 1: The proposed W-sinker RF LDMOS device structure.

FIGURE 2: Cross-sectional SEM view of fabricated step gate oxide structure.

drain extension), G-shield (grounded shield), and sinker. A lightly doped epitaxial layer with certain thickness is grown on the highly doped Si substrate to meet the requirement of breakdown voltage for the transistor. A tungsten G-shield plate formed between gate and drain not only reduces the feedback capacitance C_{gd} but also improves the reliability of the device by reducing the peak electric field at the gate-edge and the drift region. By optimizing the dopant and length of the N-LDD, high breakdown voltage, low on-resistance, and low HCI (hot carrier injection) could be realized. Gate is formed by Ti-salicided polysilicon with sheet resistance lower than 1.5 ohm, which could ensure power swing under high frequency and low power loss of the large power device composed of multifinger; hence both efficiency and power density could be improved. The back-end which consists of three metal layers and total 10 μm thick interlayer dielectric helps to reduce the output capacitance, and 3 μm thick top metal further makes the device low parasitic metal resistance, good electromigration (EM) reliability. Step gate oxide structure is adopted as shown in Figure 2, and the thermal gate oxide is thin at the source side and is tapered to a thicker oxide at the drain side, which not only reduces input capacitance C_{iss} , output capacitance C_{oss} , and feedback capacitance C_{gd} , but also improves power gain and reliability of the device [10]. Furthermore, self-align channel is formed by the lateral diffusion of boron ions which is implanted self-aligned to the gate, and extremely short and uniform channel can be achieved

FIGURE 3: Cross-sectional SEM view of the fabricated RF LDMOS.

even without high resolution photolithograph process and thus also enhances the gain and reliability of device.

Many techniques have been used to improve power density of RF LDMOS device. For example, RESURF (reduced surface field) method and triple G-shield have been adopted in [10]. In this study, a novel W-sinker (tungsten sinker) is employed in the RF LDMOS device to replace the traditional heavily doped diffusion sinker to realize ultralow resistance connection from source to the back side of the substrate; the W-sinker is formed by deep trenching to the P+ substrate and filling it with chemical vapor deposited tungsten, and then the trench is planarized by CMP (chemical mechanical polishing). Compared with the conventional diffusion sinker, by adopting W-sinker, the chip size of RF LDMOS device can be reduced by more than 30% and power density of the device can also be greatly improved. Although trenched sinker LDMOSFET (TS-LDMOS) structure has been proposed in [11] in which the trench is filled with highly doped polysilicon, the W-sinker proposed in this study still has many advantages over the trenched poly sinker. Firstly, the resistivity of tungsten material is normally 2 orders lower than that of polysilicon even if it is heavily doped. For example, at room temperature (20°C), the resistivity of tungsten is about 5.48×10^{-6} ohm-cm while the resistivity of heavily doped silicon is about 1.17×10^{-3} ohm-cm under boron dosage of $1 \times 10^{20} \text{ cm}^{-3}$. Secondly, the trench filling capability of tungsten is better than polysilicon; in particular, it is shown to be more beneficial when it comes to high aspect ratio of the trench. For a RF LDMOS device of 50 V operating voltage, the EPI thickness reaches around 9-10 μm , the trench depth is required to be even higher, and W-sinker is more adoptable. Thirdly, polysilicon is apt to yield stress on the wafer compared with tungsten due to different material properties; in the followed up high temperature processes, drastic stress changes caused by poly recrystallization may lead to dislocation, device leakage, and reliability failure of the power device.

The cross-sectional SEM view of the fabricated W-sinker RF LDMOS is shown in Figure 3, where the W-sinker has depth of 10 μm and width of 1 μm , respectively.

FIGURE 4: DC characteristics of W-sinker RF LDMOS device ($W = 80 \mu\text{m}$).

3. Test Results of the Fabricated RF LDMOS Device

Based on the W-sinker RF LDMOS device structure and technology described in Section 2, a 30 V/100-Watt $F + A$ power amplifier (PA) product for the application of 4G LTE base station is developed; DC characteristics of a single transistor device (width = $80 \mu\text{m}$), RF performance, and ruggedness of the $F + A$ power amplifier product are evaluated, and the results are shown as follows.

3.1. DC Characteristics. Instead of the $F + A$ PA product, DC characteristics of the single transistor device (width = $80 \mu\text{m}$) are measured due to the ability of Agilent 1500A tester. Test results are shown in Figure 4(a) ID-VG curve, Figure 4(b) ID-VD curve, and Figure 4(c) breakdown curve, and the device

achieves a breakdown voltage of 67 V, threshold voltage of 1.2 V, and saturation current (I_{dsat}) of $204 \mu\text{A}/\mu\text{m}$ with gate and drain biased on 5 V and 28 V, respectively.

Furthermore, the degradation experiments of quiescent current (I_{dq}) are conducted to investigate HCI concern. During the test, the RF LDMOS device is stressed under $V_d = 28 \text{ V}$ and $I_d = 5 \mu\text{A}/\mu\text{m}$ which is a typical DC bias for class AB amplifier of base station application. The measurement results of I_{dq} degradation are shown in Figure 4(d), and I_{dq} degradation is concluded to be less than 5% in 20 years, which meets the requirements of various applications of the industry.

3.2. RF Performance. The RF performance of the $F + A$ PA product is characterized by focus load pull measurement system (Figure 5(a): the picture of the system; Figure 5(b): its

FIGURE 5: (a) Focus load pull system and (b) its schematic diagram.

FIGURE 6: Output power, gain, and PAE versus input power for the 100-Watt $F + A$ product.

schematic diagram). The device is stressed under $V_d = 28$ V and $I_d = 5$ mA/mm which is the same as actual operating conditions of base station application, and the RF input is pulsed CW (continuous wave) signal with 40μ s pulse width and 4% duty cycle. Test results are shown in Table 1; the RF linear gain is 21 dB, the PAE (power added efficiency) is near 68% with the frequency of 1880 MHz at F band, output power at 3 dB gain compression point (P_{3dB}) reaches 50.2 dBm, and power density is over 1.16 W/mm. And the performance only shows a slight drop with the frequency of 2025 MHz at A band. The detailed output power, gain, and PAE versus input power for 100-Watt $F + A$ product are shown in Figure 6. Industry advanced performance is achieved [10].

TABLE 1: RF performance of the W-sinker RF LDMOS product.

(a)					
Frequency	Zsource				
			Real	Imag.	
1880 MHz			11.604	9.494	
2025 MHz			2.354	−3.706	
(b)					
Frequency	Zpwr				
	Real	Imag.	Gain (dB)	PAE (%)	P3dB (dBm)
1880 MHz	1.6	−3.001	18.66	57.8	50.22
2025 MHz	1.447	−3.22	18.42	58.3	50.03
(c)					
Frequency	Zeff				
	Real	Imag.	Gain (dB)	PAE (%)	P3dB (dBm)
1880 MHz	1.081	−1.971	21.3	67.7	48.79
2025 MHz	0.813	−2.325	20.81	65.1	48.11

FIGURE 7: TLP result of the 100-Watt $F + A$ PA product.

3.3. Ruggedness. The device ruggedness is one of the important intrinsic reliability factors for RF LDMOS as challenging electrical and thermal environments are presented for the device in RF power applications. The most common ruggedness failure mechanism for LDMOS devices is the catastrophic failure resulting from the snapback of a parasitic bipolar junction transistor of the device [12]. TLP (transmission line pulse) measurement can be used to characterize the device's breakdown behavior and evaluate the ruggedness performance. Due to the ability of TLP measurement tool Barth 4002, test is conducted on the single transistor device (width = 80 μ m). The result is shown in Figure 7. I_{t2} (secondary breakdown current) reached 400 mA/mm which indicates that the device has very good ruggedness.

For the high power PA devices, the ruggedness can be measured by the VSWR (voltage standing wave ratio) load mismatch test using the same system as RF test (Figure 5). Test results show that the $F + A$ PA product passes P10dB conditions at the drain voltage of 32 V with the VSWR 20:1 load terminal mismatch. In 20:1 VSWR output mismatch, 82% of the output power is reflected from the load back to the devices and only 18% is transmitted to the load. The device shows very good device ruggedness.

4. Conclusion

A novel W-sinker RF LDMOS device structure is proposed and corresponding manufacturing process is developed based on conventional 0.35 μm CMOS technology, and deep trench W-sinker is used to realize effective connection from source to the back side of the substrate. Compared to the conventional diffusion sinker, chip size can be reduced and power density of the device can be improved greatly. And the W-sinker proposed in this study also has advantages over the trenched poly sinker proposed by other works regarding the aspects of resistance, process adaptability, and stress. Combined with the adoption of the techniques like G-shield, step gate oxide, LDD optimization, and so forth, an advanced technology for RF LDMOS is well established. An $F + A$ power amplifier product is developed for the application of 4G LTE base station on this technology. Test results show that BV of 67 V and Idsat of 204 mA/mm are achieved. RF linear gain is 21 dB and the PAE is near 68% with the frequency of 1880 MHz at F band, output power at 3 dB gain compression point (P3dB) reaches 50.2 dBm, and power density is over 1.16 W/mm. All the parameters advance in the industry currently. Besides, the qualification results show the device reliability and ruggedness can also meet requirement of the application.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

The authors would like to gratefully acknowledge the contributions of many Huahong Grace colleagues for process and module development, device simulation and characterization, and helpful discussions. The authors would also like to give great thanks to Dajie Zeng and Nan Liu from Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, for supporting RF measurement and ruggedness evaluation. This study is financially supported by the Chinese National Key Project (no. 2012ZX02502).

References

- [1] A. Wood, C. Dragon, and W. Burger, "High performance silicon LDMOS technology for 2GHz RF power amplifier applications," in *Proceedings of the IEEE International Electron Devices Meeting*, pp. 87–90, December 1996.
- [2] H. F. F. Jos, "Novel LDMOS structure for 2 GHz high power basestation application," in *Proceedings of the 28th European Microwave Conference*, pp. 739–744, 1998.
- [3] H. Brech, W. Brakensiek, D. Burdeaux et al., "Record efficiency and gain at 2.1 GHz of high power RF transistors for cellular and 3G base stations," in *Proceedings of the IEEE International Electron Devices Meeting—Technical Digest*, pp. 359–362, December 2003.
- [4] F. van Rijs and S. J. C. H. Theeuwen, "Efficiency improvement of LDMOS transistors for base stations: towards the theoretical limit," in *Proceedings of the International Electron Devices Meeting (IEDM '06)*, pp. 1–4, San Francisco, Calif, USA, December 2006.
- [5] F. van Rijs, "Status and trends of silicon LDMOS base station PA technologies to go beyond 2.5 GHz applications," in *Proceedings of the IEEE Radio and Wireless Symposium (RWS '08)*, pp. 69–72, Orlando, Fla, USA, January 2008.
- [6] S. J. C. H. Theeuwen and H. Mollee, "S-band radar LDMOS transistors," in *Proceedings of the 4th European Microwave Integrated Circuit Conference (EuMIC '09)*, pp. 53–56, 2009.
- [7] R. Pengelly, D. Vye, L. Pelletier et al., "The new power brokers: high voltage RF devices," *Microwave Journal*, vol. 52, no. 6, pp. 22–40, 2009.
- [8] K. Werner and S. Theeuwen, "RF driven plasma lighting—the next revolution in light sources are powered by solid state RF technology," *Microwave Journal*, vol. 12, pp. 68–74, 2010.
- [9] P. H. Aaen, *Modeling and Characterization of RF and Microwave Power FETs*, chapter 1, 2007.
- [10] S. J. C. H. Theeuwen and J. H. Qureshi, "LDMOS technology for RF power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 6, pp. 1755–1763, 2012.
- [11] C. S. Kim, J.-W. Park, and H. K. Yu, *Trenched Sinker LDMOSFET (TS-LDMOS) Structure for High Power Amplifier Application above 2 GHz*, IEDM 01-887, IEEE, 2001.
- [12] D. Burdeaux and W. Burger, "Intrinsic Reliability of RF Power LDMOS FETs," IRPS11-435~443, 2011.