Research Article

Improving Breakdown Voltage for a Novel SOI LDMOS with a Lateral Variable Doping Profile on the Top Interface of the Buried Oxide Layer

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In order to achieve a high breakdown voltage (BV) for the SOI (Silicon-On-Insulator) power device in high voltage ICs, a novel high voltage n-channel lateral double-diffused MOS (LDMOS) with a lateral variable interface doping profile (LVID) placed at the interface between the SOI layer and the buried-oxide (BOX) layer (LVID SOI) is researched. Its breakdown mechanism is investigated theoretically, and its structure parameters are optimized and analyzed by 2D simulation software MEDICI. In the high voltage blocking state, the high concentration ionized donors in the depleted LVID make the surface electric field of SOI layer (E_s) more uniform and enhance the electric field of BOX layer (E_t), which can prevent the lateral premature breakdown and result in a higher BV. Compared with the conventional uniformly doped (UD) SOI LDMOS, E_t of the optimized LVID SOI LDMOS is enhanced by 79% from 119 V/ μm to 213 V/ μm , and BV is increased by 33.4% from 169 V to 227 V. Simulations indicate that the method of LVID profile can significantly improve breakdown voltage for the SOI LDMOS.

1. Introduction

SOI technology has been widely used in high voltage ICs due to its advantages such as superior isolation, high speed, and low loss [1]. However, SOI power devices suffer from a low vertical BV. A feasible way to increase the BV is to enhance the dielectric layer field (ENDIF), and several new structures have been proposed by ENDIF, in which introducing interface charges is effective and attractive [2]. The variable doping profile is a method of introducing interface charges which was firstly proposed to avoid high voltage breakdown for planar junctions in 1985 [3]. The approach of designing and implementing the linear doping profile on thin SOI for lateral high voltage devices was presented in 1995 [4]. A submicron thin film SOI LDMOS with the variable doping profile and numerical modeling of linear doping profiles were proposed in 1996 and 1999, respectively [5, 6]. After 2000,

several new SOI devices structures with linear doping profile were proposed [7–11].

In this paper, a novel SOI device with a LVID profile (LVID SOI LDMOS) is designed. The doping profile of drift region is a combination of linear variable doping and uniform doping in vertical dimension, which is different from the above-mentioned structures. The influence of the parameters on BV and the specific on-resistance ($R_{\text{on,sp}}$) is presented. The simulated results indicate that the method of LVID profile can significantly improve BV compared with UD profile.

2. Structure and Mechanism

The cross-section of LVID SOI LDMOS is illustrated in Figure 1(a). The LVID profile is placed at the interface between the SOI layer and the BOX layer, the thickness of which is expressed as t_{LVID} . The lateral doping concentration

FIGURE 1: LVID SOI LDMOS. (a) Schematic cross-section; (b) the doping concentration of the LVID profile.

of the LVID profile is shown in Figure 1(b), which can be expressed as

$$C(x) = Gx + C_0, \quad (1)$$

where x is the distance away from source, G is the linear graded coefficient which determines the slope of the profile, $C(x)$ is the doping concentration of LVID profile, and C_0 is the doping concentration at $x = 0$, $y = t_s$. Here, t_s is the thickness of the SOI layer and N_d is the doping concentration of uniform doping section.

According to Figure 1(b) and (1),

$$G = \frac{C_{L_d} - C_0}{L_d}, \quad (2)$$

where C_{L_d} is the doping concentration at $x = L_d$, $y = t_s$. Since C_0 is much less than C_{L_d} , it is ignored in the above expression. G is proportional to C_{L_d} .

The device mechanism at breakdown can be explained as follows. When a high positive voltage V_d is applied to the drain while the source, gate, and substrate are grounded, the LVID profile will be depleted and high concentration ionized donors are accumulated at the top interface of BOX layer just as shown in Figure 2, and due to the LVID profile, the concentration of ionized donors in LVID profile will linearly increase from source to drain. According to the theory of ENDIE, the interface charges can not only increase the electric field in BOX layer but modulate the surface electric field of drift region [2]. The modulation effect is that the surface electric field peaks at source and drain are decreased and the surface electric field in the middle drift region is improved. Thus LVID profile should prevent the lateral premature breakdown. At the same time, because the vertical breakdown voltage is sustained by the BOX layer, the improved E_I can significantly enhance the vertical BV. The influences of the LVID profile on the breakdown performance of SOI LDMOS transistor will be analyzed and compared with UD SOI LDMOS in Section 3. The parameters used in the simulations are detailed in Table 1.

FIGURE 2: Device mechanism of the LVID SOI LDMOS.

TABLE 1: Device parameters used in the simulations.

Parameter	Value
Thickness of the SOI layer, t_s (μm)	2
Thickness of the buried oxide layer, t_I (μm)	1
Thickness of P-substrate, t_{sub} (μm)	2
Thickness of the LVID profile, t_{lvid} (μm)	0.1–2
Length of n-type drift region, L_d (μm)	10
Length of the p-well, L_{pw} (μm)	5
Concentration of P-substrate, N_{sub} (cm ⁻³)	8×10^{14}
Concentration of p-well, N_{pw} (cm ⁻³)	3×10^{16}
Concentration of uniform doping in drift region, N_d (cm ⁻³)	Optimized
The slope of the LVID profile, G (cm ⁻⁴)	Optimized

3. Results and Discussion

Figure 3 is the electrical performances at breakdown of the two devices whose structure parameters are optimized with $t_{lvid} = 0.1 \mu\text{m}$. UD SOI LDMOS reaches the maximum BV at $N_d = 9 \times 10^{15} \text{ cm}^{-3}$, and LVID SOI LDMOS reaches the maximum BV at $N_d = 4 \times 10^{15} \text{ cm}^{-3}$, $G = 4.48 \times 10^{20} \text{ cm}^{-4}$.

FIGURE 3: Distributions of equipotential contours, electric fields, and interface charges at breakdown for the UD and LVID SOI LDMOS. (a) Equipotential contours (10 V/contour) distributions for the UD SOI LDMOS with the optimized $N_d = 9 \times 10^{15} \text{ cm}^{-3}$; (b) equipotential contours (10 V/contour) distributions for the LVID SOI LDMOS with the optimized $N_d = 4 \times 10^{15} \text{ cm}^{-3}$, $G = 4.48 \times 10^{20} \text{ cm}^{-4}$. (c) The comparison of the lateral surface electric field distributions at breakdown. (d) Interface charges concentration distributions of LVID profile and UD profile at breakdown.

Figures 3(a) and 3(b) are the equipotential contours distributions at breakdown for the two devices. It can be seen that, compared with the UD SOI LDMOS shown in Figure 3(a), the equipotential contours of the LVID SOI LDMOS shown in Figure 3(b) are more uniform and denser. The surface electric field distributions at breakdown for the two devices are shown in Figure 3(c). It is clear that the E_s of LVID SOI LDMOS is optimized and more uniform, and the E_s at $x = L_d/2$ is improved by 111% compared with UD SOI LDMOS which means an increase of lateral BV, and the shadow part is just the improvement value of lateral BV. The optimization of E_s and improvement of lateral BV are the results of the high concentration ionized donors distributed in the LVID profile as shown in Figure 3(d), the inset of which is the lower ionized donors concentration distribution of UD profile.

The vertical electric fields and potentials distributions for the UD and LVID SOI LDMOS at breakdown along line MN (shown in Figure 1(a)) are shown in Figure 4. It is clear that,

for the LVID SOI LDMOS, E_T is improved by 79% from $119 \text{ V}/\mu\text{m}$ to $213 \text{ V}/\mu\text{m}$, and BV is improved by 34.3% from 169 V to 227 V , which are both the results of the introduced interface charges in the LVID profile.

Figure 5 shows the dependences of BV on the G for different N_d . Simulation results indicate that there is always an optimum concentration slope for different N_d to make BV reach the maximum value and the optimum G decreases with the increase of N_d . The reason is that the total doping concentration of drift region needed for the device breakdown at the maximum BV is certain by RESURF (Reduced Surface Field) theory [12]. When N_d increases, the doping concentration of LVID profile needed for the maximum BV will decrease, which is proportional to G as defined in (2). So G is inversely proportional to N_d . Figure 6 shows the dependences of BV on N_d for different G . Results indicate that there is also always an optimum N_d for different G to make BV reach the maximum value and the optimum N_d decreases

FIGURE 4: Vertical electric fields and potentials distributions at breakdown along line MN for UD SOI LDMOS ($N_d = 9 \times 10^{15} \text{ cm}^{-3}$) and LVID SOI LDMOS ($N_d = 4 \times 10^{15} \text{ cm}^{-3}$, $G = 4.48 \times 10^{20} \text{ cm}^{-4}$).

FIGURE 5: Dependences of BV on G with $t_{\text{lvid}} = 0.1 \mu\text{m}$.

with the increase of G . The results accord with the inverse relationship of G and N_d .

Figure 7 shows the influence of t_{lvid} on BV. It can be seen that G is inversely proportional to t_{lvid} , which means the optimum G decreases with the increase of t_{lvid} . This is also because the total doping concentration needed for the maximum BV is certain. Simulations show that when t_{lvid} is less than $0.5 \mu\text{m}$, BV can reach maximum values above 210 V for different t_{lvid} and attains 227 V at $t_{\text{lvid}} = 0.1 \mu\text{m}$. When t_{lvid} is greater than $0.6 \mu\text{m}$, BV falls quickly and drops to 184 V at $t_{\text{lvid}} = 1 \mu\text{m}$. BV remains in about 180 V within $1 \mu\text{m}$ to $2 \mu\text{m}$. It can be concluded that t_{lvid} has a great influence on BV within $0.5 \mu\text{m}$ and has a little influence on BV when t_{lvid} is greater than $1 \mu\text{m}$.

FIGURE 6: Dependences of BV on N_d with $t_{\text{lvid}} = 0.1 \mu\text{m}$.

FIGURE 7: The influence of t_{lvid} on BV.

Figure 8 shows the influences of t_{lvid} on BV and $R_{\text{on,sp}}$. The results are obtained in the case of the optimized devices for the highest BV for different t_{lvid} . It can be seen that BV and $R_{\text{on,sp}}$ both decrease with the increase of t_{lvid} . Figure of Merit (FOM) is a value calculated by $\text{BV}^2 / R_{\text{on,sp}}$ which balances the trade-off between BV and $R_{\text{on,sp}}$ [13]. The optimized FOM is 6.22 MW/cm^2 at $t_{\text{lvid}} = 0.1 \mu\text{m}$ when gate voltage is 15 V. $R_{\text{on,sp}}$ is calculated by $L_d \times V_{\text{ds}} / I_{\text{ds}}$ at the linear region of I - V curve and is $8.28 \text{ m}\Omega\cdot\text{cm}^2$ at $t_{\text{lvid}} = 0.1 \mu\text{m}$.

Figure 9 shows the major fabrication steps for an LVID SOI wafer: (a) implanting arsenic to form the LVID profile region on the bottom of the SOI layer; (b) thermally growing to form the buried oxide layer on the p-type substrate; (c) bonding the SOI layer and the substrate layer; (d) annealing

FIGURE 8: The influences of t_{lvid} on BV and $R_{on,sp}$.

FIGURE 9: Major fabrication steps of LVID profile.

the wafer and then thinning and polishing the wafer. The LVID profile can be achieved by using the lateral variation doping technique [4, 9]. It can be seen that only an additional process of arsenic implanting before bonding is needed to form LVID SOI wafer. Other fabrication processes are fully compatible with conventional CMOS/SOI technology.

4. Conclusion

The LVID SOI high voltage device structure is proposed. The proposed structure increases greatly the BV because of the modulation effect of interface charges on the electric fields in the BOX layer and drift region. Compared with UD SOI LDMOS, E_f and BV of LVID SOI LDMOS are improved by 79% and 33.4%, respectively, which proves that the LVID profile is an effective method to improve the BV for SOI high voltage devices.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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