Research Article

Strain and Dimension Effects on the Threshold Voltage of Nanoscale Fully Depleted Strained-SOI TFETs

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Received 13 April 2015; Revised 8 June 2015; Accepted 16 June 2015

Academic Editor: Rosa Lukaszew

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A novel nanoscale fully depleted strained-SOI TFET (FD-SSOI TFET) is proposed and exhaustively simulated through Atlas Device Simulator. It is found that FD-SSOI TFET has the potential of improved on-current and steep subthreshold swing. Furthermore, the effect of strain and dimension on the threshold voltage of FD-SSOI TFET is thoroughly studied by developing a model based on its physical definition. The validity of the model is tested for FD-SSOI TFET by comparison to 2D device simulations. It is shown that the proposed model can predict the trends of threshold voltage very well. This proposed model provides valuable reference to the FD-SSOI TFETs design, simulation, and fabrication.

1. Introduction

Recently, minimizing energy consumption in mobile devices, processors, and biomedical electronics is one of the most challenging tasks. TFETs with steep subthreshold swing (less than 60 mV/dec) are considered as a promising device for low power applications [1–5]. However, in traditional TFETs, low on-current in comparison to conventional MOSFETs is the major shortcoming due to the poor tunneling probability of silicon. In addition, average subthreshold swing of traditional TFETs which is important for switch performance needs to be further improved [6]. By using narrow band gap materials, TFETs can achieve improved performance. Tensile strained silicon which has a smaller band gap than silicon and is compatible with conventional silicon processing can help to improve the tunneling currents. SOI technology has some straightforward advantages, such as the absence of latchup in CMOS structures and the reduction of parasitic capacitances. Single-layer strained-SOI (SSOI) structure [7, 8] combines the advantages of strained Si with thin film SOI and is less susceptible to misfit dislocation induced leakage current.

In this work, we propose a novel fully depleted SSOI TFET (FD-SSOI TFET) structure. High on-current can be

achieved by introducing SSOI structure, and the average subthreshold swing can be effectively decreased. Moreover, the effect of strain (in terms of equivalent Ge mole fraction X in the relaxed SiGe buffer), strained Si layer thickness, gate length, and other device parameters on the threshold voltage of FD-SSOI TFET is thoroughly studied by developing a model based on its physical definition. The results from the model are compared with the simulation results and are found to be in excellent agreement.

2. Device Structure and Simulations

The structure of an FD-SSOI N-TFET is shown in Figure 1, where V_s , V_g , V_d , and V_{sub} represent the source, gate, drain, and substrate electrode, respectively. The device consists of a high- κ dielectric layer with a thickness of t_{ox} , a strained Si layer with a thickness of t_{ssi} , a buried oxide layer with a thickness of t_{box} , and a gate with a length of L_g .

Simulations are done in Silvaco Atlas, using nonlocal band-to-band tunnelling model for including effect of tunneling, which is the most important model for TFETs simulations. Two other important models that are applied during simulations are the band gap narrowing model and the

FIGURE 1: Schematic representation of the FD-SSOI N-TFET used in this paper. Poisson's equation is solved on the three regions I, II, and III, corresponding to the depletion regions induced by the junctions inside the source and drain (I and III) and the intrinsic region (II).

quantum model (see [9, 10] for more details). The accuracy of these models has already been proven in [10, 11]. In simulations, junctions are ideally abrupt, with the doping concentration of $N_s = 10^{20} \text{ cm}^{-3}$ in the P^+ -type source, $N_i = 10^{17} \text{ cm}^{-3}$ in P^-/N^- -type body, and $N_d = 5 \times 10^{18} \text{ cm}^{-3}$ in the N-type drain, the gate length is $L_g = 50 \text{ nm}$, the gate dielectric thickness is $t_{ox} = 3 \text{ nm}$, the strained Si layer thickness is $t_{Si} = 10 \text{ nm}$, the gate work function is $\Phi_M = 4.5 \text{ eV}$, and the gate leakage is neglected.

In Figure 2, the Atlas simulated band diagrams are shown for a reference silicon TFET ($X = 0$) and for a FD-SSOI TFET ($X = 0.6$) in the on-condition. A narrowing of the barrier is seen in the case of the 0.6-equivalent Ge mole fraction device, which increases tunneling probability and hence I_{on} . Figure 3 shows the transfer characteristics for FD-SSOI TFETs with different strain (equivalent Ge mole fraction X in the relaxed SiGe buffer layer). The FD-SSOI TFET devices show large enhancements in the on-state current as compared to silicon TFET. The off-state leakage current is increased with increased strain but still in the fA range. In addition, a remarkable improvement is found in the point and average subthreshold swing, presented in more detail in Figure 4. Point subthreshold swing ranges from 17 mV/dec for the TFET without strain, down to 11 mV/dec for the device with strain whose Ge mole fraction up to 0.6, and average subthreshold swing ranges from 63 mV/dec down to 46 mV/dec.

The threshold voltage is one of the most important electrical parameters of a solid-state switch. For TFETs, the physical definition of threshold voltage is the gate voltage marking the transition between an exponential dependence and a linear dependence, of drain current on applied bias [12]. Figure 5 shows the threshold voltage of FD-SSOI TFET versus strain (equivalent Ge mole fraction X in the relaxed SiGe buffer layer). The threshold voltage is extracted from Atlas simulations using transconductance change (TC) method, which universally defines the threshold voltage of any nonlinear

FIGURE 2: Band diagram profiles along the channel in the on-condition. $V_{ds} = V_{gs} = 1 \text{ V}$.

device as the gate voltage corresponding to the maximum of the transconductance derivative $dg_m/dV_{gs}(dI_{DS}^2/dV_{gs}^2)$ [13]. It is shown that the threshold voltage decreases almost linearly with Ge mole fraction (from 1.25 V for no strain to 1.09 V for Ge mole fraction $X = 0.6$).

3. Model Derivation

3.1. Length of the Depletion Regions. Now we calculate the lengths of two depletion regions (L_1 and L_2). Since the basic structure of the FD-SSOI TFET is a gated PIN diode, the potential in the channel is modulated by the gate-source and drain-source voltage. To consider the influence of these two voltages on each other, L_1 and L_2 can be calculated

FIGURE 3: Simulated transfer characteristics of FD-SSOI TFETs for varying strain X .

FIGURE 4: Point and average subthreshold swings versus strain X in FD-SSOI TFETs.

FIGURE 5: Threshold voltages versus strain X in FD-SSOI TFETs.

by imposing $E_{s,I}(-L_1) = 0$ and $E_{s,III}(L_g + L_2) = 0$, but the calculation would be complicated. Here a useful approximation is made, separately considering the source-body junction and body-drain junction. In a junction, from the potential drop across the junction the length of the depletion region can be calculated [14]. Therefore, the values of L_1 and L_2 can be calculated as

$$L_1 = \sqrt{\frac{2\epsilon_{si}(\phi_l - \phi_s)}{qN_s}}, \quad (1)$$

$$L_2 = \sqrt{\frac{2\epsilon_{si}(\phi_d - \phi_l)}{qN_d}},$$

with

$$\phi_s = -\frac{KT}{q} \log\left(\frac{N_s}{n_{i,SSi}}\right)$$

$$\phi_d = V_{ds} + \frac{KT}{q} \log\left(\frac{N_d}{n_{i,SSi}}\right) \quad (2)$$

$$\phi_l = V'_{gs} - \frac{qN_it_{ssit_{ox}}}{\epsilon_{SSi}},$$

where ϕ_s is the boundary value of the potential at source depletion end, ϕ_d is the boundary value of the potential at drain depletion end, ϕ_l is the potential in intrinsic region due to the gate without influence of the junctions, $n_{i,SSi}$ is the intrinsic carrier concentration in strained Si [15], and ϵ_{SSi} is the strained Si dielectric constant.

3.2. Surface Potential Model. For the FD-SSOI N-TFET structure in Figure 1, the 2D Poisson equation in the strained silicon layer can be written as

$$\frac{\partial^2 \phi_i(x, y)}{\partial x^2} + \frac{\partial^2 \phi_i(x, y)}{\partial y^2} = -\frac{qN}{\epsilon_{SSi}} \quad (3)$$

$$0 \leq x \leq t_{SSi}, \quad i = I, II, III,$$

where $\phi_i(x, y)$ is the electrostatic potential in regions I, II, and III and N is the strained Si layer effective doping and is equal to $-N_s$ in the region I, N_d in the region III, and $\pm N_i$ in the region II.

The potential profile in the vertical direction in strained Si layer can be approximated by a parabolic function as [16]

$$\phi_i(x, y) = \phi_{s,i}(y) + a_{0,i}(y)x + a_{1,i}(y)x^2 \quad (4)$$

$$0 \leq x \leq t_{SSi}, \quad i = I, II, III,$$

where the coefficients $a_{0,i}(y)$ and $a_{1,i}(y)$ are functions of y only and $\phi_{s,i}(y)$ is the surface potential in regions I, II, and III.

For region II, the coefficients $a_{0,II}(y)$ and $a_{1,II}(y)$ can be solved by the following boundary conditions:

$$\left[\frac{d\phi_{II}(x, y)}{dx} \right]_{x=0} = -\frac{\epsilon_{ox}}{\epsilon_{SSi}} \left(\frac{V'_{gs} - \phi_{s,II}(y)}{t_{ox}} \right), \quad (5)$$

$$\left[\frac{d\phi_{II}(x, y)}{dx} \right]_{x=t_{SSi}} = 0,$$

where ϵ_{ox} is the dielectric constant of the gate dielectric, t_{ox} is the gate dielectric thickness, $V'_{gs} = V_{gs} - (V_{\text{FB},f})_{\text{SSi}}$, and $(V_{\text{FB},f})_{\text{SSi}}$ is the flatband voltage, which can be expressed as $(V_{\text{FB},f})_{\text{SSi}} = (V_{\text{FB},f})_{\text{Si}} + \Delta V_{\text{FB},f}$, with $(V_{\text{FB},f})_{\text{Si}} = \phi_M - \phi_{\text{Si}}$, $\Delta V_{\text{FB},f} = (-\Delta E_C/q) + (\Delta E_g/q) - V_T \ln(N_{V,\text{Si}}/N_{V,\text{SSi}})$:

$$\begin{aligned}\Delta E_C &= 0.57X, \\ \Delta E_g &= 0.4X, \\ V_T \ln\left(\frac{N_{V,\text{Si}}}{N_{V,\text{SSi}}}\right) &= V_T \ln\left(\frac{m_{h,\text{Si}}^*}{m_{h,\text{SSi}}^*}\right)^{3/2} \approx 0.075X,\end{aligned}\quad (6)$$

where ϕ_M is the gate work function, ϕ_{Si} is the Si work function, ΔE_C and ΔE_g are the increase in electron affinity and the decrease in the band gap of Si due to strain, respectively, $V_T = KT/q$ is the thermal voltage, $N_{V,\text{Si}}$ and $N_{V,\text{SSi}}$ are the density of states in the valence band in Si and strained Si, respectively, $m_{h,\text{Si}}^*$ and $m_{h,\text{SSi}}^*$ are the hole density of states effective masses in Si and strained Si, respectively, and X is the Ge mole fraction in $\text{Si}_{1-x}\text{Ge}_x$ substrate.

Substituting the coefficients $a_{0,\text{II}}(y)$ and $a_{1,\text{II}}(y)$ in (4) and then in (3), we obtain

$$\frac{\partial^2 \varphi_{s,\text{II}}(y)}{\partial y^2} - \alpha_2^2 \varphi_{s,\text{II}}(y) = \beta_2, \quad (7)$$

where $\alpha_2^2 = C_{\text{ox}}/t_{\text{SSi}}\epsilon_{\text{SSi}}$, $\beta_2 = qN_i/\epsilon_{\text{SSi}} - C_{\text{ox}}V'_{gs}/t_{\text{SSi}}\epsilon_{\text{SSi}}$.

In the above relations, $C_{\text{ox}} = \epsilon_{\text{ox}}/t_{\text{ox}}$.

The above equation (7) is a simple second-order nonhomogenous differential equation which has a solution of the form

$$\varphi_{s,\text{II}}(y) = A_2 \exp(\alpha_2 y) + B_2 \exp(-\alpha_2 y) - \frac{\beta_2}{\alpha_2^2}. \quad (8)$$

The electric field distribution can be written as

$$E_{s,\text{II}}(y) = -A_2 \alpha_2 \exp(\alpha_2 y) + B_2 \alpha_2 \exp(-\alpha_2 y). \quad (9)$$

On the regions I and III, the fringing field effect is taken into account by conformal mapping techniques as $C'_{\text{ox}} \cong (2/m\pi)(\epsilon_{\text{ox}}/t_{\text{ox}})$ (m must satisfy the condition $\sin(m\pi/2) = 1$) [16]. Then, the surface potential in regions I and III can be written as

$$\begin{aligned}\varphi_{s,\text{I}}(y) &= A_1 \exp(\alpha_1 y) + B_1 \exp(-\alpha_1 y) - \frac{\beta_1}{\alpha_1^2}, \\ \varphi_{s,\text{III}}(y) &= A_3 \exp(\alpha_3 y) + B_3 \exp(-\alpha_3 y) - \frac{\beta_3}{\alpha_3^2}.\end{aligned}\quad (10)$$

The electric field distribution in these regions can be written as

$$\begin{aligned}E_{s,\text{I}}(y) &= -A_1 \alpha_1 \exp(\alpha_1 y) + B_1 \alpha_1 \exp(-\alpha_1 y), \\ E_{s,\text{III}}(y) &= -A_3 \alpha_3 \exp(\alpha_3 y) + B_3 \alpha_3 \exp(-\alpha_3 y),\end{aligned}\quad (11)$$

where $\alpha_1^2 = \alpha_3^2 = C'_{\text{ox}}/t_{\text{SSi}}\epsilon_{\text{SSi}}$, $\beta_1 = (qN_s/\epsilon_{\text{SSi}}) - C'_{\text{ox}}V'_{gs}/t_{\text{SSi}}\epsilon_{\text{SSi}}$, and $\beta_3 = -(qN_d/\epsilon_{\text{SSi}}) - C'_{\text{ox}}V'_{gs}/t_{\text{SSi}}\epsilon_{\text{SSi}}$.

Using the boundary conditions (12), the unknown functions A_1 , B_1 , A_2 , B_2 , A_3 , and B_3 in (8) and (10) can be obtained:

$$\begin{aligned}\varphi_{s,\text{I}}(-L_1) &= -\frac{KT}{q} \log\left(\frac{N_s}{n_{i,\text{SSi}}}\right), \\ \varphi_{s,\text{III}}(L_2 + L_g) &= V_{ds} + \frac{KT}{q} \log\left(\frac{N_d}{n_{i,\text{SSi}}}\right), \\ \varphi_{s,\text{I}}(0) &= \varphi_{s,\text{II}}(0), \\ \varphi_{s,\text{II}}(L_g) &= \varphi_{s,\text{III}}(L_g), \\ E_{s,\text{I}}(0) &= E_{s,\text{II}}(0), \\ E_{s,\text{II}}(L_g) &= E_{s,\text{III}}(L_g).\end{aligned}\quad (12)$$

3.3. Threshold Voltage Model. The physically based definition of threshold voltage for TFETs is the gate voltage marking the transition of drain current on applied bias between an exponential dependence and a linear dependence. This also marks the transition between the strong control and weak control of the tunneling energy barrier width at the tunnel junction by the gate voltage. The inflection point in tunneling energy barrier width (w_{bs}) [3, 12] shows this transition point. The threshold voltage of FD-SSOI TFET is taken to be that value of gate-source voltage for which the potential in the point $y = w_{bs}$ reaches the value $V_{ds} + (KT/q)\log(N_d/n_{i,\text{SSi}})$. Hence, by substituting $y = w_{bs}$ and $V_{ds} + (KT/q)\log(N_d/n_{i,\text{SSi}})$ into (8), we can get the following equation:

$$\begin{aligned}A_2 \exp(\alpha_2 w_{bs}) + B_2 \exp(-\alpha_2 w_{bs}) - \frac{\beta_2}{\alpha_2^2} \\ = V_{ds} + \frac{KT}{q} \log\left(\frac{N_d}{n_{i,\text{SSi}}}\right).\end{aligned}\quad (13)$$

In the above relation, A_2 , B_2 , and β_2 are the function of V_{gs} .

Threshold voltage values of FD-SSOI TFET can be determined by solving this equation numerically for V_{gs} , which are shown in Section 4.

4. Model Evaluation

The threshold voltage is extracted from simulations using the TC method. This method locates the voltage where there is a transition between strong and weak control of the tunneling energy barrier width, consistent with the model formulation.

Figure 6 plots the variation of threshold voltage with change in strain (i.e., equivalent Ge mole fraction X). The line represents the model results, and scatter represents the simulation results. It can be found that the threshold voltage obtained from the model tracks the simulation values very well. We also observe that threshold voltage V_{th} is lower for higher strain in the strain silicon layer. This reduction in the threshold voltage of FD-SSOI TFET with an increasing Ge mole fraction X can be attributed to a reduced band gap at the tunnel junction. The model presented in this paper can describe this effect well.

FIGURE 6: Threshold voltage versus strain X . $V_{ds} = 1$ V, $L_g = 50$ nm, $\epsilon_{ox} = 29$, $t_{ox} = 3$ nm, and $t_{SSi} = 10$ nm.

FIGURE 8: Threshold voltage versus strained Si layer thickness t_{SSi} . $\epsilon_{ox} = 29$, $t_{ox} = 3$ nm, $L_g = 50$ nm, and $V_{ds} = 1$ V.

FIGURE 7: Threshold voltage versus gate length L_g . $\epsilon_{ox} = 29$, $t_{ox} = 3$ nm, $t_{SSi} = 10$ nm, and $V_{ds} = 1$ V.

The variation of threshold voltage with the gate length L_g for $X = 0$ and $X = 0.3$ is plotted in Figure 7. As can be seen from Figure 7, there is no obvious change in threshold voltage with change in gate length. It is also observed that the threshold voltage of FD-SSOI TFETs is lower for higher strain. The threshold voltage values from our model are in close proximity with the simulation results. This suggests that scaling the gate length L_g of FD-SSOI TFET has little effect on the threshold voltage as long as gate length is longer than some critical length at which too much P-I-N leakage current occurs in the off-state. In general, the critical length is about the order of 10 nm [17, 18], which is a function of ϵ_{ox} , t_{ox} , t_{SSi} , $n_{i,SSi}$, and so forth and needs further study. Here, FD-SSOI TFET scaling is restricted to 20 nm.

In Figure 8, the variation of threshold voltage with change in strained Si layer thickness is plotted for $X = 0$ and $X = 0.3$.

FIGURE 9: EOT versus gate dielectric permittivity.

It is observed that threshold voltage increases with increase in strained Si layer thickness.

Improved characteristics of FD-SSOI TFET can be obtained by careful choice of a gate dielectric. Figure 9 shows the variation of EOT (equivalent oxide thickness) with gate dielectric permittivity for $t_{ox} = 3$ nm. As shown in the figure, for a given gate dielectric thickness, the EOT decreases with increasing gate dielectric permittivity. Figure 10 shows the variation of threshold voltage with gate dielectric permittivity for different values of drain-source voltage and for a Ge mole fraction of 0.3. It is observed that the device with the high- κ gate dielectric or the thinner EOT has the low threshold voltage. A higher gate dielectric permittivity or a smaller EOT increases the gate control, thereby decreasing the threshold voltage. We can also observe that the threshold voltage is lower for lower drain-source voltage. This result can be confirmed from Figure 10. The proposed model can predict the change in threshold voltages induced by the high- κ gate dielectric very well.

FIGURE 10: Threshold voltage versus gate dielectric permittivity. $t_{ox} = 3\text{ nm}$, $t_{ssi} = 10\text{ nm}$, $L_g = 50\text{ nm}$, and $X = 0.3$.

5. Conclusion

We have proposed and exhaustively simulated a novel nanoscale FD-SSOI TFET structure. Due to using SSOI structure, the FD-SSOI TFET shows high on-current and steeper SS, exhibiting significant performance improvement compared with traditional Si TFET. Furthermore, based on the physical definition of threshold voltage for FD-SSOI TFET, a threshold voltage model for FD-SSOI TFET has been developed. We have shown that the model can predict the trends of the device characteristics very well. The model can also predict the improved performance on the physical threshold voltage when using SSOI structure, high- κ dielectrics, and thin strained Si film and the limited effect on threshold voltage when scaling the gate length.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgment

The project is supported by the National Natural Science Foundation of China (Grant no. 61474085).

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