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Research Article

Analysis of Conduction and Charging Mechanisms in Atomic Layer Deposited Multilayered HfO_2/Al_2O_3 Stacks for Use in Charge Trapping Flash Memories

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Method for characterization of electrical and trapping properties of multilayered high permittivity stacks for use in charge trapping flash memories is proposed. Application of the method to the case of multilayered HfO_2/Al_2O_3 stacks is presented. By applying our previously developed comprehensive model for MOS structures containing high-κ dielectrics on the $J-V$ characteristics measured in the voltage range without marked degradation and charge trapping (from −3 V to +3 V), several parameters of the structure connected to the interfacial layer and the conduction mechanisms have been extracted. We found that the above analysis gives precise information on the main characteristics and the quality of the injection layer. $C-V$ characteristics of stressed (with write and erase pulses) structures recorded in a limited range of voltages between −1 V and +1 V (where neither significant charge trapping nor visible degradation of the structures is expected to occur) were used in order to provide measures of the effect of stresses with no influence of the measurement process. Both trapped charge and the distribution of interface states have been determined using modified Terman method for fresh structures and for structures stressed with write and erase cycles. The proposed method allows determination of charge trapping and interface state with high resolution, promising a precise characterization of multilayered high permittivity stacks for use in charge trapping flash memories.

1. Introduction

High permittivity (high-κ) dielectric stacks are subject of particular interest as material for charge trapping flash memories [1–3]. Stacks of different high-κ oxides, such as Al_2O_3-TiO_2-Al_2O_3 [4], combinations with semiconductor layers such as Al_2O_3–Cu_2O [5], and compound high-κ oxides [6] have proven to provide effective solutions for the choice of material for trapping layer.

Multilayered high-κ stacks present increasing interest for researchers [7]. Precise characterization of the trapping properties is required in order to describe correctly the functioning of the charge trapping memory devices.

The issues of relation between conduction mechanisms and electrically active defects have been studied [8], as well as the charging mechanisms that are to be considered in the case of charge trapping memories [9, 10]. The particular role of the blocking layer and effect of double-layered blocking oxide have been studied in [11].

In [12] it has been demonstrated that while inserting thin Al_2O_3 layer in HfO_2 films, memories exhibit larger memory window, faster program/erase speed, and better

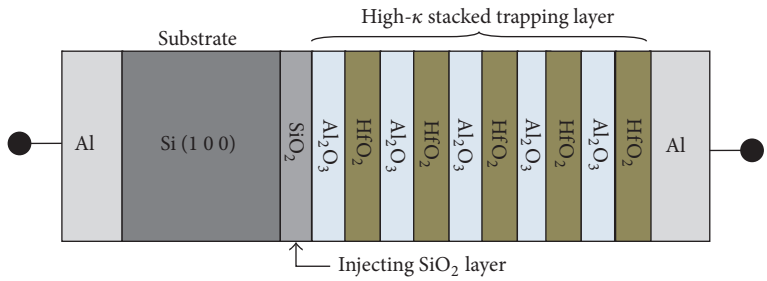

Figure 1: Schematic representation of the test structure used in this study.

data retention. These improvements are explained by the modulation of charge distribution by bandgap engineering in trapping layer. Based on this, in this work Al_2O_3/HfO_2 nanolaminates as a promising solution for charge trapping flash memories are studied.

In the present work our aim is to propose a method of characterization of trapping using sensitive nondestructive methods. For this purpose, a structure without blocking layer is used. Oxide and interface charge are characterized by using recently proposed modified Terman method [13].

2. Fabrication of the Samples and Experimental Procedure

The samples studied here were fabricated on p-type (1 0 0) 7 Ω cm Si substrates. After chemical cleaning, a multilayered stack $5 \times (HfO_2/Al_2O_3)$ has been deposited by atomic layer deposition. The thickness of each HfO_2 layer is 2.8 nm and that of each Al_2O_3 layer is 1.0 nm. Calculations of the thicknesses were done based on the previously made calibration of the fabrication process. Total high-κ stacked layer thickness is therefore $5 \times (2.8 + 1.0)$ nm = 19 nm. After deposition, the samples were subject to rapid thermal annealing in N_2 at 800°C for 1 min.

In order to obtain as thinnest as possible tunneling SiO_2 layer, no particular oxidation was made prior high-κ stacked layer deposition. As is known, due to thermodynamic instability, an interfacial layer is inevitably grown between the Si substrate and the high-k layer [14]. Thus, an interfacial oxide layer about 2.5 nm thick has been grown during the fabrication of the structures. This value of the interfacial layer thickness was estimated by previous calibrations of the fabrication process and is in accordance with extrapolations from literature values reported in the work [15].

The gate areas of the devices used in this study were $S = 2.5 \times 10^{-3}$ cm^2. Al metal gates were obtained by thermal evaporation and structured by photolithography. Backside of Si substrate was also Al metalized, providing a back ohmic contact.

C-V characteristics were measured in serial mode at the signal level of 24 mV and frequency of 100 Hz with the use of a HP 4284 A LCR-meter. $I - V$ (leakage) characteristics were measured by using a HP4140A picoammeter/DC voltage source, for both positive and negative gate polarity, in the voltage range from −6 V to +24 V. Current was measured in steps of 0.05 V, with a hold time of 5 s, in order to suppress the displacement currents.

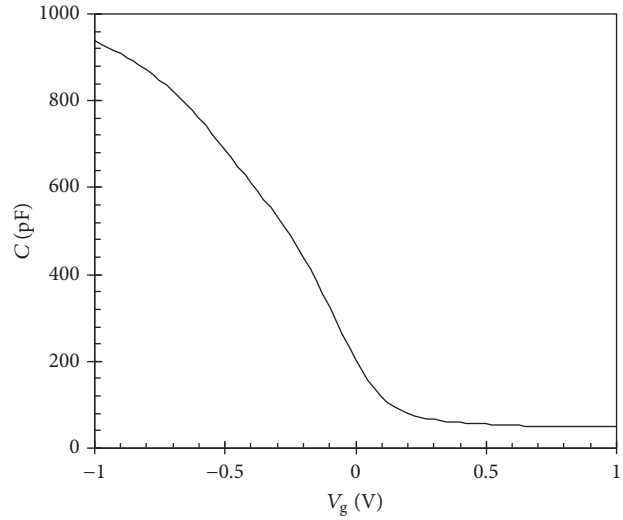

Figure 2: $C - V$ characteristic of a fresh structure.

A schematic representation of the test Al-high-κ/SiO_2-Si structure is shown in Figure 1.

3. $C - V$ Characteristics of Fresh Structures

First, $C - V$ characteristics of the fresh structure in a limited voltage range between −1 V and +1 V (Figure 2) have been analyzed. Neither significant charge trapping nor visible degradation of the test Al-high-κ/SiO_2-Si structures is expected to occur under these measurement conditions, as it was found in our previous works on similar structures. The method described in detail in [13] was used.

Capacitance (C_0) of the whole dielectric stack (multilayered HfO_2/Al_2O_3 trapping layer/SiO_2) was determined using the extrapolation method proposed by Kar et al. [16]. Illustration of the application of this method in determination of C_0 is given in Figure 2. Value of $1/C_0$ is obtained from the intercept of the fitted straight line of the plot of $\sqrt{(d/dV_g)(1/C^2)}$ versus $1/C$ (Figure 3).

Thus obtained capacitance is C_0 = 1152 pF. Corresponding equivalent thickness is 7.49 nm. The flatband voltage obtained

Table 1: Parameters used in the theoretical calculations shown in Figure 6; indices h and e are for holes and electrons, respectively.

d_{in} (nm)	d_{hk} (nm)	σ_{hc} (Ω^{-1} cm^{-1})	σ_{PF} (Ω^{-1} cm^{-1})	Φ_e (eV)	Φ_h (eV)
2.53	19.0	1×10^{-16}	8×10^{-17}	3.15	4.7

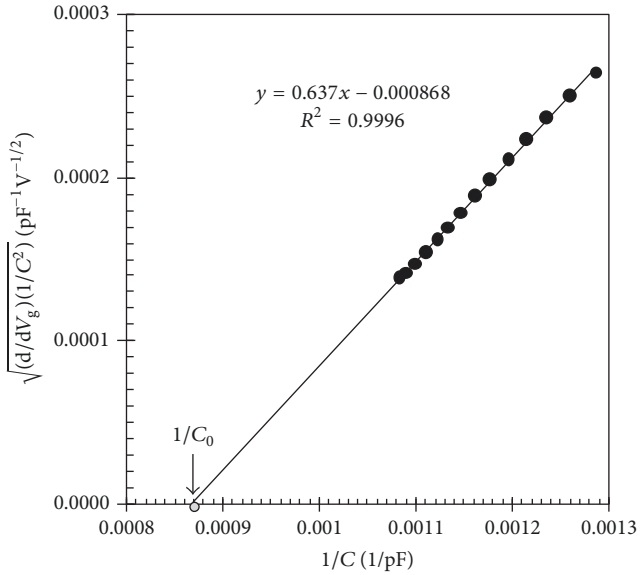

Figure 3: Illustration of the method of determination of the capacitance in accumulation.

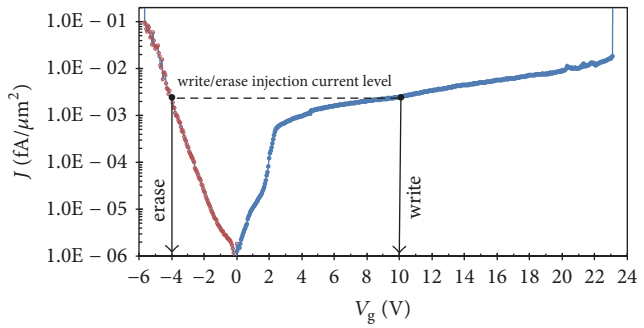

Figure 4: $J-V$ characteristics of the structures for both positive and negative gate polarity.

from these experimental data is $V_{fb} = -0.005$ V, and the flatband capacitance is 221.4 pF.

4. Complete J-V Characteristic

Next, J-V characteristics of the structure for both positive and negative gate polarity until destructive breakdown were studied. Curves for positive and for negative gate were recorded separately on different fresh devices. Typical curves are shown in Figure 4. For negative gate, destructive breakdown is observed at voltages of about 5.65 V, while for positive gate breakdown voltage is much higher, attaining the value of 23.1 V. The situation with the breakdown current values is opposite: for negative bias it is 0.1 fA/μm^2 while for positive gate bias it is only 0.02 fA/μm^2. In both cases the breakdown power ($J \cdot V_g$) is practically the same (0.5 W/m^2). This finding indicates that the final destructive breakdown of the structure is dominantly dissipation related.

In order to avoid severe degradation and breakdown, injection current level is to be selected at much lower values than the lowest breakdown current value, that is, 0.02 fA/μm^2. Here, we choose the value of 0.002 fA/μm^2, an order of magnitude lower than the lowest breakdown current measured. Corresponding write voltage (positive) is +10 V, while the corresponding erase voltage (negative) is −4 V.

5. Low Voltage Segments of $J-V$ Characteristic

Several parameters of the interfacial layer and conduction mechanisms can be extracted, by consideration of the $J-V$ characteristics in the narrow voltage range where no marked degradation and charge trapping (from −3 V to +3 V) occur and applying the comprehensive model for structures containing Ta_2O_5 developed in [17] and explained in detail [18] for structures with various high-κ dielectrics. The method is briefly described below.

Band diagram of the considered structure constructed on the same way as it was described in [17] for Al-Ta_2O_5/SiO_2-Si structures is shown in Figure 5. Data for nanolaminated Al_2O_3/HfO_2 films are taken from the work [19].

First, the voltage drop across the whole dielectric stack (referred to as oxide voltage, V_{ox}) corresponding to the applied voltage on the structure (V_g) is calculated by using the expression:

$$V_{ox} = V_g - V_{fb} - V_s, \tag{1}$$

where V_{fb} is the flatband voltage and V_s the voltage drop in silicon (surface potential).

Depending on the oxide voltage level, injection current in SiO_2 is due to direct tunneling through a trapezoidal barrier or due to Fowler-Nordheim tunneling trough a triangular barrier. Direct tunneling current density (J_t) through the injecting SiO_2 layer is given by the following expression:

$$J_t = \frac{q^2}{8\pi h\Phi} E_{in}^2 \cdot \exp\left(-\frac{8\pi\sqrt{2m^* q\Phi^3}}{3hE_{in}}\left(1-\left(1-\frac{d_{in}}{\Phi}E_{in}\right)^{3/2}\right)\right), \tag{2a}$$

and for Fowler-Nordheim tunneling it is given by

$$J_t = \frac{q^2}{8\pi h\Phi} E_{in}^2 \exp\left(-\frac{8\pi\sqrt{2m^* q\Phi^3}}{3hE_{in}}\right), \tag{2b}$$

where q is the electron charge, h is Planck's constant, m^* is the effective tunneling mass of carriers in SiO_2, d_{in} is the

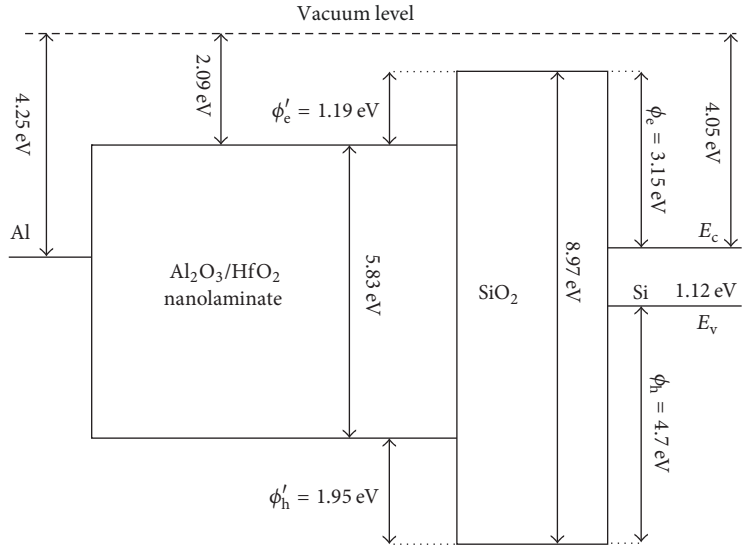

Figure 5: Energy band diagram for the structure studied in this work.

thickness of injecting SiO_2 layer, Φ is the tunneling barrier height, and E_{in} is the electric filed in the injecting SiO_2 layer.

Different carriers from the silicon substrate produce this current: electrons in the case of gate positively biased and holes in the case of gate negatively biased [17]. Total current through the injection layer (J_{in}) is

$$J_{in} = J_t + \sigma_{hc} E_{in}, \tag{3}$$

where σ_{hc} is the hoping conductivity of the injecting SiO_2 layer.

The current density due to the Poole-Frenkel effect in the high-κ stacked trapping layer (J_{PF}) is given by the following expression:

$$J_{PF} = \sigma_{PF} E_{hk} \exp\left(\frac{1}{kT}\sqrt{\frac{q^3}{\pi\varepsilon_0 K_T}}\sqrt{E_{hk}}\right), \tag{4}$$

where E_{hk} is the effective electric field in the high-κ stacked trapping layer, σ_{PF} is temperature-dependent defect-related constant having dimensions of conductivity, k is the Boltzmann constant, ε_0 is the dielectric constant of vacuum, and $K_T = n^2$ is the optical frequency dielectric constant (n is the effective refractive index of the high-κ stacked trapping layer).

Theoretical oxide voltage is calculated as

$$V_{ox} = d_{in} E_{in} + d_{hk} E_{hk}, \tag{5}$$

where d_{hk} is the thickness of the high-κ stacked trapping layer.

Theoretical determination of the parameters is done numerically using the steady state condition for the current densities

$$J = J_{in} = J_{hk}. \tag{6}$$

In Figure 6 the experimental results (circles) for leakage currents as a function of the oxide voltage that are compared with the theoretically obtained curves are shown. Very good agreement between the theoretical and experimental curves is obtained, confirming that expected conduction mechanisms are the most important ones in the studied structure. Saturation of the current in inversion (at positive gate polarity), observed for oxide voltages higher than 1.5 V, is explained to be due to the exhaustion of minority carriers (electrons in p-type substrate) [17]. This part has a shape of a reverse biased diode characteristics and can be included in a complete model for the device using an equivalent circuit containing a diode connected in series with the structure [18]. Since the main aim of this work is to study conduction and trapping properties of a nanolaminated high-κ dielectric, we do not consider this part of the characteristics. Details on the fitting method and determination of the parameters are explained in [17].

Applicability of the theory used in this work has been previously tested on many various metal-high-κ/SiO_2-Si structures, which is resumed in our review paper [18]. In inversion (positive gate in the case of a p-type substrate) saturation occurs at approximately 2 V. In accumulation, the straightforward application of the theory is limited by the appearance of wear-out and charge trapping at higher voltages, depending on the interfacial layer thickness and the high-κ composition and quality. Usually, limiting values are between 3 V and 7 V. In this work only small effect of charge trapping (slightly lower leakage current) is manifested for the three rightmost measured points, thus justifying the use of the theory in the given measurement range.

Optimal values of the parameters used in computation are displayed in Table 1. Nonlinear successive adjustment of the parameters (d_{in}, σ_{hc}, σ_{PF}, Φ_e, and Φ_h) fitting method has been used, as it was described in the work [17]. Barrier heights for injections of electrons (Φ_e) and holes (Φ_h) from the Si substrate play important role in the considered range along with the conduction mechanism in the high-κ layer. For dielectric films substantially thicker than 10 nm, voltage

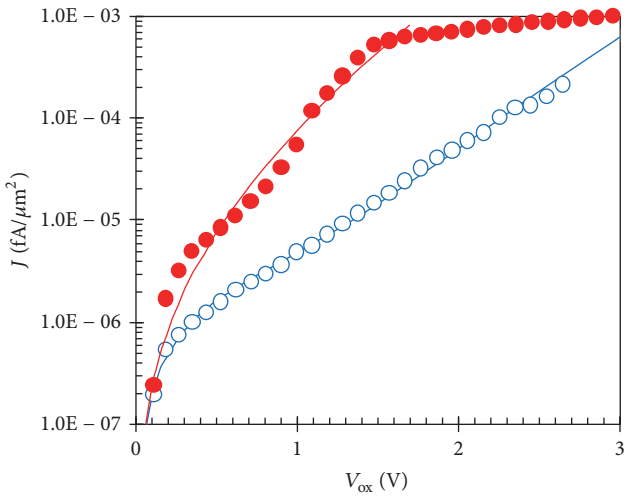

FIGURE 6: Experimental $J-V$ characteristics (circles) and theoretical curves (solid lines); full circles are for positive gate bias and empty circles for negative one.

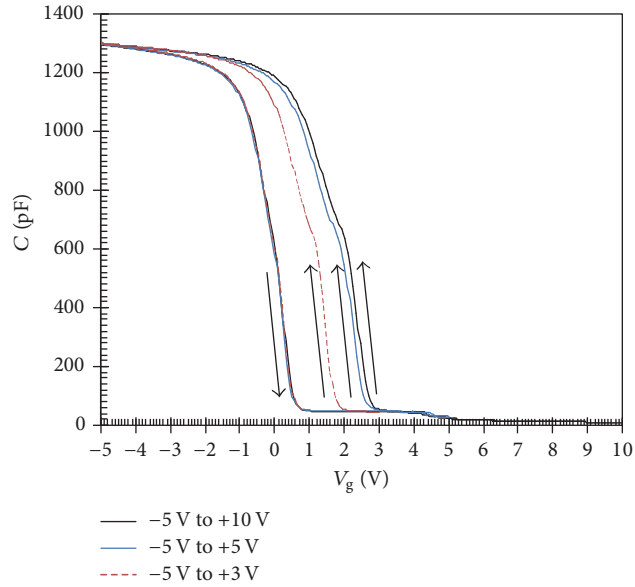

FIGURE 7: C-V hysteresis between maximum write and erase voltages.

regions with dominant conduction mechanism for similar structures can be clearly separated, as is shown in [20]. However, as we have demonstrated in [21], in the case of nanosized high-κ dielectrics methods based on the use of single dominant conduction mechanism are inconsistent and the use of models that involve simultaneously several mechanisms has to be considered.

Significant information on the quality of both the injection and the high-κ stacked trapping layer is obtained using the extracted parameters given in Table 1. First, the precise value of the injection layer thickness (electrical thickness) is obtained (d_{in} = 2.53 nm). This is the most relevant figure describing the electrical properties of the injection layer. Second, the values of barrier heights for electrons and holes are 3.15 eV and 4.7 eV, respectively, as is expected for stoichiometric SiO_2 layer. In addition, the value of the hopping conductivity of this layer ($\sigma_{hc} = 1 \times 10^{-16}\ \Omega^{-1}\,cm^{-1}$) is exceptionally low, showing that the injecting layer is of particularly good quality, since the hopping conductivity currents are substantially lower than the injection currents which are the main mechanism allowing proper functioning of the charge trapping flash memories. For a comparison, the value of the hopping conductivity obtained for $Al/ZrO_2/Al_2O_3/ZrO_2/SiO_2/Si$ structures ($\sigma_{hc} = 3.5 \times 10^{-11}\ \Omega^{-1}\,cm^{-1}$) [9] is markedly higher than for the structures studied here. Such low value as obtained here is close to the value obtained for $Al/Ta_2O_5/SiO_2/Si$ structures ($\sigma_{hc} = 5 \times 10^{-17}\ \Omega^{-1}\,cm^{-1}$) where dielectric ($Ta_2O_5$) is obtained by thermal oxidation of Ta [17], thus providing exceptionally low density of defects.

Therefore, we conclude that the above analysis gives precise information on the main characteristics and the quality of the injection layer.

6. $C-V$ Hysteresis

Usually, the structures to be used in trapping memories are characterized by $C-V$ hysteresis. Different sweeping ranges have been tested in order to determine the optimal write voltage providing satisfactory value for the memory window. Such hysteresis loops between the voltages −5 V to +3 V, −5 V to +5 V, and −5 V to +10 V are shown in Figure 7.

It is important to note the observation that capacitance in accumulation at −5 V has substantially higher value (1300 pF) than that obtained on fresh structures using limited voltage range from −1 V to +1 V (1152 pF). Above difference is not due to the method of extrapolation, which has been shown to give precise estimates of the capacitance of the insulating layer itself, but to some real changes in the dielectric. Namely, as we have shown in the work [22], voltage stress causes an increase of the capacitance in accumulation (C_0) by effective thinning of the SiO_2 layer by creation of conductive paths in this layer during the stress, as it was previously found from stress induced leakage current characteristics in the work [23]. Detailed study of the variations of $C-V$ characteristics with consecutive runs has been reported in [24].

Hysteresis width ΔV_{fb} = 2.1 V is obtained for sweeping between −5 V and +10 V, ΔV_{fb} = 2.0 V is obtained for sweeping between −5 V and +5 V, and ΔV_{fb} = 1.2 V is obtained for sweeping between −5 V and +3 V. Above values are consistent with the literature results obtained for Al_2O_3/HfO_2 stacks on $In_{0.53}Ga_{0.47}As$ [25]. Namely, in [25] it is observed that there is a maximum value of ΔV_{fb} between the two Al_2O_3/HfO_2 thicknesses ratios of 2.5 nm/3.0 nm and 0.5 nm/2.5 nm higher than or equal to 0.4 V. From our experiment a higher value of 1.2 V is obtained for the thicknesses ratio 1.0 nm/2.5 nm. This value is substantially higher than the value reported for pure HfO_2 [26] under similar conditions. Therefore, it can be concluded that the insertion of Al_2O_3 between HfO_2 layers for the given thickness ratio substantially increases the trapping in the high-κ stacked layer.

Values of flatband voltages for runs left from different starting positive voltages and for the runs back right from

Table 2: Flatband voltages of the samples for various runs.

Start point	Fresh	−5 V	+3 V	+5 V	+10 V
V_{fb} (V)	−0.01	0.37	1.54	2.33	2.49
Q_{ox} (cm^{-2})	-1.9×10^{12}	-2.9×10^{12}	-6.2×10^{12}	-8.4×10^{12}	-8.9×10^{12}

Table 3: Flatband voltages and oxide charge after the write and the erase pulse.

	Erase	Write
V_{fb} (V)	0.41	0.76
Q_{ox} (cm^{-2})	-3.0×10^{12}	-4.0×10^{12}

−5 V are given in Table 2. Corresponding calculated oxide charges are also shown.

As is seen from Figure 6, increase of the turn-around voltage from +5 V to +10 V does not significantly enlarge the hysteresis width (only about 0.1 V). This finding can be explained by rather small increase of the injection current in that voltage region (see Figure 4). Therefore, it is no use to increase the write voltage over 5 V, since the gain in ΔV_{fb} is rather small, while the degradation of the structure will become rather important, thus limiting the endurance of the devices.

An important feature of the structures is the observed higher absolute value of the oxide charge after both runs left and runs rights compared to the fresh sample. Therefore, when applying voltages substantially higher than ±1 V, irreversible change of the oxide charge occurs. After this initial irreversible change, repeatable patterns of the C–V curves are obtained depending generally on the starting voltage. This is a common behavior of the metal/high-κ/SiO_2/Si structures, as we have shown in [24].

7. Detailed Analysis of $C - V$ Characteristics of Stressed Structures

In this section, C-V characteristics (measured in a limited voltage range between −1 V and +1 V) of stressed (with write and erase pulses) structures (Figure 8) have been analyzed. Since neither significant charge trapping nor visible degradation of the structures is expected to occur under these measurement conditions, by this method of analysis precise measures of the effect of stresses can be found with no influence of the measurement process itself.

It is seen that the write pulse (+5 V for 60 s) causes a shift to the right (trapping of electrons). Erase pulse (−5 V for 60 s) shifts the curve back to the left, as a result of removal of electrons trapped during the write pulse. Holes injected from the substrates at negative gate bias are expected to be responsible for this effect.

Flatband voltages (V_{fb}) corresponding to the shown curves and the calculated values of the oxide charges (Q_{ox}) are summarized in Table 3.

Oxide charge obtained after the erase pulse (−5 V for 60 s) is practically equal to these obtained from the measured $C - V$ curves with starting point −5 V. Therefore, it is to be concluded that no significant discharging occurs between

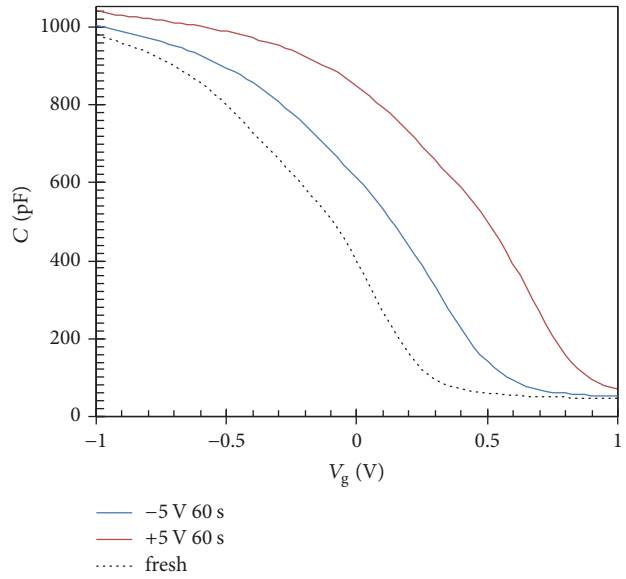

Figure 8: $C - V$ characteristics of the structures after write (+5 V for 60 s, thick line) and erase (−5 V for 60 s, thin line) cycles. For comparison $C - V$ characteristic of the fresh sample (Figure 1) is shown as dotted line.

the end of the erase pulse and the consecutive $C - V$ measurement between −1 V and +1 V. In contrast with this behavior, the absolute value of the oxide charge extracted from $C - V$ measurement after the write pulse (+5 V for 60 s) is substantially lower than this obtained from the measured $C - V$ curves with starting point +5 V. Above finding can be attributed to the discharge of a significant part of negative charge (4.4×10^{12} cm^{-2}) trapped during the write pulse. Most probably, this is the part of the charge that is accumulated at the interface between the injecting SiO_2 layer and the multilayered HfO_2/Al_2O_3 stack [9]. By adding a blocking layer, the total oxide charge to be retained is expected. However, due to the leakage, retention time for the accumulated charge at the interface of the high-κ with the injecting layer [27] is expected to be substantially lower than that for the trapped charge. Further improvement of the fabrication process is to be intended towards increasing the part of the charge trapped in the stack. Here described method can be effectively used in such an analysis.

In order to analyze in more detail the trapping/detrapping process, detailed analysis of $C - V$ characteristic of fresh and stressed structures using the method described in [13] has been performed here. Results for fresh samples are shown in several steps, while for the others the final figures only are presented.

In Figure 9 distribution of densities of interface states (D_{it}) obtained by standard Terman method versus energy (E)

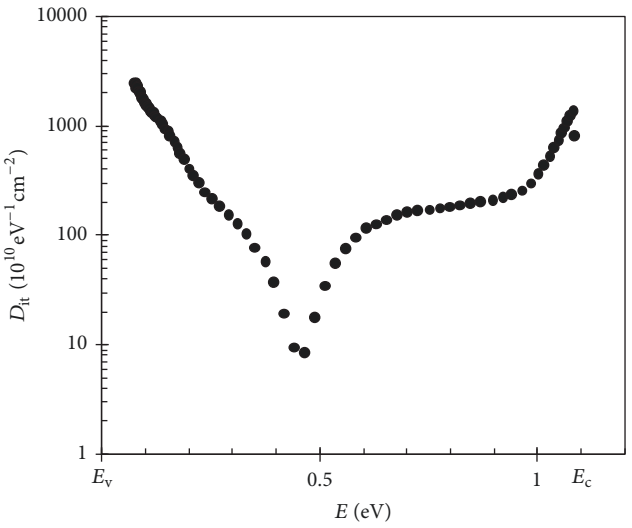

FIGURE 9: Distribution of densities of interface states (D_{it}) obtained by standard Terman method versus energy (E) through the silicon bandgap obtained on fresh samples.

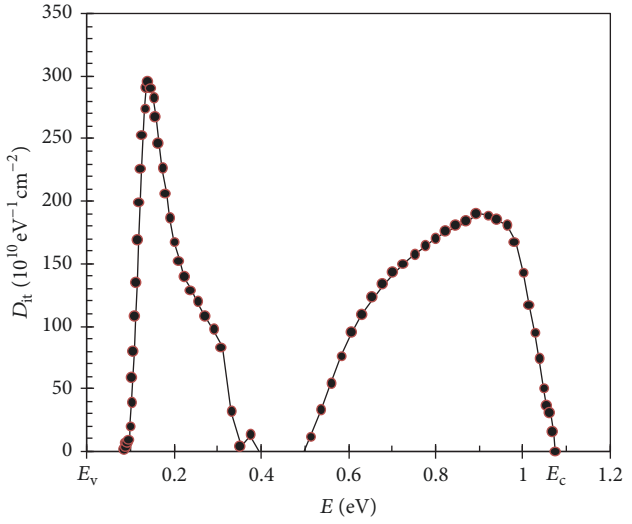

FIGURE 10: Distribution of densities of interface states (D_{it}) determined by modified Terman method versus energy (E) in silicon bandgap obtained on fresh samples.

in the silicon bandgap obtained on fresh samples is shown. Reference zero-energy level is set to the top of the valence band (E_v) of Si. Both positions of E_v and E_c (bottom of the conduction band) are labelled in Figure 9. Exponential tails towards band edges in our work [13] have been attributed to the effect of quantum charge in silicon substrate close to the interface with the dielectric. Using the method described in [13], quantum charge has been determined from the slopes of the curve for the stretch-out of the measured $C - V$ characteristic relative to the ideal one (ΔV_g) versus oxide voltage (V_{ox}). After extraction of the contribution of quantum charge, distribution of interface states displayed in Figure 10 is obtained. Two clear maxima are observed in the distribution.

In Figure 11 the experimental $C - V$ characteristic for fresh samples, along with the ideal low frequency $C - V$

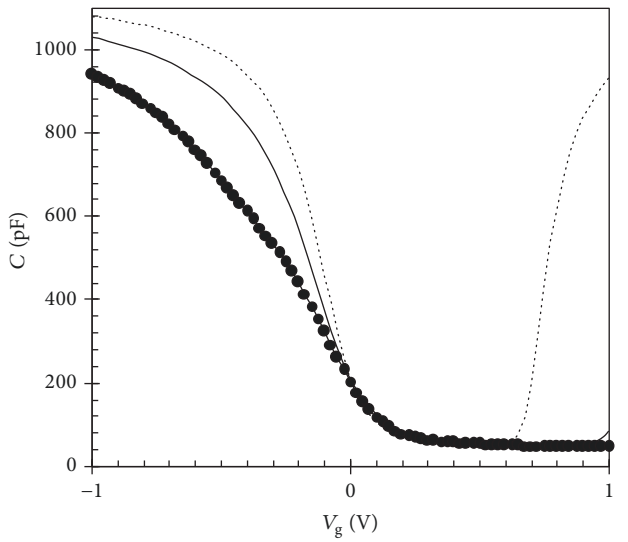

FIGURE 11: Experimental $C - V$ characteristic of fresh samples (filled circles), along with the ideal $C - V$ characteristic (dotted line) and corrected for quantum charge ideal $C - V$ characteristic (solid line).

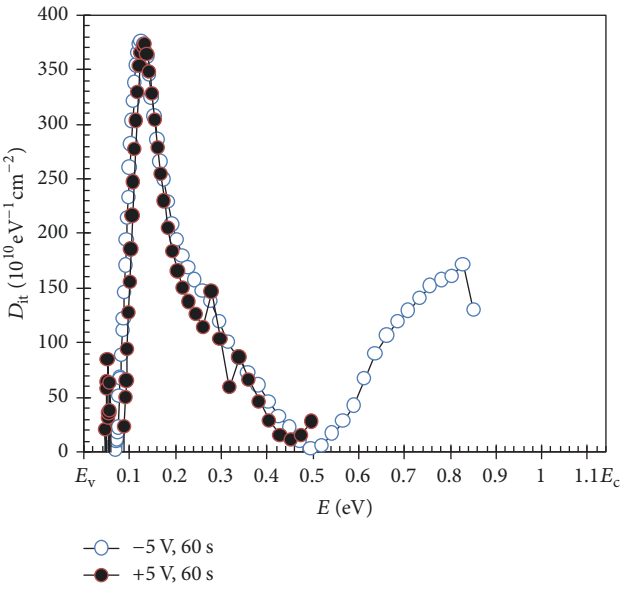

FIGURE 12: Distributions of densities of interface states (D_{it}) determined by modified Terman method versus energy (E) in silicon bandgap obtained on samples stressed under write (empty circles) and erase conditions (filled circles).

characteristic obtained by the standard method, is shown. In addition, an ideal $C - V$ characteristic corrected for quantum charge is presented. The corrected ideal curve is obtained by subtracting the voltage drop on the quantum charge layer from the measured gate voltage.

In Figure 12 distributions of densities of interface states (D_{it}) determined by modified Terman method versus energy (E) in silicon bandgap obtained on fresh and stressed samples during the write cycle are shown. It is seen that the distributions remain practically unchanged. Moreover, no visible changes are observed for further three write/erase cycles.

8. Conclusions

Proposed method for characterization of multilayered HfO_2/Al_2O_3 stacks for use in charge trapping flash memories in this work allows precise characterization of the electrical properties of the structures and the trapping properties.

In the particular case of multilayered HfO_2/Al_2O_3 stacks studied in this work, it is found that the used ratio of thicknesses of the homogeneous layers $d(HfO_2)/d(Al_2O_3)$ = 2.8 nm/1.0 nm provides excellent conditions for charge trapping and accumulation in the stack.

Based on a refined analysis, it is found that dominant part of the oxide charge is related to the accumulated charge, compared to the trapped charge. In order to improve further the charging properties of the stack, fabrication method for increasing the part due to the charge trapping is to be developed.

Under considered working conditions, no significant generation of interface states is observed. Therefore, no marked variations of the characteristics of the devices with the repeated write/erase cycling are expected. Long-term degradation is to be studied further, using the same methods as used in this work.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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