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Research Article

Unusual Operation of the Junction Transistor Based on Dynamical Behavior of Impurities

Roberto Baca Arroyo

Department of Electronics, National Polytechnic Institute, 07738 Mexico City, Mexico

Correspondence should be addressed to Roberto Baca Arroyo; rbaca02006@yahoo.com.mx

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The dynamical behavior of impurities into the silicon junction transistor has been studied using an empirical methodology to investigate its behavior knowing only the physical parameters of materials together with practical behavior of their passive components. The operating modes suggested with equations governing circuit performance are derived considering transient analysis. The relationship between material properties and equivalent circuit is discussed from a physical viewpoint. Theoretical solution of the equations yields a graphical response as approximation of the experimental results obtained from a proposed circuit built with an inductor and an NPN silicon MPSH10 transistor. Hence, the impurities-controlled electrical properties indicate that the observed unusual operation can be a good strategy to optimize signal processing in electronics.

1. Introduction

The most important solid-state device is the bipolar junction transistor (BJT) made from silicon. It was for three decades the active device of choice in the analog design of integrated circuits used in wide applicability in electronics, including computers, televisions, mobile phones, audio amplifiers, industrial control, and radio-frequency (RF) circuits of the wireless systems [1], but today the use of the BJT has declined in favor of the CMOS technology in the design of digital integrated circuits (ICs) [2–4]. Due to the low impedance at the base, high transconductance, and output resistance compared to MOS devices, the BJT is characterized as current-controlled current source useful to compute nonlinear functions by their logarithm dependence between base-emitter voltage V_{BE}, collector current I_C, and temperature, which recently has led to its integration into the CMOS-based architectures [5–8]. Currently, the BJT has been shown to be a viable option as transducer in electrochemical sensor, because it has significantly greater sensitivity and signal to noise ratio (SNR) and minor calibration requirements independent of voltages for operation, which implies that optimal measurements can be made over the entire sensing range, for example, to detect both $[Cl^-]$ ions and biomolecules in portable diagnostics [9, 10]. The last demonstrate that the junction transistor remains a competitive technology for adaptive multiple operation functions in comparison to the widely used MOS technology [11].

On the other hand, it is well known that an inductor can be electrically controlled under switching conditions and it can store energy into their bulk [12]. Hence, the total amount of energy stored can remain unchanged until the inductor exchanges energy dynamically with a capacitor [13]. Such inductor property can be employed to operate at the junction transistor under unusual behavior as a function of its physical action. Figure 1(a) shows a schematic diagram for an NPN junction transistor connected to two voltage sources, where conventionally forward-biasing the emitter-base junction and reverse-biasing the base-collector junction allow flow of the electrons from the emitter into the base, and between base and collector the majority of these electrons will diffuse as minority carries under electric field existing [14]. Hence, due to that junction transistor is combined by two junctions; currently the two built-in capacitances remain dependent on biasing condition, charge densities, and temperature [15]. Thus, taking into account the inductor action and junction transistor capacitances, the proposed circuit shown in Figure 1(b) inspired by the switching response of the inductor will determine the unusual biasing condition in the base-collector junction.

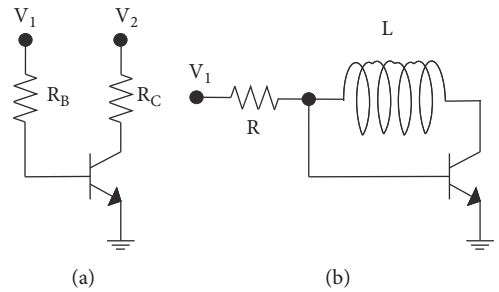

Figure 1: (a) Representation of the active mode in circuits. (b) Proposed circuit for the unusual operation.

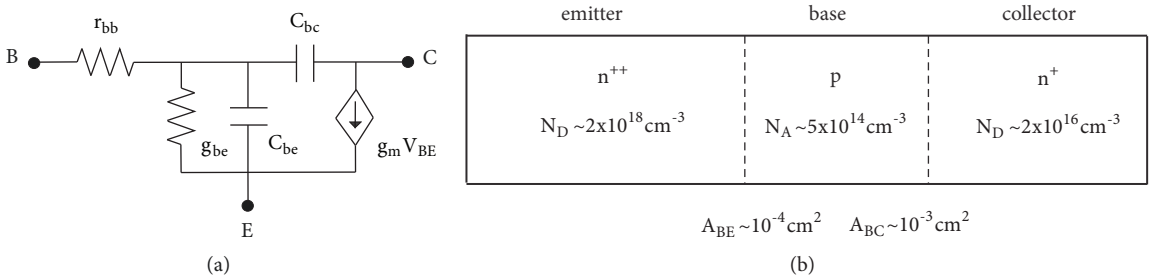

Figure 2: (a) Equivalent-circuit approximation for high frequencies. (b) Junction transistor model. Representative impurities concentration and cross-sectional areas are indicated.

In this work, impurities-controlled electrical properties at the base-collector junction will show how a silicon junction transistor (SJT) can add new functionalities based on switching cycles of the inductor polarity to design novel electronic circuits by combining both passive components and active devices (BJT).

2. Transient Analysis

Design of the electronic circuits has motivated us to investigate a manner that could serve as mutual analysis between physical structure and equivalent circuit of the several solid-state devices. Thus, a solution involving the number of parameters minimized to understand the physical phenomena into the SJT action, the hybrid-π equivalent circuit shown in Figure 2(a), will be used here as the basis for the study of the unusual operation based on dynamical behavior of impurities. Analytic formulation of the hybrid-π equivalent circuit proposed by Giacoletto has been based on measurements to evaluate physical parameters of the materials as well as theoretical studies which are predicted to obtain the answers desired for the design of SJTs without recourse of their previous building [16]. To validate utility of the equivalent circuit of Figure 2(a), the maximum frequency for the junction transistor at which their amplification is unity, being dependent somewhat upon the DC collector voltage, was assumed by Giacoletto as

$$f = \frac{1}{4\pi}\left(\frac{g_m}{r_{bb}C_{bc}C_{be}}\right)^{1/2} \quad (1)$$

where r_{bb} is the base-lead resistance which is function of the junction transistor geometry and inversely proportional to the conductivity of the base region, C_{bc} is the space-charge capacitance at the base-collector junction, and C_{be} is the space-charge capacitance at the base-emitter junction, while transconductance g_m can be empirically defined as $g_m \approx I_E\phi^{-1}$ with $\phi = e^{-1}kT\ln(N_DN_An_i^{-2})$ as the built-in potential at the junction, where k is the Boltzmann constant, $8.62 \times 10^{-5}eV/{}^oK$, T the temperature, N_D the donors density, N_A the acceptors density, n_i the density at intrinsic Fermi level, and I_E the DC emitter current [17].

On the other hand, as the complexity in the analysis of p-n junctions involves equations using boundary conditions, here we introduce a physical approximation derived from Poisson's equation describing the potential function $\phi(x)$ into the space-charge layers when charge densities for both electrons $n(x)$ and holes $p(x)$ vary by Boltzmann's law.

Using these facts for the analysis in both emitter-base junction and base-collector junction, the following properties at each junction must be taken into account:

(a) All N_D and N_A are ionizing and the condition for $\phi(x)$ is satisfied as $\phi_+(x)$ in the range $0 < x < x^+$ and as $\phi_-(x)$ in the range $-x^- < x < 0$, respectively. Hence, the concentration of the carries will vary exponentially as a function of $\phi(x)$ and, at the large distances from the junction, will decrease at negligible values.

(b) As the electric field must be continuous into the three regions, emitter, base, and collector, let the ratio $N_Dx^+ = N_Ax^-$ find space-charge widths x^+ and x^- between n and p regions [14], being estimated by Poisson's equation as

$$x^+ = \sqrt{\frac{K\varepsilon_o(\phi \pm V)}{2\pi e}\cdot\frac{N_A}{N_D(N_D+N_A)}} \quad (2)$$

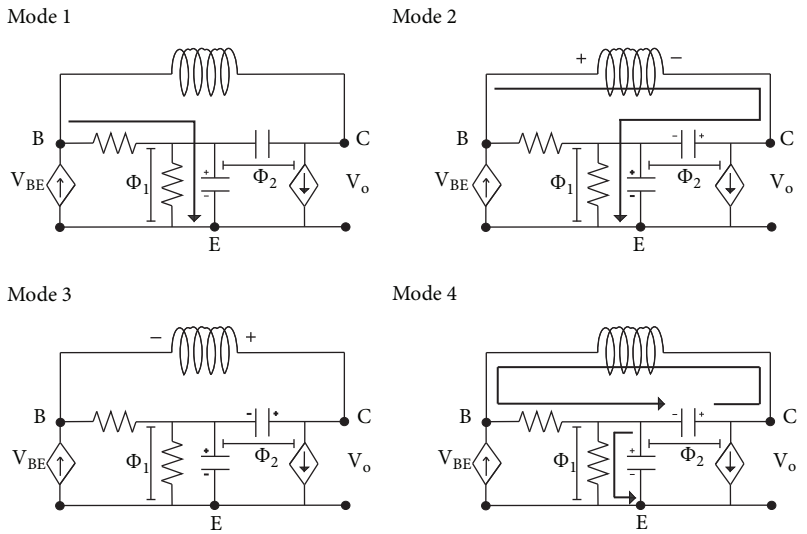

FIGURE 3: Operation modes for the proposed circuit of Figure 1(b) as a function of the transient current paths and potentials actuating on transition junction capacitances.

$$x^{-} = \sqrt{\frac{K\varepsilon_o(\phi \pm V)}{2\pi e} \cdot \frac{N_D}{N_A(N_D + N_A)}} \tag{3}$$

where $\varepsilon_o = 8.86 \times 10^{-14}\ F/cm$ is the permittivity at the free space and K is the dielectric constant, while the polarity (+) for V into (2) and (3) is used under reverse-biasing condition and at the forward-biasing condition polarity (-) is used.

It is known that, at higher frequencies, the increase in the electric field on both n and p regions will bring a reduction in the space-charge width. As a result, the presence of voltage across the base-collector junction produces change in the space-charge width proportional to displacement of the carries [18], where such effect gives rise to transition junction capacitances defined by

$$C_{be} = \frac{K\varepsilon_o}{x_{BE}} A_{BE} \tag{4}$$

$$C_{bc} = \frac{K\varepsilon_o}{x_{BC}} A_{BC} \tag{5}$$

where x_{BE} and x_{BC} are the effective junction widths and A_{BE} and A_{BC} are the cross-sectional areas at the junctions base-emitter and base-collector, respectively

The variation of the space-charge capacitances under applied voltage will depend upon impurities distribution $dQ = eN_D x^{+} = eN_A x^{-}$ in the locality of the base-emitter junction, where their density is much greater than that at the base-collector junction, where the input admittance will be r_{bb} in series with a parallel combination of g_{be} with C_{be} (see Figure 2(a)), and the parameter g_{be} increases approximately linearly with I_E, being constant with the operating frequency at the biasing condition empirically given by $g_{be} \approx V_{CE}(V_{BE})^{-1} g_m$, where V_{CE} and V_{BE} are voltages under ON characteristics [17].

2.1. Operating Modes for the Proposed Circuit. It was demonstrated that the junction transistor operating at higher frequencies has a conductive component and a susceptive component as admittance parameters, which indicate that a transient analysis can be done because the approximation based on susceptive components can be developed simply from the conductive components by applying considerations of the transit time by carrier [16]. Susceptive parameters consist in part of space-charge capacitances and other diffusion contributions which are collector current dependent and can be considered to raise the transit time, $t \approx W_b^2/2D_n$. Taking into account the fact that there is a phase difference between an applied V_{BE} and the resulting current I_C, an angular frequency ω with a phase angle corresponding to one transit time through the base width W_b is $e^{\pm j\omega t} = \cos(\omega t) \pm j\sin(\omega t)$, where as long as ω is valid, higher frequencies are indicated by the inequality $\omega t \ll 1$, which is used to specify the valid frequency range required for the diffusion D_n of an incremental change of minority carries through W_b [18].

Hence, it is instructive to analyze the transient current paths into the four basic operation modes described by state equations [19]. Such analysis will reveal the electrical parameters into the SJT whose nominal junction transistor model shown in Figure 2(b) is used here to give a qualitative idea of the physics involved to operate the circuit of Figure 1(b) [14].

The detailed description of each mode is given below.

Mode 1. At the beginning, emitter-base junction is turned on with V_{BE} usually above 650 mV at room temperature. In this mode, electrons are injected from n^{++} emitter region into p base region, and holes are injected from p base region into n^{++} emitter region. Thus, C_{be} is initially loaded at built-in potential ϕ_1 (see Figure 3). The equation governing this operation mode is

$$C_{be}\frac{d\phi_1}{dt} + g_{be}\phi_1 = \frac{V_{BE} - \phi_1}{r_{bb}}. \tag{6}$$

Table 1: Physical parameters for the NPN silicon MPSH10 transistor.

Parameter	$I_C = 30mA$ $V_{BE} = 0.65V$	$I_C = 60mA$ $V_{BE} = 0.75V$	$I_C = 90mA$ $V_{BE} = 0.85V$
r_{bb}	9.35 Ω	17.25 Ω	23.02 Ω
g_m	0.039 Ω^{-1}	0.079 Ω^{-1}	0.119 Ω^{-1}
g_{be}	0.020 Ω^{-1}	0.041 Ω^{-1}	0.062 Ω^{-1}
x_{BE}^{+}	1.34 x10^{-8} cm	1.39 x10^{-8} cm	1.43 x10^{-8} cm
x_{BE}^{-}	5.38 x10^{-5} cm	5.57 x10^{-5} cm	5.75 x10^{-5} cm
x_{BC}^{+}	7.82 x10^{-7} cm	6.97 x10^{-7} cm	5.99 x10^{-7} cm
x_{BC}^{-}	3.12 x10^{-5} cm	2.78 x10^{-5} cm	2.39 x10^{-5} cm
C_{be}	7.70 nF	7.44 nF	7.20 nF
C_{bc} (±)	1.32 nF	1.48 nF	1.73 nF
C_{bc} (∓)	33.14 pF	37.18 pF	43.21 pF
$n\tau$	12.04 ns	18.62 ns	40.68 ns
D_n	0.934 cm^2s^{-1}	0.604 cm^2s^{-1}	0.276 cm^2s^{-1}
μ_n	35.92 $cm^2V^{-1}s^{-1}$	23.23 $cm^2V^{-1}s^{-1}$	10.63 $cm^2V^{-1}s^{-1}$

Mode 2. After a time delay proportional to $\tau \approx (g_{be}(C_{be})^{-1} + (r_{bb}C_{be})^{-1})^{-1}$ and when base-collector junction is reverse-biased, current flow through the inductor occurs with polarity shown in Figure 3. In this mode, electrons from emitter-base junction are swept away by electric field into the base-collector junction, and holes are drifted to the emitter-base junction. Thus, C_{bc} starts to be loaded at built-in potential ϕ_2 of base-collector junction, where the transient displacement of charge carries (electrons and holes) through both emitter-base junction and base-collector junction occur as a function of the inductor polarity (±). A potential ϕ^+ proportional to the output voltage V_o is dynamically built-up between both C_{be} and C_{bc} (see Figure 3). The equation describing this operation mode is

$$C_{bc}\frac{d\phi_2}{dt} = g_{be}\phi_1 + C_{be}\frac{d\phi_1}{dt}. \tag{7}$$

Mode 3. The current flow through C_{bc} is now negligible because space-charge width of the base-collector junction has completed their final value and inductor behaves as short circuit after time delay equivalent to $n\tau$, where n depends on time response (see the appendix). The inductor polarity changes as shown in Figure 3 and output voltage V_o has maximum magnitude, being proportional to the potential ϕ^+.

Mode 4. A short-circuit state of the inductor occurs during the time delay; the following effects are taken into account: (a) Space-charge width in the base-collector junction is reversed because the inductor polarity (∓) forces unloading of C_{bc} through r_{bb} as shown in Figure 3. (b) As base-collector junction is like the reverse-biased junction during this operation mode, the potential ϕ^- proportional to the output voltage V_o reduces. (c) The built-in potential ϕ_1 is decreasing until turning off of the emitter-base junction with V_{BE} below 650 mV and the recombination process into the base occurs. The equations governing this operation mode are

$$C_{be}\frac{d\phi_1^*}{dt} = -g_{be}\phi_1^* \tag{8}$$

$$\frac{\phi_1^* - V_{BE}}{r_{bb}} = C_{bc}\frac{d\phi_2^*}{dt}. \tag{9}$$

3. Results and Discussion

To give an example of the unusual operation in the SJT, the NPN silicon MPSH10 transistor has been chosen, operating approximately under the small-signal properties in accordance with the junction transistor model of Figure 2(b). First, solving (1) to (5), the equivalent parameters exhibiting the same properties as the physical device under suggested biasing conditions are computed in Table 1. Second, the graphical response of the operation modes of Figure 3 is done by solving (6) to (9).

The physical parameters included in Table 1 have been computed by means of the following stages: (a) Using N_D, N_A, A_{BE}, and A_{BC} from Figure 2(b) the built-in potentials Φ_1 and Φ_2 of each junction indicated in Figure 3 are calculated. (b) By means of (2) and (3) and as a silicon transistor is used, $K = 11.7$, and then the space-charge widths x_{BE}^{+} and x_{BC}^{+} are obtained under forward bias while x_{BE}^{-} and x_{BC}^{-} under reverse bias conditions. (c) After that, transition junction capacitances C_{be} and C_{bc} are obtained by (4) and (5), where to calculate C_{be} only x_{BE}^{+} was used, whereas at forward bias $C_{bc}(\pm)$ is proportional to x_{BC}^{+} and $C_{bc}(\mp)$ under reverse bias proportional to x_{BC}^{-}. (d) Finally, knowing I_C and V_{BE}, as well as evaluating the empirical expressions $g_m \approx I_E\phi^{-1}$ and $g_{be} \approx V_{CE}(V_{BE})^{-1}g_m$, r_{bb} is obtained from (1) for $f = 650MHz$ as maximum frequency for the NPN silicon MPSH10 transistor.

3.1. Graphical Response of the SJT under Transient Operation. To know the graphical response of the proposed circuit

Table 2: Operation parameters for the proposed circuit of Figure 1(b).

Parameter	$I_C = 30mA$ $V_{BE} = 0.65V$	$I_C = 60mA$ $V_{BE} = 0.75V$	$I_C = 90mA$ $V_{BE} = 0.85V$
$L_1 = 26.3nH$			
2 turns			
V_o	0.27 V	0.72 V	0.98 V
f_o	30.75 MHz	28.97 MHz	28.25 MHz
t_p	18 ns	14 ns	14 ns
D_p	7.62 cm^2s^{-1}	9.79 cm^2s^{-1}	9.79 cm^2s^{-1}
μ_p	293.07 $cm^2V^{-1}s^{-1}$	376.53 $cm^2V^{-1}s^{-1}$	376.53 $cm^2V^{-1}s^{-1}$
$L_2 = 164.4nH$			
5 turns			
V_o	0.46 V	0.89 V	0.94 V
f_o	27.17 MHz	24.04 MHz	22.22 MHz
t_p	12 ns	10 ns (1) 8 ns (2)	10 ns (1) 12 ns (2)
D_p	11.43 cm^2s^{-1}	13.71 cm^2s^{-1} (1) 17.14 cm^2s^{-1} (2)	13.71 cm^2s^{-1} (1) 11.43 cm^2s^{-1} (2)
μ_p	439.72 $cm^2V^{-1}s^{-1}$	527.67 $cm^2V^{-1}s^{-1}$ (1) 659.59 $cm^2V^{-1}s^{-1}$ (2)	527.67 $cm^2V^{-1}s^{-1}$ (1) 439.72 $cm^2V^{-1}s^{-1}$ (2)
$L_3 = 532.6nH$			
9 turns			
V_o	0.98 V	1.11 V	1.24 V
f_o	22.83 MHz	14.27 MHz	12.55 MHz
t_p	20 ns	10 ns (1) 20 ns (2)	15 ns (1) 25 ns (2)
D_p	6.85 cm^2s^{-1}	13.71 cm^2s^{-1} (1) 6.85 cm^2s^{-1} (2)	9.14 cm^2s^{-1} (1) 5.48 cm^2s^{-1} (2)
μ_p	263.83 $cm^2V^{-1}s^{-1}$	527.67 $cm^2V^{-1}s^{-1}$ (1) 263.83 $cm^2V^{-1}s^{-1}$ (2)	351.78 $cm^2V^{-1}s^{-1}$ (1) 211.06 $cm^2V^{-1}s^{-1}$ (2)

of Figure 1(b), the solution for (6) to (9) governing the operating modes of Figure 3 is derived in the appendix. Also, the inductor action shown in Figure 4 must be transitorily analyzed together with the hybrid-π equivalent circuit of Figure 2(a), where the equation describing this mode is

$$\phi_2 = g_m L \frac{d\phi_1}{dt}. \tag{10}$$

To understand the key role of the inductor in Figure 1(b), three inductors were chosen (see Table 2) as a function of the resonance behavior in the LC circuit operating at high frequencies between C_{bc} included in Table 1 and L [13]. Using solution for ϕ_1 (see the appendix) during *Modes* 1 and 2, the physical behavior of the inductor is computed through (10). Practical inductors were built with single winding using AWG # 20 on a cylindrical tube having length equal to 1.5 cm and diameter of 1 cm.

Figures 5(a)–7(a) show the theoretical graphical response of the dynamical behavior of ϕ^+ and ϕ^- for transistor action in comparison with ϕ_2 for inductor action during *Modes* 1 and 2, where ionized impurities N^+_{DE} at the emitter region, N^-_{AB} at the base region, and N^+_{DC} at the collector region are

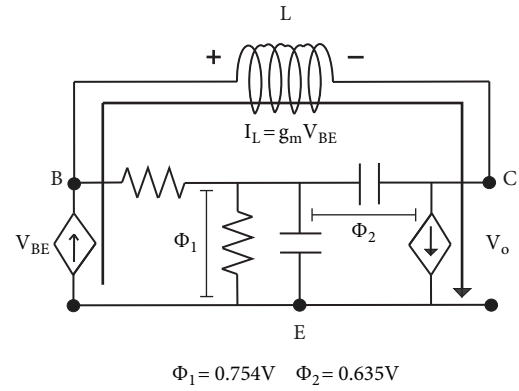

Figure 4: Equivalent-circuit approximation for inductor action. Built-in potentials at each junction are also indicated.

responsible parameters of the carriers conduction involved at each SJT region exhibiting transient behavior, which has been evaluated using $\phi = e^{-1}kT\ln(N^+_D N^-_A n_i^{-2})$ proportional at the potential ϕ^+ and ϕ^-. The time delay τ for which graphics

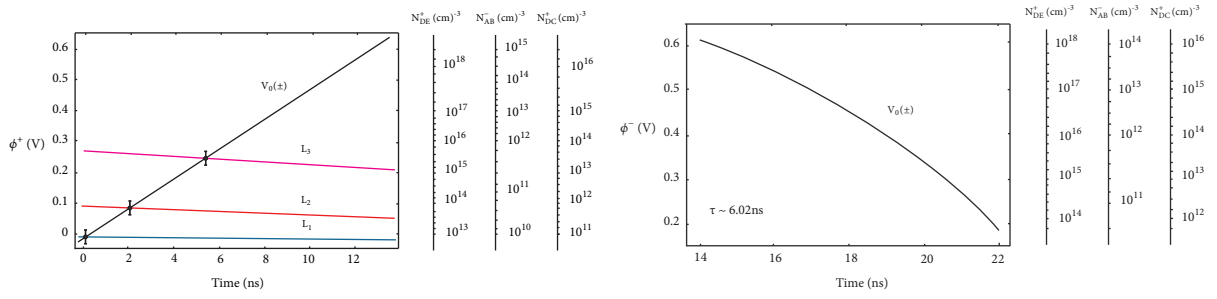

FIGURE 5: Dynamical behavior of the transistor action at $I_C = 30mA$ and $V_{BE} = 0.65V$.

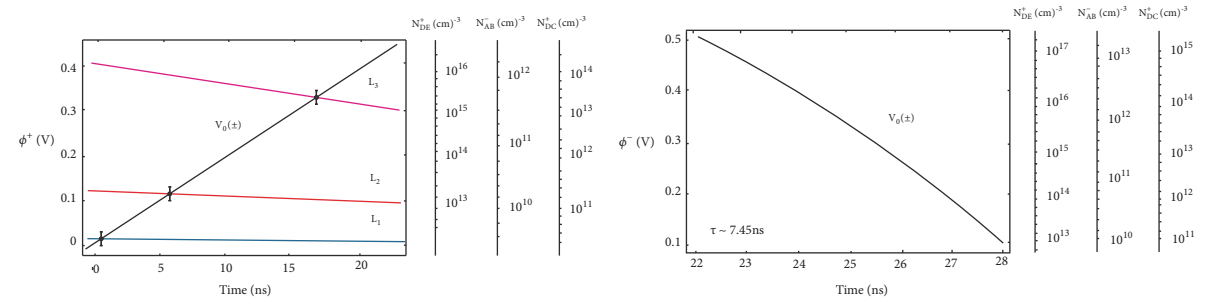

FIGURE 6: Dynamical behavior of the transistor action at $I_C = 60mA$ and $V_{BE} = 0.75V$.

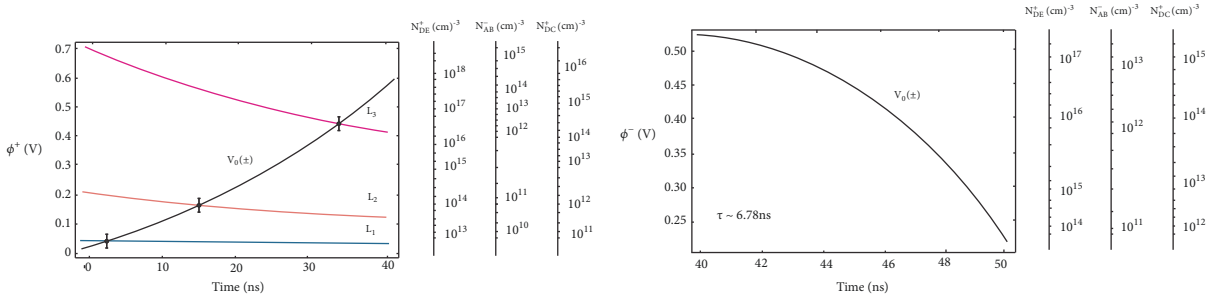

FIGURE 7: Dynamical behavior of the transistor action at $I_C = 90mA$ and $V_{BE} = 0.85V$.

from Figures 5(b)–7(b) were computed is specified, being proportional to the minority-carrier lifetime. Following, as in *Modes* 3 and 4, the inductor polarity switch, the transient transistor action is corresponding at its conventional action, where base-collector junction is reverse-biased and ionized impurities will decrease as a function of $t \approx W_b^2/2D_n$.

3.2. Physical Behavior of the SJT under Transient Operation. To validate that a SJT can operate under unusual operation, the proposed circuit was built. Figures 8(a)–8(c) show the resulting alternating voltage waveforms at the output. To ensure biasing conditions a resistor R = 100Ω was employed. A digital storage oscilloscope, Tektronix TDS1002B, was used for registering of the waveforms. The operating physical parameters under several test conditions are given in Table 2. Those parameters are output voltage V_o, operating frequency f_o, hole transient time t_p, and both mobility μ_p and diffusivity D_p of the hole carriers injected during *Modes* 1 and 2 from base region to collector region (see Figure 9(a)).

Supposing that low level injection of hole carries across the base-collector junction occurs in a thickness identical to W_b for displacement of the electron carries when the limit of ϕ changes in response to an abrupt alteration in the N_A profile obeying at the Debye length L_D, then it must be considered that $W_b < L_D$, with $W_b = 1.5\mu m$ being nominal base width for the junction transistor model of Figure 2(b) [20]. Hence, a diffusion coefficient $D_n = D_{0p}$ that depends on both interatomic distance and atomic frequency of vibration can be estimated using $t_p \approx W_b^2/2D_{0p}$, but, as carriers conduction in the SJT is sensitive to changes in the bias voltages and temperature, the mobility under transient behavior during *Modes* 1 and 2 follows at the Arrhenius dependence

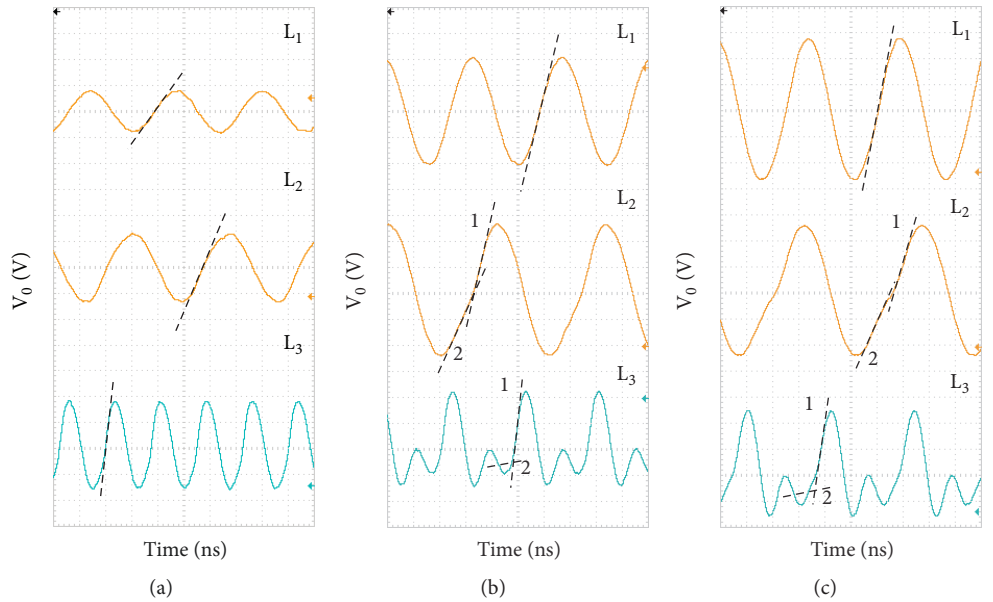

FIGURE 8: Output voltage waveforms from the proposed circuit of Figure 1(b). (a) Under bias at $I_C = 30mA$. (b) Under bias at $I_C = 60mA$. (c) Under bias at $I_C = 90mA$.

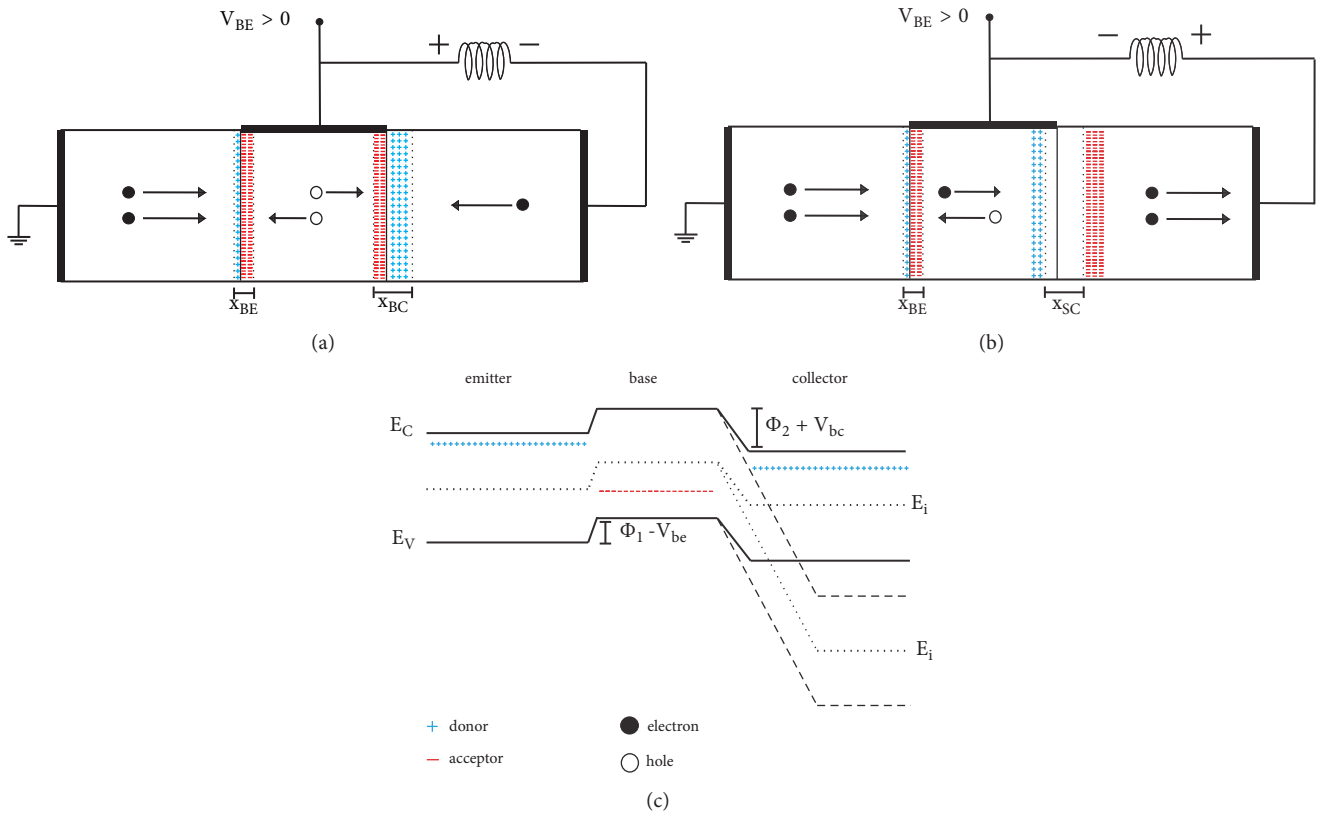

FIGURE 9: Transistor action dependent on ionized impurities. (a) Displacement of the charge carries at inductor polarity (±). (b) Displacement of the charge carries at inductor polarity (∓). (c) Action in the energy band diagram.

$\mu_p = e(kT)^{-1}D_p$ [21], where D_p is the diffusivity of hole carries related to $D_{0p} \approx D_p \exp(-\phi_a/kT)$ with $\phi_a \approx 0.065eV$ as activation energy due to thermally generated electron-hole pairs when the temperature into the SJT increases because of the large currents being used inside base-collector junction during *Modes* 1 and 2 (see Table 1) [22]. Consequently, t_p was measured alongside each slope (1) and (2) specified in Figures 8(b) and 8(c), and then the rest of the physical parameters responsible for the transistor action such as D_p and μ_p were calculated at room temperature (see Table 2).

The evolution of ϕ^+ equivalent to $V_o(\pm)$ during *Modes* 1 and 2 is compared with the ϕ_2 generated for each inductor chosen in Table 2, where intersection dots from Figures 5(a), 6(a), and 7(a) indicate the corresponding amount of the ionized impurities under transient operation. It has been exhibited that the $V_o(\pm)$ is linear in Figure 5(a) for each curve of ϕ_2 with ϕ^+at low level of $N^+_{DE} \sim 10^{15}\text{cm}^{-3}$, $N^-_{AB} \sim 10^{11}\text{cm}^{-3}$, and $N^+_{DC} \sim 10^{13}\text{cm}^{-3}$, respectively. In Figure 6(a), $V_o(\pm)$ continues to be quasi-linear, and slight increase of the ionized impurities can occur.

Instead, a minor nonlinearity of $V_o(\pm)$ with larger amount of $N^+_{DE} \sim 10^{17}\text{cm}^{-3}$, $N^-_{AB} \sim 10^{13}\text{cm}^{-3}$, and $N^+_{DC} \sim 10^{15}\text{cm}^{-3}$ is observed, which means that displacement of the charge carries through the junctions x_{BE} and x_{BC} could be perturbed by ionization processes into the base region [14, 16]. However, when I_C and V_{BE} increase as biasing parameters, nonlinearity of $V_o(\pm)$ in Figure 7(a) increases, which means that densities of the ionized impurities (N^+_{DE}, N^-_{AB}, and N^+_{DC}) can be unevenly distributed into the base region.

Thus, the energy band diagram of Figure 9(c) for the transistor action of Figure 9(a) indicates that potential distribution at the emitter-base junction is forward-biased with voltage $V_{BE} > 0$ lowering the built-in potential ϕ_1 and narrowing its space-charge width, while in the base-collector junction forward-biased at $V_{BE} > 0$, injection of the hole carries rises when the position of the Fermi level equivalent to ϕ^+ is around $0.2eV$ within the forbidden gap as a function of temperature for N_{AB} into base region which allows the two Fermi levels corresponding to donors and acceptors to be closeness. However, under this linear regime (Ohmic behavior), the magnitude of the base current tends to increase slightly (small conduction of hole carries) due to the negligible electric field through the base region. Hence, the density of the minority carries will be much smaller than the density of majority carries and x_{BC} reduces as the electric field increases.

The solution of (8) and (9) corresponding to the *Modes* 3 and 4 gives the evolution of ϕ^- equivalent to $V_o(\mp)$ in Figures 5(b), 6(b), and 7(b) when base-collector junction is reverse-biased as a function of time delay $n\tau$ being proportional to $W_b^2/2D_n$, where parameters such as r_{bb}, g_{be}, C_{be}, and C_{bc} are responsible for slower displacement of charge carries as a function of the theoretical parameters D_n and μ_n listed in Table 1. Besides, recombination into the base region limits diffusion of electron carries, which may be the result of the nonlinearity of $V_o(\mp)$ during inductor polarity ($\mp$) in Figure 7(b). Therefore, the energy band diagram of Figure 9(c) under conventional reverse bias, denoted by dotted lines, indicates that the electrons and holes through the base-collector junction occur at voltage $V_{BC} < 0$, where the depletion layer x_{SC} is widening (see Figure 9(b)).

Under transient operating conditions of Figure 1(b), at $\phi^+ \geq 0.2eV$ the amount of N_{AB} increases until achieving their saturation and x_{BC} decreases at minimum. Therefore, the electric field maximizes and current flow upon the base-collector junction can produce ionization runaway at low collector-emitter voltage, producing nonlinearities in the waveforms of Figures 8(b) and 8(c), where coexistence of both linear regime and ionized-impurities-limited regime happens [22, 23]. This nonlinearity may be the result of irregular distribution of ionized impurities near the metallurgical base-collector junction when holes injection is limited by D_p and μ_p responsible for the narrowing of W_b and presence of two diffusivities corresponding to each conduction regime.

Likewise, when inductor chosen is $L \geq 200nH$ at forward bias, the governing mechanism for the conduction in base-collector junction will be dependent on energy storage into the inductor and space-charge limited current (SCLC) [24], where x_{BC} increases slowly at $\phi^+ \geq 0.2eV$ under constant electric field, increasing ionized-impurities-limited regime and depleting linear regime. On the other hand, due to the lower diffusion of electron carries under reverse bias when inductor polarity changes at ($\mp$) (see Figure 9(b)), both conduction regimes are negligible and exhaustion of majority carries arises.

For stable behavior of the proposed circuit, the following must be taken into account: (a) Ionized impurities will increase linearly as a function of time when $\phi^+ < \phi_1$ and $\phi^- < \phi_1$ at the base-emitter junction, as well as $\phi^+ < \phi_2$ and $\phi^- < \phi_2$ at the base-collector junction. (b) Stable concentration of ionized impurities will occur with $C_{bc}(D_p, \mu_p)$ as diffusion capacitance when $L \leq 200\text{nH}$ and μ_p is lower than 450 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ when inductor polarity ($\pm$) takes place. (c) $\mu_n < \mu_p$ and $D_n < D_p$ must be satisfied to operate the SJT into their linear regime as shown in Figures 8(a), 8(b), and 8(c) for L_1 and L_2.

4. Conclusions

In this work, electrical response of an inductor under switching conditions dependent on transistor action and their capability to exchange energy has been taken into account together with the physical parameters involved to achieve the unusual operation based on dynamical behavior of impurities. An empirical model to investigate the physics of a SJT knowing only the physical parameters of the materials has been studied using an equivalent-circuit approximation. As example, the NPN silicon MPSH10 transistor has been chosen to validate the theoretical model ensuring functionally stable as a function of their impurities-controlled electrical properties. Good agreement is found between theory and measurements. Modeling physical parameters for existing semiconductor technologies is at least needed to propose and design novel electronic circuits with adaptive operation characteristics and performance enhanced. Interest in discovering unusual properties is key piece to continue

trends on optimized signal processing to the next generation of electronics.

Appendix

Solution of the Governing Equations for Transistor Action Model

Using the well-known analytical method to solve second-order linear differential equations, the solution of (6) can be written as below.

$$\phi_1 = C_1 + C_2 e^{-t/\tau} \tag{A.1}$$

The time delay τ corresponds to $(g_{be}(C_{be})^{-1} + (r_{bb}C_{be})^{-1})^{-1}$ and constants C_1 and C_2 are determined at initial conditions $t = 0$ and $\phi_1(0) = 0$ where the valid solution for (A.1) with $\Phi_1 = 0.754V$ as maximum built-in potential can be expressed as below.

$$\phi_1 = \Phi_1 \left(1 - e^{-t/\tau}\right) \tag{A.2}$$

For (7), the built-in potential ϕ_2 must be solved as a function of ϕ_1 from the following equation.

$$\phi_2 = \frac{g_{be}}{C_{bc}} \int_0^t \phi_1 dt + \frac{C_{be}}{C_{bc}} \phi_1 \tag{A.3}$$

Substituting (A.2) into (A.3), the suitable solution for (A.3) is determined as below.

$$\phi_2 = \Phi_1 \cdot \frac{g_{be}}{C_{bc}} \left[\left(t + \tau \left(e^{-t/\tau} - 1\right)\right) + \frac{C_{be}}{g_{be}} \left(1 - e^{-t/r_{bb}C_{be}}\right) \right] \tag{A.4}$$

To find ϕ_2 in accordance with the operation *Mode 2*, it must be considered that the base-collector capacitance C_{bc} will be equivalent to the forward-biased capacitance at the base-collector junction (see Table 1). Then, the behavior of the circuit of Figure 1(b) can be confirmed as a function of the potential $\phi^+ = \phi_2 - \phi_1$ valid for the *Modes* 1 and 2 at the potential values $\phi^+ < \Phi_1$.

At the transient state in *Mode 3*, that is, at $t = 4\tau$ approximately, it can be supposed that the potential ϕ^+ is equivalent to Φ_1; therefore, now (8) can be solved as below.

$$\phi_1^* = C_1 e^{-(g_{be}/C_{be})t} \tag{A.5}$$

Again, the constant C_1 is determined at initial conditions $t = 0$ and $\phi_1^*(0) = 0$ where the valid solution for (A.5) with $\Phi_1 = 0.754V$ as maximum built-in potential can be confirmed as below.

$$\phi_1^* = \Phi_1 e^{-(g_{be}/C_{be})t} \tag{A.6}$$

Equation (9) must be solved as a function of ϕ_1^*. Substituting (A.6) into (9), the useful solution for ϕ_2^*, taking into account time delay $n\tau$ with $n = 2$, $n = 2.5$, and $n = 6$ for each one biasing condition established in Table 1 to adjust the time response during the dynamical-exchange energy into a LC circuit, can be written as below.

$$\phi_2^* = -\frac{\Phi_1}{r_{bb}C_{bc}^*} \left[(t - n\tau) - \frac{C_{be}}{g_{be}} \left(1 - e^{-(g_{be}/C_{be})(t-n\tau)}\right) \right] \tag{A.7}$$

Again, to find ϕ_2^* in accordance with the operation *Mode 4*, it must be considered that the base-collector capacitance C_{bc}^* will be equivalent to the reverse-biased capacitance at the base-collector junction (see Table 1). Then, the behavior of the circuit of Figure 1(b) can be confirmed as a function of the potential $\phi^- = \phi_1^* - \phi_2^*$ valid for the *Modes* 3 and 4 with potential values $\phi^- < \Phi_1$.

Finally, using (A.2) and (A.4), (10) can be validated to demonstrate the high-frequency response of the proposed circuit of Figure 1(b) as function of the inductor value.

Data Availability

All the manuscript is legible for the readers, because it demonstrates, through replicable experimental results, unusual operation principles for the junction transistor. Furthermore, the following has been specified in the manuscript: the graphical response of the equations governing circuit performance from operation modes suggested at each stage with details about the equations solutions, with an appendix of the conditions to solve those equations, supporting the conclusions of the study. Finally, the intention of the author is to motivate other researchers to explore new research routes using similar methodology to that proposed here. Data are also available from the corresponding author upon request.

Conflicts of Interest

The author declares that there are no conflicts of interest regarding the publication of this paper.

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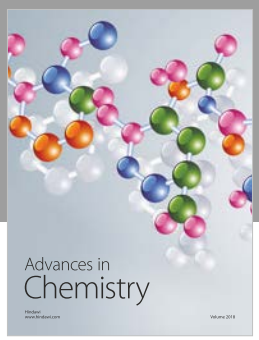

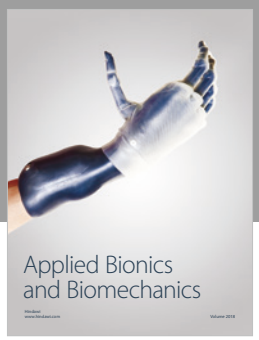

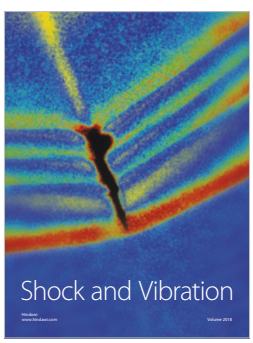

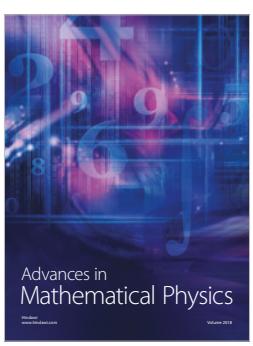

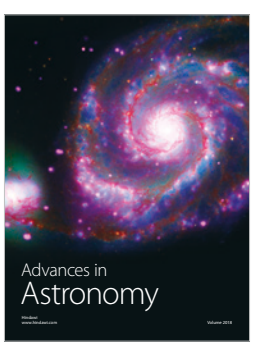

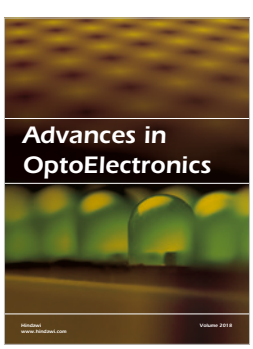

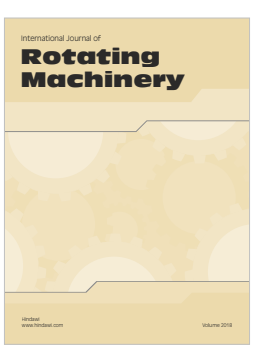

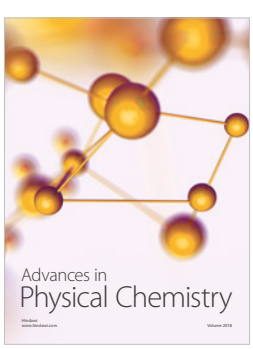

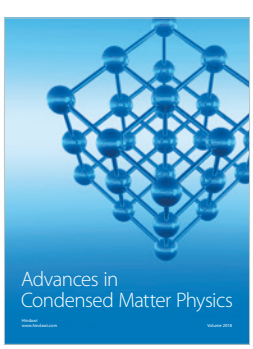

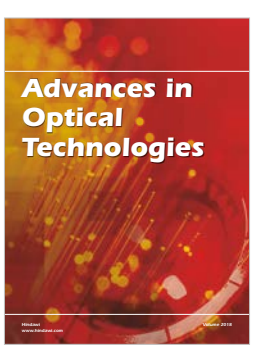

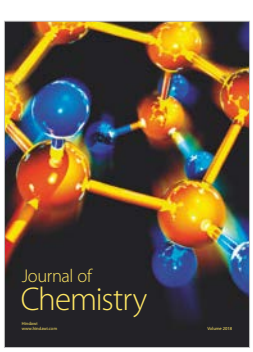

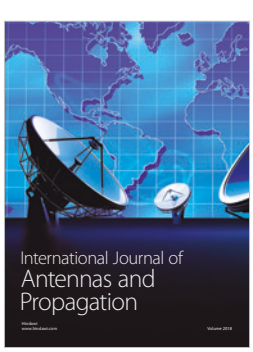

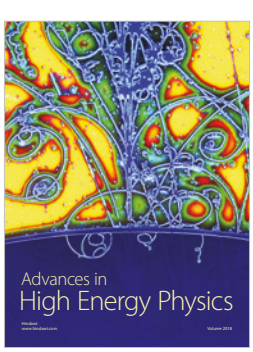

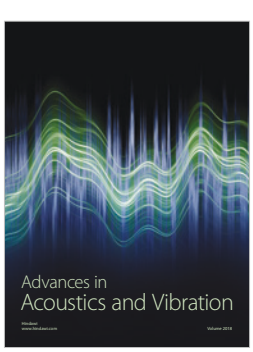

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