Hindawi
Advances in Condensed Matter Physics
Volume 2018, Article ID 5483756, 6 pages
https://doi.org/10.1155/2018/5483756

Research Article

The TDDB Characteristics of Ultra-Thin Gate Oxide MOS Capacitors under Constant Voltage Stress and Substrate Hot-Carrier Injection

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Received 2 November 2017; Accepted 16 April 2018; Published 20 May 2018

Academic Editor: Faheem. K. Butt

The breakdown characteristics of ultra-thin gate oxide MOS capacitors fabricated in 65 nm CMOS technology under constant voltage stress and substrate hot-carrier injection are investigated. Compared to normal thick gate oxide, the degradation mechanism of time-dependent dielectric breakdown (TDDB) of ultra-thin gate oxide is found to be different. It is found that the gate current (I_g) of ultra-thin gate oxide MOS capacitor is more likely to be induced not only by Fowler-Nordheim (F-N) tunneling electrons, but also by electrons surmounting barrier and penetrating electrons in the condition of constant voltage stress. Moreover it is shown that the time to breakdown (t_{bd}) under substrate hot-carrier injection is far less than that under constant voltage stress when the failure criterion is defined as a hard breakdown according to the experimental results. The TDDB mechanism of ultra-thin gate oxide will be detailed. The differences in TDDB characteristics of MOS capacitors induced by constant voltage stress and substrate hot-carrier injection will be also discussed.

1. Introduction

With the aggressive scaling of the feature size of MOS devices, the gate oxide has had a continuous thinning trend for the past 30 years. However, the power supply voltage has not scaled down nearly. This results in a sharp increase in the electric field on the gate oxide of MOS device and further increase of gate leakage current. Thus there have been increasing concerns about the reliability of SiO_2 gate dielectric films [1–7]. In particular, the thickness of SiO_2 gate dielectric films reduces to 1~2 nm in the new generation technologies and that is in close proximity to a fundamental limit of 0.7 nm on the thinnest which is ascribed to Si/SiO_2 interface roughness of SiO_2 gate dielectric [8]. In this condition, there will be more likely to be several soft breakdown events in the ultra-thin SiO_2 gate dielectric before hard breakdown event occurs [9].

In addition, the reliability of the SiO_2 gate dielectric of advanced technology MOS devices is often not influenced by Fowler-Nordheim tunneling electrons, but rather by hot-carrier injection in the actual working environments. Therefore, constant voltage stress used for producing F-N tunneling electrons can not evaluate the lifetime of SiO_2 gate dielectric of MOS devices in ICs exactly. The impacts of hot carriers to the TDDB reliability of gate oxides must be taken into account. Substrate hot-carrier injection is thought to be a better method to evaluate the breakdown characteristics of ultra-thin gate oxides of MOS devices in the actual working environments [10].

In this study, the TDDB characteristics of ultra-thin gate oxide MOS devices fabricated in 65 nm CMOS technology under constant voltage stress and substrate hot-carrier injection will be presented. The differences in TDDB mechanisms of ultra-thin gate oxides and thick gate oxides will be detailed in the same 65 nm technology. The experimental results of constant voltage stress will be also compared with that of substrate hot-carrier injection acting on the same MOS devices.

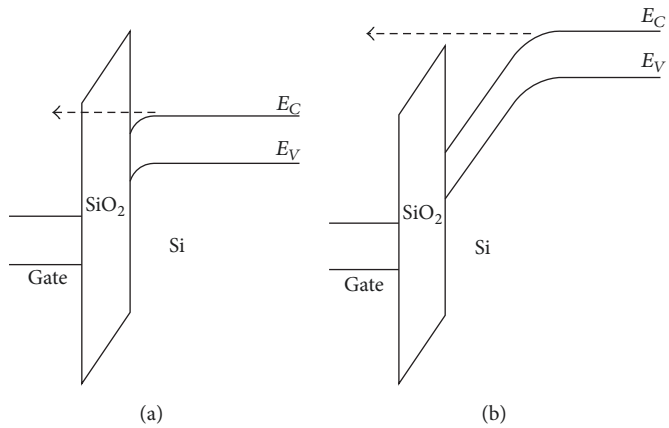

Figure 1: (a) Energy-band diagram of F-N tunneling electrons; (b) energy-band diagram of substrate hot-carrier injection.

In this work, the differences in TDDB characteristics and physical mechanism of ultra-thin gate oxides and thick gate oxides will be explained. Meanwhile, the influence of hot-carrier injection on ultra-thin gate oxide is also taken into account. The work will provide the valuable references for the further reliability study of the advanced nano-MOS devices.

2. Theoretical Description

The TDDB effects of MOS devices have been widely studied. A high constant voltage stress is applied to the gate electrode of MOS device and makes electrons inject into the gate oxide in the form of F-N tunneling in the universal experiments. The gate leakage current is mainly formed by F-N tunneling electrons in the condition of constant voltage stress. Energy-band diagram of F-N tunneling electrons is displayed in Figure 1(a). The charge traps are generated in the dielectric and at the interface because of F-N tunneling electrons injecting into the gate oxides. With the continuous accumulation of charge traps, it results in an increase of local electric field in gate oxide. Further, the increase of local electric field causes higher gate leakage current. Finally the positive feedback of thermoelectricity results in the degradation of gate oxide and further the gate oxide breakdown.

In order to accurately evaluate the lifetime of SiO_2 gate dielectric of MOS device in the actual working environments, the impacts of hot-carrier injection to gate oxide breakdown must be taken into account. Substrate hot carriers are generated by the leakage current of substrate junction and its current multiplication. Substrate hot carriers can gain sufficient energies from high electric field in substrate depletion layer and inject into the gate oxide uniformly. Energy-band diagram of substrate hot-carrier injection is displayed in Figure 1(b). As is well known, the TDDB effect of gate oxide induced by F-N tunneling electrons mainly relies on the role of high electric field in gate oxide. However, the TDDB of gate oxide induced by substrate hot-carrier injection mainly depends on the energies of hot carriers and almost has no relation to the electric field intensity of gate oxide.

3. Devices and Experiments

The devices studied in the experiments are NMOS capacitors fabricated in a typical 65 nm commercial bulk CMOS technology. There are two types of NMOS capacitors with 2 nm and 5.6 nm thick SiO_2 gate dielectric films, respectively. The area of test capacitors is 900 μm^2.

The measurements are realized with the help of an Agilent B1500A high precision semiconductor parameter analyzer and a microprobe station. The measurements are performed on MOS capacitors at room temperature. The testing system provides real-time monitoring of the gate oxide degradation.

In the condition of constant voltage stress, 2 nm thick oxide NMOS capacitor is stressed with V_G = 3.2 V and V_S = 0 V in test case (1). Similarly, 5.6 nm thick oxide NMOS capacitor is stressed with V_G = 7.5 V and V_S = 0 V in test case (2). I_g-t characteristic curves are monitored in real time. The high electric field in gate oxide ensures that electrons are injected into the gate oxide in the form of F-N tunneling. The schematic of constant voltage stress of NMOS capacitor is displayed in Figure 2(a).

In the condition of substrate hot-carrier injection, 2 nm thick oxide NMOS capacitor is stressed with V_G = 1.2 V and V_S = −2 V in test case (3). I_g-t characteristic resulting from substrate hot-carrier injection is monitored in real time. In order to generate the substrate hot carriers, a high voltage (V_S) is stressed on the substrate [10]. This results in the formation of high electric field in the substrate depletion layer. Substrate hot carriers can gain sufficient energies from the high electric field in substrate depletion layer and be injected into the gate oxide uniformly. The schematic of substrate hot-carrier injection of NMOS capacitor is displayed in Figure 2(b). The electric potential difference between V_G and V_S on the 2 nm thick oxide test capacitor is the same ($V_G - V_S$ = 3.2 V) in test cases (1) and (3). It is convenient to compare the differences in the breakdown characteristics induced by the two stress conditions: constant voltage stress and substrate hot-carrier injection.

In addition, in order to investigate the relationship between the energy of substrate hot carrier and gate voltage and substrate bias voltage, another two test cases are added in

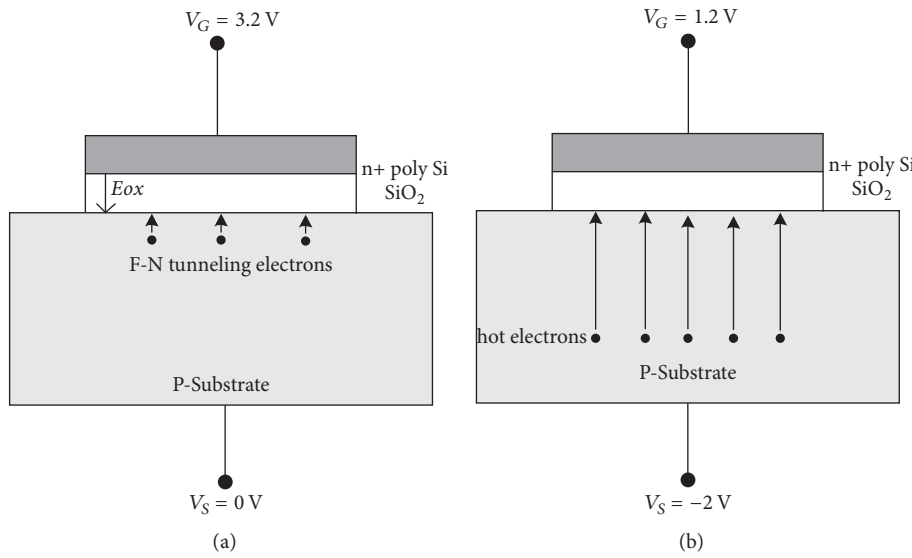

Figure 2: The schematic of (a) constant voltage stress of NMOS capacitor; (b) substrate hot-carrier injection of NMOS capacitor.

this study: (4) V_G = 1.7 V and V_S = −2 V and (5) V_G = 1.2 V and V_S = −2.5 V on the 2 nm thick oxide NMOS capacitors.

4. Results

The following results are obtained from the above test cases (1)~(5).

4.1. I_g-t Characteristics of NMOS Capacitors with 2 nm and 5.6 nm Thick Gate Oxides under Constant Voltage Stress. In order to compare the differences in TDDB characteristics of ultra-thin gate oxides and thick gate oxides under constant voltage stress, we perform test cases (1) and (2). 2 nm thick oxide NMOS capacitor is stressed with V_G = 3.2 V and V_S = 0 V in test case (1), and 5.6 nm oxide capacitor is stressed with V_G = 7.5 V and V_S = 0 V in test case (2). Their I_g-t characteristic curves are displayed in Figure 3. As can be seen from Figure 3, a hard breakdown occurs at 1308 s at a constant gate voltage of 7.5 V in 5.6 nm thick gate oxide. However there are several soft breakdown events in the 2 nm ultra-thin gate oxide and no hard breakdown during more than 20000 s.

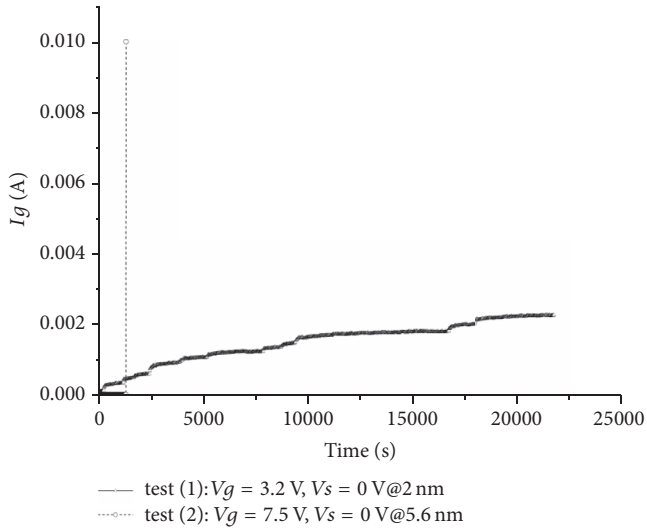

Figure 3: I_g-t characteristics of NMOS capacitors with 2 nm and 5.6 nm thick gate oxides under constant voltage stress.

4.2. I_g-t Characteristics of 2 nm Thick Gate Oxide NMOS Capacitors under Constant Voltage Stress and Substrate Hot-Carrier Injection. Test cases (1) and (3) are performed to investigate the differences between constant voltage stress and substrate hot-carrier injection. The results of test cases (1) and (3) are displayed in Figure 4. For ease of comparison, we ensure that the electric potential difference between V_G and V_S ($V_G - V_S$ = 3.2 V) in test case (1) is the same as that in test case (3). As described above, no hard breakdown occurs under constant voltage stress, even if stress time exceeds 20000 s in test case (1). We can see different results in test case (3). Hard breakdown occurs quickly in the condition of substrate hot-carrier injection. There are still several associated soft breakdown events during the process. The time to hard breakdown (t_{HBD}) is 5600 s.

4.3. I_g-t Characteristics of 2 nm Thick Gate Oxide NMOS Capacitors in Different Forms of Substrate Hot-Carrier Injection Conditions. In order to investigate the relationship between the energy of substrate hot carrier and gate voltage and substrate bias voltage, test cases (3), (4), and (5) are together performed. The time to hard breakdown is as a basis for judgment. Test case (3) is used as a benchmark, in which the test capacitor is stressed with V_G = 1.2 V and V_S = −2 V. In test case (4), V_G increases from 1.2 V to 1.7 V, and V_S remains unchanged based on the stress condition of test case (3). Similarly V_G remains unchanged, and V_S decreases from −2 V to −2.5 V in test case (5). The results of test cases (3), (4), and (5) are displayed in Figure 5. The result of test case (3) has been mentioned above. The experimental

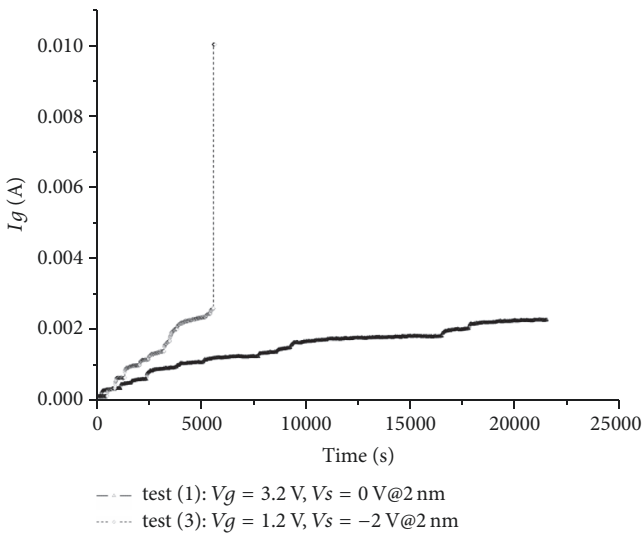

Figure 4: I_g-t characteristics of 2 nm thick gate oxide NMOS capacitor under constant voltage stress and substrate hot-carrier injection.

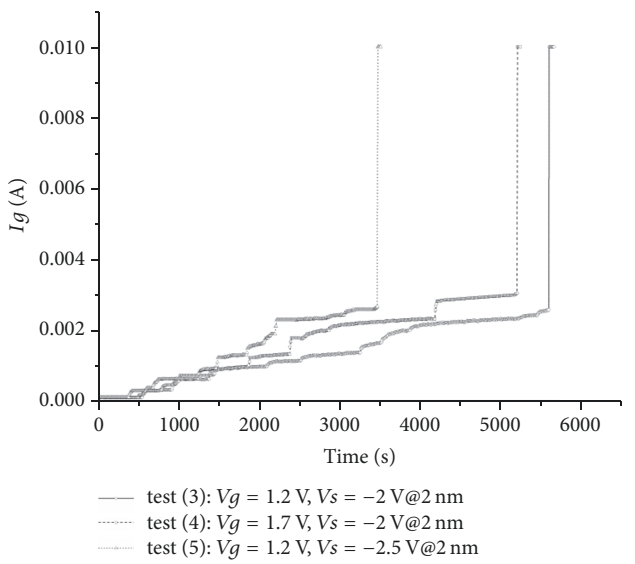

Figure 5: I_g-t characteristics of test capacitors in different forms of substrate hot-carrier injection conditions.

phenomena of test cases (4) and (5) are similar to test case (3). t_{HBD} of test case (4) is roughly equal to that of test case (3), approximately 5200 s. However, as can be seen from Figure 5, t_{HBD} of test case (5) is far less than that of test cases (3) and (4), approximately 3460 s.

5. Discussions

5.1. The Differences in TDDB Mechanisms of Ultra-Thin Gate Oxide and Thick Gate Oxide. The gate oxide thickness of NMOS capacitor is 2 nm in test case (1). The impact of the interface roughness to SiO_2 dielectric characteristics is severe in the ultra-thin gate oxide. The interface roughness is mainly

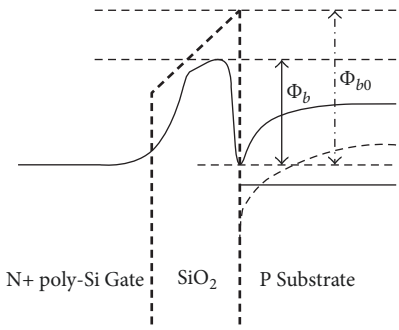

Figure 6: Energy-band diagram of the ultra-thin gate oxide NMOS capacitor.

due to Si and SiO_2 atoms interlacing at the Si/SiO_2 interface [11]. For 2 nm thick gate oxide MOS capacitor, the thickness of SiO_2 dielectric film on the thinnest is even less than 1.2 nm. It is very close to 1 nm. Thus electrons can penetrate to gate electrode from the thinnest sites of dielectric films.

Compared to thick gate oxide, energy-band structure of ultra-thin gate oxide has changed a lot because of extremely thin oxide and rougher interface. Energy-band diagram of the ultra-thin gate oxide NMOS capacitor is displayed in Figure 6. As can be seen from Figure 6, the barrier height (Φ_b) of Si/SiO_2 interface is less than the theoretic value (Φ_{b0} = 3.15 eV) due to the influence of the mirror image force. Moreover, the form of SiO_2 barrier is not a regular rectangle. Usually the actual barrier can be expressed as

$$\Phi_b = \Phi_{b0} - a_0 \varepsilon_{ox}^{1/2} - b_0 \varepsilon_{ox}^{2/3}, \tag{1}$$

where ε_{ox} can be determined from

$$\varepsilon_{ox} = \frac{V_{gs} - V_{fb} - 2\Phi_f - V_{ds}}{t_{ox}}. \tag{2}$$

Therefore, the barrier height (Φ_b) can reduce significantly with the decrease of gate oxide thickness. Electrons can surmount the barrier to inject into gate electrode more easily in 2 nm thick gate oxide.

Furthermore, it is reported that the experimental tunneling barrier (Φ_b') is only 0.936 eV in average in 2 nm thick gate oxide after soft breakdown, which is much less than the barrier of Si/SiO_2 interface (Φ_{b0} = 3.15 eV) [12]. The reason is likely to be that, after soft breakdown, a number of charge traps are generated in the gate oxide, and the electrons are not necessary to directly tunnel to the oxide conduction band. The electrons existing in the quantization energy levels of Si/SiO_2 interface firstly tunnel to the oxide traps band and secondly move free from the traps to the oxide conduction band or the gate electrode [13]. Thus the electrons can be easier to inject into the gate electrode in the form of F-N tunneling after soft breakdown.

From the above, the gate current (I_g) of NMOS capacitor with 2 nm thick gate oxide is composed of three parts: electrons penetrating from the thinnest sites of gate oxides to gate electrode, electrons surmounting the barrier to gate electrode, and electrons tunneling to gate electrode which is the major component of gate current.

The TDDB process in test case (1) is described as below: in the initial stage of adding constant voltage stress, electrons mainly tunnel and surmount the barrier into the gate electrode. As time goes on, the number of traps increases in the gate oxide due to the role of impact ionization. A conductive path is formed in the oxide when the amount of injected electrons meets a certain threshold, and the first breakdown of SiO_2 dielectric film occurs. As can be seen from Figure 3, the first few breakdowns are usually soft breakdowns. After soft breakdown, the barrier height of Si/SiO_2 interface decreases because of the existence of oxide traps and the gate oxide thickness with a few atoms across. That makes it easier for electrons to be injected into the gate oxide. When a new conductive path is formed in the oxide, the gate current increases in the form of jumping. It is indicated that a new soft breakdown occurs. Although several soft breakdowns give rise to the increase of gate current, the lifetime of ultra-thin gate oxide also gets longer because several conductive paths weaken energy concentration rate in the gate oxide. Thus the hard breakdown is not easy to happen; even it will never happen in the ultra-thin gate oxide.

For 5.6 nm thick oxide NMOS capacitor in test case (2), the I_g-t data indicates that gate current decreases slightly with the increase of stress time and then has a sharp increase suddenly. The process can be explained as that charge traps are generated in the gate oxide under constant voltage stress. The injected electrons are trapped, and so the gate current decreases slightly. The anode electric field increases with the continuous accumulation of trapped electrons. When the electric field reaches a certain critical value, destructive breakdown occurs and gate current has a sharp increase [14–23].

5.2. TDDB Characteristics of Ultra-Thin Gate Oxide under Constant Voltage Stress and Substrate Hot-Carrier Injection. TDDB characteristics and physical mechanisms of ultra-thin gate oxide under constant voltage stress have been detailed above. In order to study TDDB characteristics of ultra-thin gate oxide of advanced technology MOS device in the actual working environments, the stress condition with substrate hot-carrier injection is performed on the test capacitor with 2 nm thick gate oxide in test case (3). The results indicate that t_{HBD} of test case (3) (abbr. $t_{HBD(3)}$) is shortened significantly compared to $t_{HBD(1)}$. It is ensured that the electric potential difference between V_G and V_S ($V_G - V_S = 3.2$ V) in test case (1) is the same as that in test case (3). The chief reason why t_{HBD} under substrate hot-carrier injection is less than that under constant voltage stress is most likely to be that the bias voltage of substrate junction makes the substrate hot carriers gain enough energy to surmount the interface barrier into the gate oxide. Moreover the actual barrier height of 2 nm thick gate oxide is lower than 3.15 eV, so hot carriers can be injected into the gate oxide more easily. In particular, after the soft breakdown events occur, the ultra-thin gate oxide is damaged further. The above factors accelerate the destructive breakdown of ultra-thin gate oxide.

5.3. The Relationship between the Energy of Substrate Hot Carrier and Gate Voltage and Substrate Bias Voltage. From the experimental results of test cases (3), (4), and (5), we can see that $t_{HBD(5)} < t_{HBD(4)} \approx t_{HBD(3)}$. The difference of stress conditions between test cases (3) and (4) is the changes of gate voltage (V_G) with 0.5 V. However t_{HBD} of test case (4) is roughly equal to that of test case (3). It is shown that the energy of substrate hot carrier has no relation to the magnitude of gate voltage. Similarly compared to test case (3), the stress condition V_S of test case (5) varies from −2 V to −2.5 V. t_{HBD} of test case (5) is shortened significantly. It is proved that the energy of substrate hot carrier has a strong correlation with the substrate bias voltage. The energies of substrate hot carriers enhance with the increase of substrate bias voltage. As a result, the time to breakdown is shortened obviously. Therefore the energy of substrate hot carrier is determined by the substrate bias voltage, and the magnitude of gate voltage only affects the electric field intensity of gate oxide.

6. Conclusions

We have investigated the TDDB characteristics of ultra-thin gate oxide MOS capacitors under constant voltage stress and substrate hot-carrier injection. As is well known, the gate leakage current of normal thick gate oxide is mainly formed by tunneling electrons under constant voltage stress. In this work, it is shown that the gate current of ultra-thin gate oxide MOS capacitor under constant voltage stress is composed of tunneling electrons, electrons surmounting the barrier, and penetrating electrons. If the failure criterion is defined as a hard breakdown, it is found that the lifetime of ultra-thin gate oxide is much longer than thick gate oxide because several soft breakdowns weaken energy concentration rate in the ultra-thin gate oxide. The reasons why the time to hard breakdown under substrate hot-carrier injection is less than that under constant voltage stress have been explained. It is proved that the energy of substrate hot carrier is determined by the substrate bias voltage, and the magnitude of gate voltage only affects the electric field intensity of gate oxide.

In this work, we have a deeply understanding of the reliability of ultra-thin gate oxide of deep submicron and nano-MOS devices. Particularly in the actual working environments, the combined influence of hot carriers and tunneling electrons to TDDB is understood deeply. This work can provide some references for the further reliability study of the advanced nano-MOS devices.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

This work is supported by the National Pre-Research Program of China under Grant 31513050303 and the National Natural Science Foundation of China under Grant 61404021.

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