Hindawi Publishing Corporation
Advances in Fuzzy Systems
Volume 2012, Article ID 419370, 8 pages
doi:10.1155/2012/419370

Research Article

A Novel Programmable CMOS Fuzzifiers Using Voltage-to-Current Converter Circuit

K. P. Abdulla and Mohammad Fazle Azeem

Department of Electronics and Communication Engineering, PA College of Engineering, Karnataka, Mangalore 574153, India

Correspondence should be addressed to K. P. Abdulla, kp.abdulla@gmail.com

Received 27 April 2012; Accepted 21 May 2012

Academic Editor: Oscar Castillo

This paper presents a new voltage-input, current-output programmable membership function generator circuit (MFC) using CMOS technology. It employs a voltage-to-current converter to provide the required current bias for the membership function circuit. The proposed MFC has several advantageous features. This MFC can be reconfigured to perform triangular, trapezoidal, S-shape, Z-Shape, and Gaussian membership forms. This membership function can be programmed in terms of its width, slope, and its center locations in its universe of discourses. The easily adjustable characteristics of the proposed circuit and its accuracy make it suitable for embedded system and industrial control applications. The proposed MFC is designed using the spice software, and simulation results are obtained.

1. Introduction

The concept of Fuzzy Logic was introduced by Zadeh nearly 40 years ago [1–6], and since then numerous applications of this theory has been implemented in various engineering and nonengineering fields. The numerous successful applications of fuzzy-control have sparked a flurry of activities in the analysis and design of fuzzy-control systems. Fuzzy-control theories have some salient features and distinguishing merits. The different fields in which fuzzy logic has been applied include signal processing, computer vision, automatic control, consumer electronics, household appliances, decision making analysis, and so on. The number of applications using fuzzy logic techniques to solve control problems has increased considerably. This rapid growth of fuzzy logic has motivated the researchers to go for efficient realization of fuzzy inference systems (FIS) [7, 8].

Fuzzy inference system can be implemented using software or hardware. Software implementation of FIS is useful when an application can be moduled to simulate, and calculate in advance, its multidimensional response characteristic. It provides flexibility as they usually support fuzzy systems with an arbitrary number of rules without any limitation concerning the number, type of membership, and range of inference mechanism. On the other hand, it works on a computer or a processor platform, and it has a drawback of being very slow [9, 10]. Hence it is not used for real-time application. A study of software and hardware implementation of FIS is described in [11], and it demonstrates the advantages of hardware design over software design in terms of speed and computational requirements. Therefore hardware realization is preferred for real-time applications, and various hardware techniques have been proposed [12].

The digital and analog techniques constitute the two existent approaches for the hardware realization of fuzzy systems. There are different techniques reported in the literature for the digital design of fuzzy systems. Among them, the most versatile methods are those which use field programmable gate arrays (FPGA) as reported by Maldonado et al. [13] and by Montiel et al. [14]. Even though the digital approach is superior in terms of ease of design, the analog fuzzy logic approach is proposed to get maximum efficiency in terms of silicon area, power consumption, and delay time or processing speed [15–19]. Thus it leads to low-cost and high-speed implementation compared to the digital counterpart. A direct interface of the controller to input and output continuous variables is also possible, thus making

the circuitry for analog-to-digital conversion unnecessary and inducing delay in the control loop too.

Fuzzification is an important concept used in the fuzzy logic theory. It is the process of converting a crisp value into a fuzzy value. The conversion is actually the incorporation of fuzziness, uncertainty, vagueness, or ambiguity in the crisp quantity. In the real world, the quantities which look crisp actually carry a considerable amount of uncertainty or vagueness. This uncertainty, vagueness, or imprecision in a fuzzy quantity can be represented by a membership function. Membership function is the key element in fuzzy signal processing. This provides a nonlinear relation that measures the compatibility of an object with the concept represented by a fuzzy set. Fuzzy set provides a convenient point of departure from the construction of a conceptual framework used in ordinary sets and have proved to have a much wider scope of applicability, particularly in the fields of pattern classification, information processing, statistical process control, and so forth. The researchers have developed various membership functions for the fuzzy processors using different techniques like digital methods [20, 21], mixed-mode signal [22, 23], and current-mode methods [24, 25]. The design of a membership function depends on the particular application to which the fuzzy processor is being applied.

The fuzzifier circuit resented in this paper is a suitable circuit to analyze and tune the nonlinear parameters of membership functions [26]. The important property of this fuzzifier is that by changing the various parameters, a membership function with different shape and slope can be easily generated. The fuzzifier designed here is a programmable circuit. This scheme is expected to find application in neuro-fuzzy processors where adaptation of the membership function parameters is required [27]. The result is a faster, cheaper, and higher controllable design compared to conventional fuzzification techniques. The proposed MFC has been laid out using full-custom techniques to provide standard cell. And it results in a CMOS-MFC standard cell, which could be then used as a standard component for implementing a number of required MFC in integrated circuit [28, 29]. This structure exploits the operation of the MOS differential amplifier as a current switch with soft transition region.

The major contributions of the proposed work can be summarized as follows: (1) firstly, the proposed design use a voltage-input, current-output interface which is very useful for the real world sensor interface with current-mode fuzzy-control systems, (2) secondly, the application of the analog voltage-to-current converter makes it easy to tune the nonlinear parameters of the MFC such as width and slope, and (3) finally, the low-power CMOS realization ensures a faster, cheaper, and highly controllable design for embedded system and industrial control applications.

This paper is organized into four sections: Section 2 describes the architecture of the proposed fuzzy membership function circuit and Section 3 explains the circuit level discretion for the same. It is followed by simulation results graphically described in Section 4, and conclusions are discussed in Section 5.

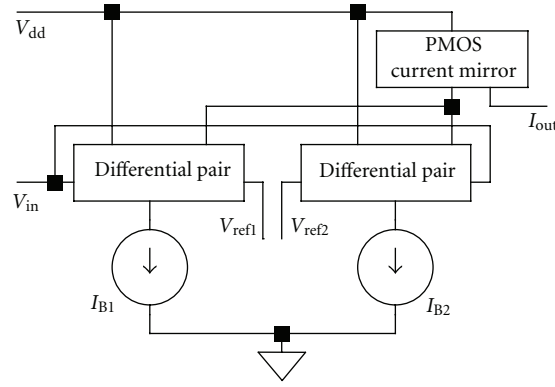

Figure 1: Block diagram of an MFC.

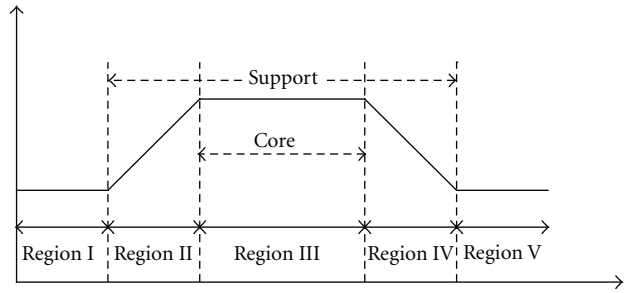

Figure 2: Trapezoidal shape of membership function.

2. The Proposed Circuit

Fuzzifying is the first step in a fuzzy system. The input data of a fuzzy logic controller are usually crisp values acquired from sensor measurement. Therefore, fuzzification interface is needed to calculate the belongingness (membership) of the observed inputs to the defined linguistic terms in the preconditions of the fuzzy rules. This is carried out through the fuzzy membership function circuits (MFCs), which performs a nonlinear transform from their inputs to their outputs. MFCs are provided with the input signal from the external environment, normally in the voltage mode. On the other hand, the processing steps following the fuzzification stage performs better in the current mode.The block diagram of an MFC is as shown in the Figure 1.

The MFC in Figure 1 is built of a coupled differential amplifier pair which has two differential pairs and a PMOS current mirror for replicating the drain currents to the output. The two reference voltages, V_{ref1} and V_{ref2}, where $V_{ref1} < V_{ref2}$, define the membership function. Depending on the relative values of input voltage V_{in} and the reference voltages V_{ref1} and V_{ref2}, the circuit operates in one of the five regions (I–V) as shown in Figure 2.

Basically, a fuzzy term can be defined by a membership function of trapezoidal shape as shown in Figure 2. The core of the function corresponds to the region which has full membership ($\mu = 1$), the ascending and descending boundaries are the regions with partial membership ($0 < \mu < 1$), and support is the sum of core and the boundaries in which $\mu > 0$. Further we assume that the current I_{B1} and I_{B2}

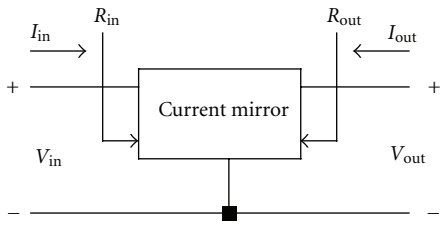

Figure 3: Block diagram of a current mirror.

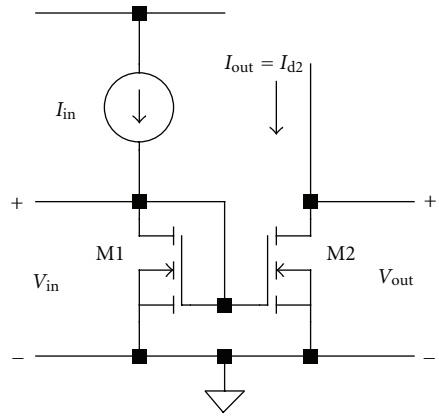

Figure 4: NMOS current mirror.

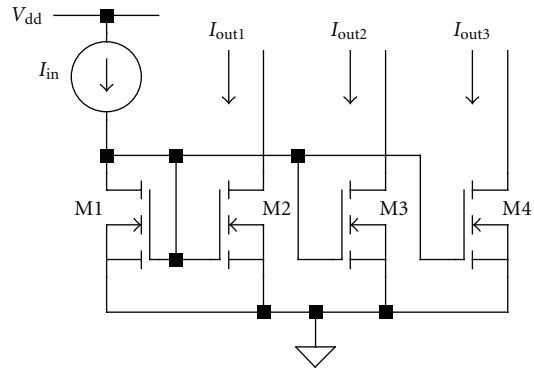

Figure 5: NMOS current replication circuit.

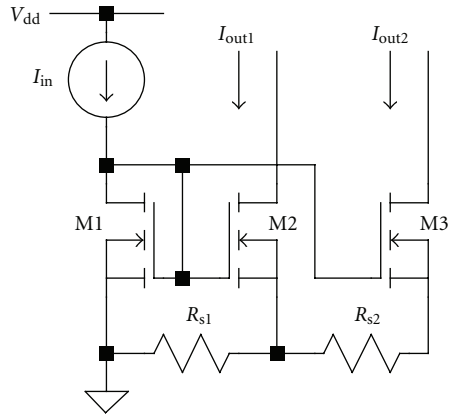

Figure 6: NMOS current mirror with two outputs and supply resistances.

in DP1 and DP2 are ideal and equivalent, the input devices in each differential pairs are symmetric, and the half widths of the transfer regions of DP1 and DP2 are V_1 and V_2, if W/L is equal for all MOSFETs used, therefore $V_1 = V_2 = \sqrt{2}V_{ov}$, where V_{ov} is the overdrive voltage.

The MFC shown in Figure 1 has four control signals—two voltage signals (V_{ref1} and V_{ref2}) and two current signals (I_{B1} and I_{B2})—for the width and slope tunability, respectively. In the proposed design of MFC, we have used an MOS voltage-to-current converter, which provides the bias current to the differential pairs DP1 and DP2. This voltage to current converter has a good linearity and very high sensitivity. The voltage-to-current converter was designed and simulated to study its characteristics and justify its usefulness in the design of tunable MFC circuits.

3. Circuit Level Description

As it can be seen from the Figure 1, the two important components of the proposed membership function circuit are the current mirrors and the differential amplifiers. This section explains the circuit level design and analysis of the basic analog structures used in the design of the proposed membership function circuit.

3.1. Current Mirrors. The block diagram of a typical current mirror is as shown in Figure 3. For an ideal condition, $I_{out} = (BI_{in})$, $R_{in} \gg 0$, and $R_{out} \gg \infty$, where R_{in} and R_{out} are the input and output impedances, respectively.

A current mirror is actually a combination of a diode-connected transistor followed by a single-transistor amplifier. The first one converts the input current into voltage, whereas the latter one converts the voltage into current. The current ratio will be quite accurate, simply because the non-linearity of the diode-connected MOS transistor (MOST) is compensated by the non-linearity of the amplifying MOST. If the ratio of their W/L's is B, then the current ratio is also B. Indeed, these MOSTs have the same V_{GS}, that is, ground-to-source voltage and hence $V_{GS} - V_T$. This ratio is the current gain.

3.1.1. NMOS Current Mirror. In the circuit shown in Figure 4, MOSFETs M1 and M2 form a current mirror and gate source voltages of both the MOSFETs are same because they are shorted. In MOSFET M1, the drain is shorted to its gate, thereby forcing it to operate in the saturation mode with

$$I_{in} = \frac{1}{2}K_n'\left(\frac{W}{L}\right)_1 (V_{GS1} - V_T)^2, \tag{1}$$

where channel length modulation is neglected. Now consider the MOSFET M2. It is also working in the saturation

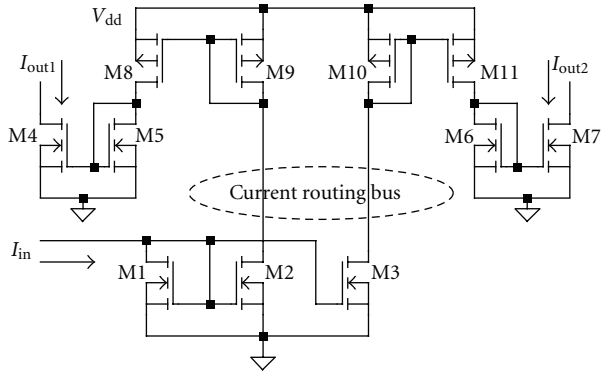

FIGURE 7: Bias distribution circuit using both current-routing and voltage-routing.

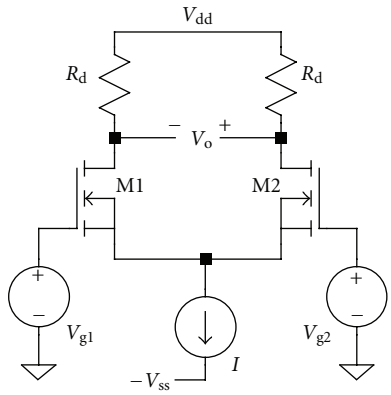

FIGURE 8: Differential pair with two inputs V_{g1} and V_{g2}.

mode, therefore the expression for its drain current (of the threshold voltages of M1 and M2 are equal) is given by

$$I_{out} = \frac{1}{2}K_n'\left(\frac{W}{L}\right)_2(V_{GS2} - V_T)^2. \quad (2)$$

Since the gates of M1 and M2 are shorted, $V_{GS1} = V_{GS2}$, therefore,

$$\frac{I_{in}}{I_{out}} = \frac{(W/L)_1}{(W/L)_2}. \quad (3)$$

Let $(W/L)_1 = (W/L)_2$, this implies that $I_{in} = I_{out}$.

Now if we would like to replicate more current of same value, then a current replication circuit is used by increasing the number of MOSFETs as shown in the Figure 5.

3.1.2. Current-Routing and Voltage-Routing. Consider the current mirror shown in Figure 6, which has one input and two outputs. At first, assume that $R_{s1} = R_{s2} = 0$. Also, assume that the input current is generated by a circuit with desirable properties.

Since the gate source voltage of M1 must be routed to M2 and M3 here, this case is referred to as an example of the *voltage routing* of bias signals. An advantage of this approach is that by routing only two nodes (the gate and the source

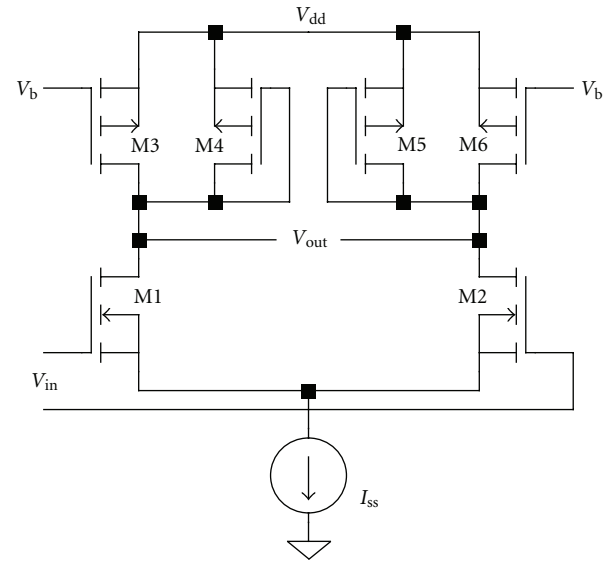

FIGURE 9: Differential pair with current source in addition to diode-connected load.

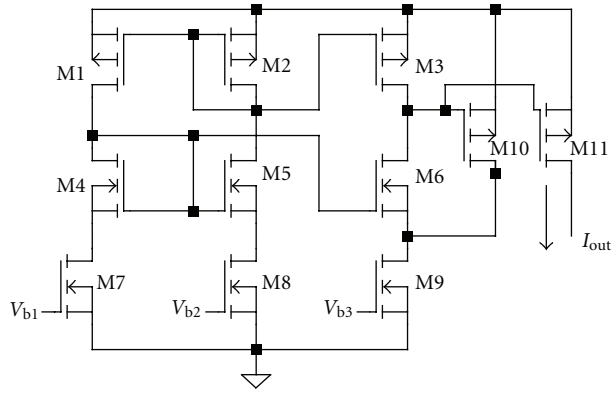

FIGURE 10: Voltage-to-current converter.

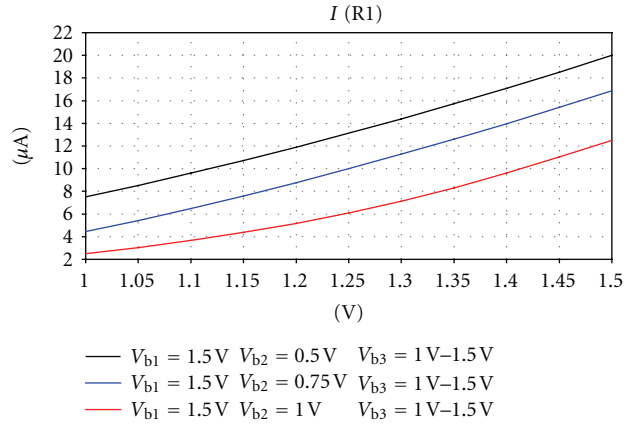

FIGURE 11: Voltage to Current converter output with $V_{b1} = 1.5$ V, $V_{b2} = 0.5$ V, 0.75 V, and 1 V, and V_{b3} sweep voltage from 1 V to 1.5 V in steps of 50 mV.

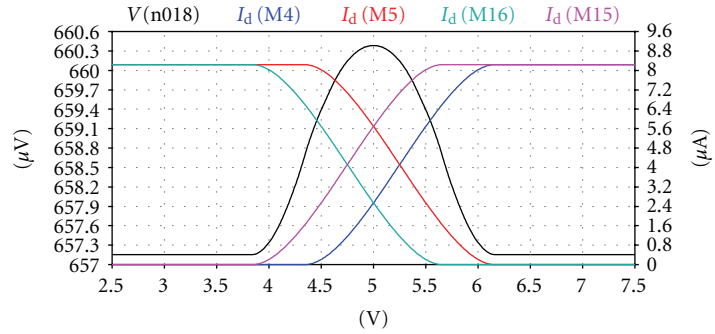

Figure 12: Gaussian-shaped membership function, $V_{b3} = 1.65$ V.

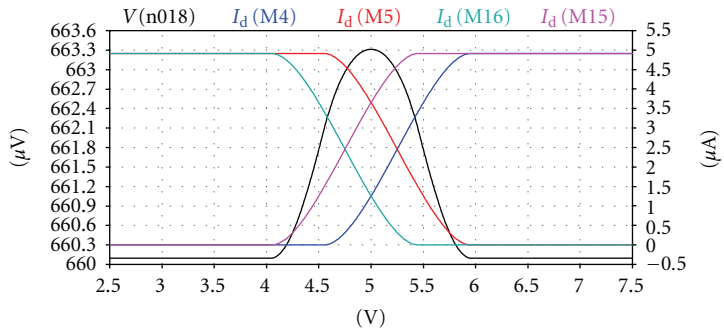

Figure 13: Gaussian-shaped membership function, $V_{b3} = 1.45$ V.

of M1) around the IC, any number of output currents can be produced.

Unfortunately, voltage routing has two disadvantages. First, the input and output transistors in the current mirror may be separated by distances that are large compared to the size of the IC, increasing the potential mismatches. In particular, the threshold voltage typically displays considerable gradient with distance across a wafer. Therefore, when the devices are physically separated by large distances, large current mismatch can result from biasing current sources sharing the same gate-source bias, especially when the overdrive is small. The second disadvantage of voltage routing is that the output currents are sensitive to variations in the supply resistances R_{s1} and R_{s2}.

To overcome these problems, the circuit in Figure 6 can be built so that M1–M3 are close together physically, and the current outputs I_{out1} and I_{out2} are routed as required on the IC. This case is referred to as an example of the current routing of bias signals as shown in Figure 7. Current routing reduces the problems with mismatch and supply resistance by reducing the distances between the input and output transistors in the current mirror compared to voltage routing. One disadvantage of current routing is that it requires one node to be routed for each bias signal. Therefore, when the number of bias outputs is large, the die area required for the "interconnect" to distribute the bias currents can be much larger than that required for voltage routing.

In practice, many ICs use a combination of current and voltage-routing techniques. If the current-routing bus in Figure 6 travels over a large distance, the parasitic capacitances on the drains of M2 and M3 may be large. In ICs using both current and voltage routing, currents are routed globally and voltages locally, where the difference between global and local routing depends on distance. When the distance is large enough to significantly worsen mismatch or supply resistance effects, the routing is global. Otherwise, it is local.An effective combination of these bias distribution techniques is to divide an IC into blocks, where bias currents are routed between blocks and bias voltages within the blocks. In this work, for the effective routing of the bias current, both current and voltage routings are used.

3.2. Differential Pair. MOS differential pair is widely used as an input stage in operational amplifiers and in many other types of circuits as well. This venerable circuit has a relatively large response to a change in the difference between its two input voltages, but a relatively small response to a change in the average value of its two input voltages. The usefulness of the differential pair stems from two key properties. First, cascades of differential pairs can be directly connected to one another without inter-stage-coupling capacitors. Second, the differential pair is primarily sensitive to the difference between two input voltages, allowing a high degree of rejection of signals common to both inputs.

Figure 8 shows an MOS differential pair. Here M1 and M2 are two matched transistors, biased by a common current

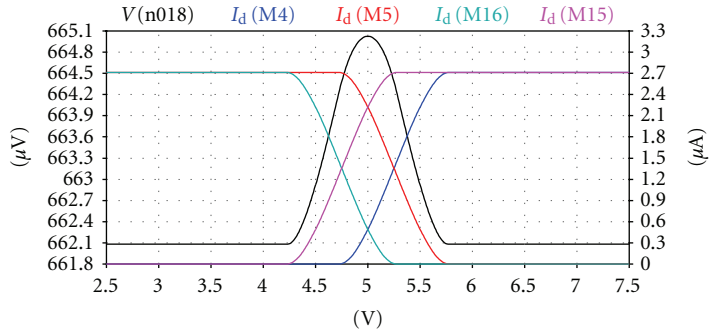

Figure 14: Gaussian-shaped membership function, $V_{b3} = 1.25$ V.

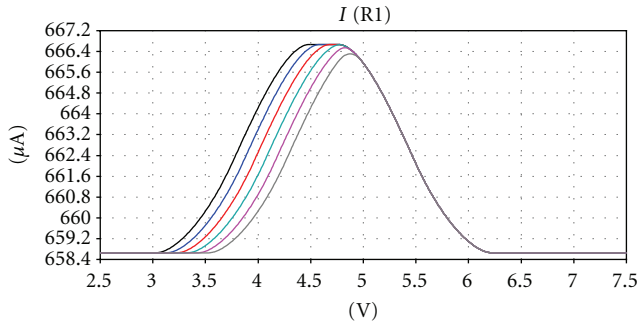

Figure 15: Width and position tunability through left side.

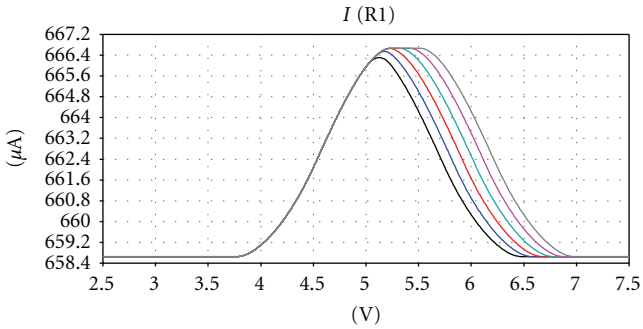

Figure 16: Width and position tunability through right side.

source $I_{applied}$, with identical drain resistance R_d. V_{g1} and V_{g2} are two input voltages applied at the gates G1 and G2.

The drain currents of the MOSFET are given by the following relation:

$$i_{d1} = \frac{I}{2} + \left(\frac{I}{V_{ov}}\right)\left(\frac{V_{id}}{2}\right)\sqrt{1 - \left(\frac{V_{id}/2}{V_{ov}}\right)^2},$$
$$i_{d1} = \frac{I}{2} - \left(\frac{I}{V_{ov}}\right)\left(\frac{V_{id}}{2}\right)\sqrt{1 - \left(\frac{V_{id}/2}{V_{ov}}\right)^2}. \quad (4)$$

When $V_{id} = \sqrt{2}V_{ov}$, $i_{d1} = I$ and $i_{d2} = 0$. When $V_{id} = -\sqrt{2}V_{ov}$, $i_{d2} = I$ and $i_{d1} = 0$.

3.2.1. Differential Pair with MOS Loads. The load of a differential pair need not be implemented by linear resistors. Differential pair can employ diode-connected or current-source loads. The diode-connected loads consume voltage headroom, thus creating a trade-off between output voltage swing, output voltage gain, and input common mode range. In order to alleviate the above difficulty, part of the current of the transistors can be provided by PMOS current sources. Here the idea is to lower the g_m of the load devices by reducing their current rather than their aspect ratio. For the proposed design, both the differential pairs shown in Figure 1 are connected with diode-connected and current-source loads to increase the gain as shown in Figure 9.

Figure 9 shows a differential pair with both diode-connected as well as current-source loads. This configuration can be used to increase the gain. For example, if M3 and M6 carry 80% of the drain current of M1 and M2, then the current through M4 and M5 is reduced by a factor of five. For a given $|V_{GSP} - V_{THP}|$, this translates to a factor of five reductions in the transconductance of M4 and M5, because the aspect ratio of the device can be lowered by the same factor. Thus, the differential gain is now approximately five times that of the case with no PMOS current source.

3.3. Voltage to Current Converter. As current-mode circuits are restricted to single fan-out, multiple current mirrors are required to share fan-out signals among several operational blocks. Voltage-mode inputs are thus preferable for fuzzy hardware systems, since they must be distributed to the membership function circuits of many rule blocks. Current-mode signals are appreciated afterwards, because of the advantages provided by current-mode processing. Tunable voltage-input current-mode membership function circuits are consequently useful building blocks to proceed fuzzification with current-mode analog hardware. For this reason, a voltage-to-current (V-to-I) converter is used to provide the bias currents in the proposed fuzzifier circuit. The schematic for the proposed voltage-to-current converter is as shown in the Figure 10.

In the above circuit, the MOS transistors M7, M8, and M9 are operated in the triode region, and a negative feedback loop is established by the MOS transistor M10. There the current through the MOS transistor M10 is B times up-scaled

current through the MOS transistor M11, which delivers the output current I_{out}, proportional to the input voltage ratio as given by the relation:

$$I_{out} = B\frac{V_{b3} - V_{b2}}{V_{b1} - V_{b2}}I_{in}, \quad (5)$$

where B is the ratio of W/L's of the MOS transistors M10 and M11, and effective I_{in} is the current through the MOS transistor M7. From the above expression, it is clear that the relationship between the input voltage V_{b3} and the output current I_{out} is linear and can be used as a voltage-to-current converter. In the proposed membership function circuit this voltage-to-current converter is used to tune the width and slope of the Gaussian-shaped membership function.

4. Simulation Results

All the above discussed circuits are designed and simulated using spice simulation software to study their characteristics and verify the working. This section provides the results of simulation for the above-discussed circuits and also a brief note on the obtained result.

The first result presented is the output for the proposed voltage-to-current converter as shown in Figure 11. Here we can observe that the V-I characteristics for the proposed circuit is linear and thus can be used as a voltage-controlled current source that can be used to supply the bias current for the membership function circuit. The required bias current can be set by varying the control voltage V_{b3} (V_{b1} and V_{b2} are fixed conveniently observing (5)).

Thus by varying the voltage V_{b3} we can control the width and the slope of the Gaussian-shaped membership function as shown in Figures 12, 13 and 14. For all the three simulation, $V_{b1} = 1.5\,V$ and $V_{b2} = 1\,V$.

Figures 15 and 16 shows the simulation results for the width and position tunability through left side and right side, respectively. For the left side tunability the voltage V_{low} is varied from 3.75 V to 4.25 V with 0.1 V increment. For right side tunability the voltage V_{high} is varied from 5.75 V to 6.25 V with 0.1 V increment.

From the above simulation results for the membership function circuit, it is clear that we have got three control voltages for the tuning of the membership function: V_{b3}, V_{low} and V_{high}. These voltages can be used to tune the slope, width and position of any particular membership function.

5. Conclusions

A new programmable CMOS fuzzifier circuit has been presented. The proposed membership function has the following advantages: proposed MFC is capable of generating different membership functions of different shapes—like Gaussian, S-shape, Z-shape, and trapezoidal—from a single circuit therefore it require lesser hardware. The proposed MFC exhibits a great programmability property just by use of three control voltages—V_{ref1}, V_{ref2}, and V_{b3}. Thus any characteristics of the MFC are easily obtained. The proposed circuit is very simple and compact and can be VLSI fabricated.

References

[1] L. A. Zadeh, "Fuzzy logic," *IEEE Computer*, vol. 21, no. 4, pp. 83–93, 1988.

[2] L. A. Zadeh, "Outline of a new approach to the analysis of complex systems and decision processes," *IEEE Transactions on Systems, Man and Cybernetics*, vol. 3, no. 1, pp. 28–44, 1973.

[3] M. Sugeno, "An introductory survey of fuzzy control," *Information Sciences*, vol. 36, no. 1-2, pp. 59–83, 1985.

[4] E. H. Mamdani, "Applications of fuzzy algorithms for simple dynamic plant," *Proceedings of the Institution of Electrical Engineers*, vol. 121, no. 12, pp. 1585–1588, 1974.

[5] C. C. Lee, "Fuzzy logic in control systems: fuzzy logic controller—part I," *IEEE Transactions on Systems, Man and Cybernetics*, vol. 20, no. 2, pp. 404–418, 1990.

[6] C. C. Lee, "Fuzzy logic in control systems: fuzzy logic controller—part II," *IEEE Transactions on Systems, Man and Cybernetics*, vol. 20, no. 2, pp. 419–435, 1990.

[7] T. J. Ross, *Fuzzy Logic with Engineering Applications*, John Wiley & Sons, 2005.

[8] A. Costa, A. D. Gloria, F. Giudici, and Olivieri, "Fuzzy logic microcontroller," *IEEE Micro*, vol. 17, no. 1, pp. 66–74, 1997.

[9] H. Watanabe and D. Chen, "Evaluation of fuzzy instructions in a RISC processor," in *2nd IEEE International Conference on Fuzzy Systems*, pp. 521–526, April 1993.

[10] H. Watanabe, D. Chen, and S. Konuri, "Evaluation of min/max instructions for fuzzy information processing," *IEEE Transactions on Fuzzy Systems*, vol. 4, no. 3, pp. 369–374, 1996.

[11] R. Sepúlveda, O. Montiel, O. Castillo, and P. Melin, "Embedding a KM type reducer for high speed fuzzy controller into an FPGA," *Applied Soft Computing*, vol. 12, no. 3, pp. 988–998, 2012.

[12] D. G. Zrilic, J. Ramirez-Angulo, and B. Yuan, "Hardware implementations of fuzzy membership functions, operations, and inference," *Computers and Electrical Engineering*, vol. 26, no. 1, pp. 85–105, 2000.

[13] Y. Maldonado, O. Montiel, R. Sepúlveda, and O. Castillo, "Design and simulation of the fuzzification stage through the Xilinx system generation," *Soft Computing for Hybrid Intelligent Systems*, vol. 154, pp. 297–305, 2008.

[14] O. Montiel, R. Sepúlveda, Y. Maldonado, and O. Castillo, "Design and simulation of the type-2 fuzzification stage: using active membership functions," *Evolutionary Design of Intelligent Systems in Modeling, Simulation and Control*, vol. 257, pp. 273–293, 2009.

[15] M. Kachare, J. Ramírez-Angulo, R. G. Carvajal, and A. J. López-Martín, "New low-voltage fully programmable CMOS triangular/trapezoidal function generator circuit," *IEEE Transactions on Circuits and Systems I*, vol. 52, no. 10, pp. 2033–2042, 2005.

[16] T. Kettner, C. Heite, and K. Schumacher, "Analog CMOS realization of fuzzy logic membership functions," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 7, pp. 857–861, 1993.

[17] J. J. Chen, C. C. Chen, and H. W. Tsao, "Tunable membership function circuit for fuzzy control systems using CMOS technology," *Electronics Letters*, vol. 28, no. 22, pp. 2101–2103, 1992.

[18] N. Kong, U. Seng-Pan, and R. P. Martins, "A novel reconfigurable membership function circuit for analog fuzzy logic controller," in *Proceedings of the China Symposium on Circuits and Systems (CSCAS '07)*, 2007.

[19] L. Tigaeru, D. Alexa, and O. Ursaru, "New analog mode membership function circuit," in *Proceedings of the IEEE*

International Symposium on Signals, Circuits and Systems (SCS '03), pp. 601–604, 2003.

[20] D. Di Cataldo, V. Liberali, F. Maloberti, and G. Palumbo, "A/D conversion with fuzzy membership function," in *European Signal Processing Conference (EUSIPCO '96)*, pp. 1279–1282, Trieste, Italy, September 1996.

[21] F. A. Samman, R. S. Sadjad, and E. Y. Syansuddin, "The reconfigurable membership function circuit using analog bipolar electronics," in *Proceedings of the Asia-Pacific Circuits and Systems (APCCAS '02)*, pp. 537–540, 2002.

[22] N. Kong, U. Seng-Pan, and R. P. Martins, "A novel current-mode reconfigurable membership function circuit for mixed-signal fuzzy hardware," in *Proceedings of the 4th Regional Inter-University Postgraduate Electrical and Electronics Engineering Conference (RIUPEEEC '06)*, July 2006.

[23] L. Mesquita, G. Botura, and Saotome, "A mixed mode membership function circuit in CMOS technology," VI Workshop IBERCHIP, pp. 443-449, 2000.

[24] M. Conti, P. Crippa, S. Orcioni, and C. Turchetti, "Current-mode circuit for fuzzy partition membership functions," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '99)*, vol. 5, pp. V-391–V-394, June 1999.

[25] M. Sasaki, N. Ishikawa, F. Ueno, and T. Inoue, "Current-mode analog fuzzy hardware with voltage input interface and normalization locked loop," *IEICE Transactions on Fundamentals*, vol. 75, no. 6, pp. 650–654, 1992.

[26] D. D. Majumder, R. Bhattacharyya, and S. Mukherjee, "Methods of evaluation and extraction of membership functions—review with a new approach," in *Proceedings of the International Conference on Computing: Theory and Applications (ICCTA '07)*, pp. 277–281, March 2007.

[27] K. Basterretxea, J. M. Tarela, and I. del Campo, "Digital gaussian membership function circuit for neuro-fuzzy hardware," *Electronics Letters*, vol. 42, no. 1, pp. 44–45, 2006.

[28] A. Khodair, A. Badawy, and M. El-khatib, "VLSI Implementation of fuzzy logic membership function circuit," in *Proceedings of the 1st International Conference on Electrical Engineering*, March 1998.

[29] M. Tokmakçi, M. Alçi, and R. Kiliç, "A simple CMOS-based membership function circuit," *Analog Integrated Circuits and Signal Processing*, vol. 32, no. 1, pp. 83–88, 2002.