Research Article

LTPS-TFT Pixel Circuit Compensating for TFT Threshold Voltage Shift and IR-Drop on the Power Line for AMOLED Displays

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We propose a new pixel design for the active matrix organic light-emitting diode (AMOLED) using low-temperature polycrystalline silicon thin-film transistors (LTPS-TFTs). The proposed pixel is composed of four switching TFTs, one driving TFT (DTFT), and one capacitor. The simulation results are performed by AIM-SPICE software. The error rate of OLED output current with V_{TH} (threshold voltage) variation (0.3 V) and V_{dd} power line drop by 1 V are improved to about 1.67% and 15%, respectively. Thus, the proposed pixel circuit can successfully overcome drawbacks suffered from DTFT threshold voltage deviation and IR-drop on power line.

1. Introduction

Organic light-emitting diode (OLEDs) displays have gained considerable interest in large-area flat panel display applications due to their excellent optoelectric properties, large viewing angle, color versatility, and potentially low fabrication cost [1]. Therefore, great effort has been made to develop active matrix driving techniques for organic light-emitting diode displays making it possible to achieve large, high-resolution displays.

Recently, AMOLED driving pixel circuits are composed of amorphous silicon thin-film transistors (a-Si TFTs) or low-temperature polysilicon thin film transistors (LTPS-TFTs). It is no doubt that LTPS-TFTs are suitable as switching and driving devices for AMOLED because of their outstanding driving capability due to the higher mobility, which can approach more practical and powerful applications [2]. However, the LTPS-TFT manufacturing process will cause nonuniform electrical characteristics such as threshold voltage variations in pixels, depending on the fluctuations in excimer laser energy, resulting in uncontrollable gate oxide trap density and irregular grain boundary distribution

in the polySilicon material [3–5]. In the typical p-type 2-TFT pixel circuit, the supply power line is connected to the DTFT source node. The output current suffers from parasitic resistance on the supply power lines. The parasitic resistance may lead to power dissipation, called $I \times R$ voltage drop. This is inevitable by Ohm's Law and will cause non-uniform luminance in the panel [6]. To solve the nonuniformity issue caused by V_{TH} variation and $I \times R$ drop-voltage, several methods have been proposed [7–13]. The current programming method effectively compensates for the threshold voltage variation and field-effect mobility shifts in TFTs. However, it requires longer charging time at the data lines compared with the voltage programming method. Thus, voltage programming methods are more suitable in large-size displays. However, most of these studies could not compensate for both the DTFT threshold voltage variation and the $I \times R$ voltage drop at the same time. Comparatively, our compensation methods can overcome both critical issues and still preserve stable driving ability.

This paper describes a new voltage programming pixel circuit based on the LTPS technology. The proposed pixel circuit has high immunity to DTFT threshold voltage

FIGURE 1: Signal lines for the proposed pixel circuit design and timing scheme.

variation and can simultaneously compensate for the voltage drop on the power line. Compared with conventional 2-TFT pixel, the simulation results demonstrate that the output current error rate and its degradation rate are improved by 1.67% and 4% due to DTFT V_{TH} variation (± 0.3 V) and V_{dd} drop of 0.3 V, respectively. We believe that the proposed pixel circuit is a good candidate for large-size, high-resolution AMOLED applications.

2. Proposed Pixel Circuit and Driving Method

Figure 1 demonstrates the proposed schematic pixel circuit based on poly-Si TFTs and its signal line driving scheme. The pixel consists of four switching TFTs (M1, M3, M4, and M5), one p-type driving TFT (M2), and one capacitor. The driving scheme has two selection lines (Scan1, and Scan2) and a data line (DT). M1 is a selection switch. M3 is used for the diode connection with M2, and M4 is used for blocking current through the OLED during the compensation period, respectively. We can modify this pixel circuit for all p-type TFT structures by adding an additional control line for M3, which can be more advantageous for manufacturing. The

operation of the proposed circuit is divided into two periods: data input and compensation period; emission period. The following statements depict each operating period. During the period before (1), the high- and low-voltage signals are applied to the Scan1 and Scan2, respectively. During this period, it is the previous frame operation for the same pixel and the DT voltage which was set to 0 V.

As shown in the period of Figure 2. Scan1 is set to the low level to turn on M1 and M3. Scan2 is set to high level to turn off M4 and M5 at the same time. The M2 gate node is connected to the M2 drain node. At present, the input signal (V_{data}), which is applied to data line (DT) delivered by M1, is stored on the left side of C1. In addition, by the M4 turnoff, we can turn off the OLED in this period to increase the OLED life time in long-time operation. Because of the diode-connected structure of M2, the M2 gate node becomes $V_{dd} - |V_{TH}|$, where V_{TH} is the M2 threshold voltage, and V_{dd} is the supply power line voltage. The stored voltage across C1 is set to $V_{dd} - |V_{TH}| - V_{data}$. The C1 reset and compensation stages can be finished at the same time in the period (1).

(2) *Emission Period.* As shown in the period (2) of the Figure 2. Scan1 is set to high level to turn off M1, and Scan2 is set to low level to turn off M3, while it turns on M4 and M5. The M2 drain node is connected to the OLED anode. The left side of C1 is connected to ground. Consequently, the M2 gate voltage will be boosted to $V_{dd} - |V_{TH}| - V_{data}$, coupling in the first period. Accordingly, I_{OLED} is determined by the V_{SG} of M2 and operated in the saturation region which becomes as follows:

$$\begin{aligned}
 I_{OLED} &= \frac{1}{2} K_{M2} (V_{SG} - |V_{TH}|)^2 \\
 &= \frac{1}{2} K_{M2} [V_{dd} - (V_{dd} - |V_{TH}| - V_{data}) - |V_{TH}|]^2 \\
 &= \frac{1}{2} K_{M2} (V_{data})^2, \quad \left(K = \mu C_{OX} \frac{W}{L} \right).
 \end{aligned} \tag{1}$$

Therefore, I_{OLED} is independent of the M2 threshold voltage variation and the voltage-drop of the power line (V_{dd}), only decided by V_{data} .

In addition, the time constant is well known as RC delay time. The minimum required time for period (1) is dependent on the RC value that you designed. Thus, the capacitance area will affect the aperture area in the pixel. The smaller the capacitance area is, the larger the aperture ratio is.

3. Proposed Circuit Simulation Results

To verify the effectiveness of the proposed 5T1C pixel circuit further, we did an AIM-SPICE simulation. The TFT model used in the simulation was poly-Si TFT Model PSIA2 (level 16). The OLED model is equivalent to a diode-connected poly-Si TFT and a capacitor. The M2 threshold voltage is set to -1 V. The M2 threshold voltage variation is set to ± 0.3 V to validate it in the worst-case process. To generate enough OLED output current, the width and length of M2 is designed as $10 \mu\text{m}$ and $4 \mu\text{m}$. The high- and low-level signals

Figure 4 shows the simulation results for the proposed 5T1C pixel circuit at different V_{data} (0.5–3.5 V) according to

FIGURE 5: Measurement results for OLED luminance degradation for each RGB element in conventional 2-TFT pixel circuit.

the M2 threshold voltage variation ($\Delta V_{TH} = \pm 0.3$ V, 0 V). Obviously, I_{OLED} is nearly independent of the threshold voltage variation. Moreover, the average I_{OLED} error rate in Figure 2 is 1.67%, while it is about 30–40% in the conventional 2-TFTs pixel.

Figure 5 shows the luminance data measured by PR-705 for the 2.2-inch QCIF ($176 \times \text{RGB} \times 220$) bottom-emission AMOLED panel, which is driven using p-type conventional 2-TFTs pixel. In this panel, V_{dd} side and I_{data} side were defined as the beginning and end of the supply power line, respectively. The luminance data is measured at V_{dd} side and I_{data} side, for each RGB elements, the luminance degradation rate, which is the luminance difference between V_{dd} side

FIGURE 6: Comparison of output current degradation rate versus V_{dd} drop for conventional 2T1C pixel circuit and proposed pixel circuit.

and I_{data} side, is about 70–80% at the input of $V_{dd} = 9$ V. The degradation of the measured luminance reveals that conventional panel which is driven by 2-TFT pixel seriously suffered from V_{GS} drop in driving TFT caused by power line $I \times R$ voltage-drop, which means the source terminal voltage of DTFT (V_{dd}) will cause the above phenomenon. The luminance uniformity is extremely dependent on the $I \times R$ voltage-drop. In addition, luminance uniformity and I_{OLED} are in direct proportion.

Figure 6 shows the simulation results of I_{OLED} degradation rate compared with conventional 2-TFTs pixel circuit. The initial V_{dd} was set to 9.5 V and the $I \times R$ voltage-drop of V_{dd} was set to 1 V, which means it decays from 9.5 V to 8.5 V. In the conventional 2-TFTs pixel, the I_{OLED} degradation rate is about 72%. It was found that the normalized degradation rate of the output current caused by the power line $I \times R$ voltage drop was apparently improved for the conventional and proposed pixel, respectively. In addition, the degradation rate of the output current, while V_{dd} drop of 0.3 V is improved by about 4%. We believe that our proposed pixel circuit can successfully solve both the threshold voltage variation and the power line $I \times R$ drop-voltage influence.

4. Conclusions

A new voltage programming pixel circuit was proposed for application to large-size, high-resolution AMOLED displays. The new pixel design can successfully compensate for the driving TFT threshold voltage non-uniform deviation. The average OLED output current error rate is about 1.67% when the threshold voltage is varied by ± 0.3 V. It also has less sensitivity to the supply power line voltage-drop than conventional p-type 2-TFT pixel designs.

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