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Research Article

Effect of Coercive Voltage and Charge Injection on Performance of a Ferroelectric-Gate Thin-Film Transistor

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We adopted a lanthanum oxide capping layer between semiconducting channel and insulator layers for fabrication of a ferroelectric-gate thin-film transistor memory (FGT) which uses solution-processed indium-tin-oxide (ITO) and lead-zirconium-titanate (PZT) film as a channel layer and a gate insulator, respectively. Good transistor characteristics such as a high "on/off" current ratio, high channel mobility, and a large memory window of 10^8, 15.0 $cm^2\ V^{-1}\ s^{-1}$, and 3.5 V were obtained, respectively. Further, a correlation between effective coercive voltage, charge injection effect, and FGT's memory window was investigated. It is found that the charge injection from the channel to the insulator layer, which occurs at a high electric field, dramatically influences the memory window. The memory window's enhancement can be explained by a dual effect of the capping layer: (1) a reduction of the charge injection and (2) an increase of effective coercive voltage dropped on the insulator.

1. Introduction

Ferroelectric-gate thin-film transistors (FGTs) have attracted much attention due to their nonvolatility, high write speed, low power consumption, and high endurance. Various types of FGTs composed of different stacked structures have been investigated [1–11]. Nevertheless, these devices exhibited very short retention time up to now, except for the case of epitaxial growth of the stacked ZnO/PZT/$SrRuO_3$ structure by pulsed laser processing [6, 12]. The main causes of the short retention time have widely been approved to be the effect of depolarization field from an interlayer and leakage current in the ferroelectric film on the Si surface channel [13–18]. In recent, the directly stacked oxide semiconductor/ferroelectric structure using pulsed laser processing is considered to be effective for forming a "clean" interface [6, 12, 19]. The costly pulsed laser processing, however, is unfavorable for industrial applications.

On the other hand, chemical solution processing can offer many advantages such as low fabrication cost, high throughput, large area deposition, direct patternability, and direct printing of devices. We have been challenging to use solution-processed indium-tin-oxide (ITO) as a channel layer with combination of ferroelectric PZT gate insulator for FGTs. However, it seems to be more difficult to obtain a "clean" solution-processed ITO/PZT interface as compared with its counterpart by means of vacuum process. That is because of component interdiffusion (such as Pb, Zr, Ti, and In) or reaction between ITO and PZT layer, which occurs even at as low as 450°C treatment [20–22]. In order to solve the interface problem, we have proposed the use of a lanthanum oxide (LO) as a capping layer between ITO and PZT to prevent the reaction and interdiffusion between these layers, as well as to improve the retention properties [23]. As a result, the ITO/LO/PZT interface with atomically flat and no undesirable interface layer was obtained. The fabricated device exhibited a typical n-channel memory transistor with a high "on/off" current ratio (I_{on}/I_{off}) of more than 10^8 and a large memory window (M_w) of 3.0 V.

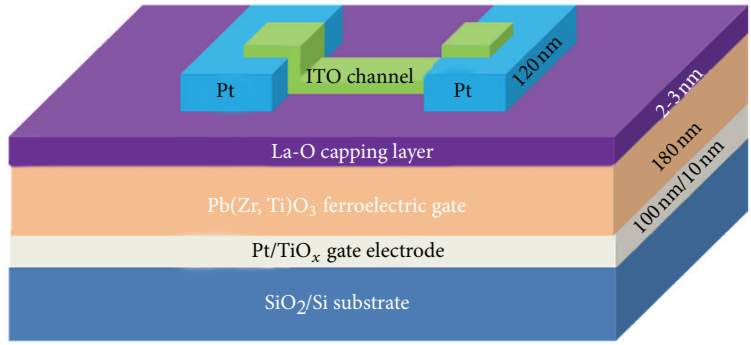

Figure 1: The cross-sectional structure of the fabricated FGT device.

Furthermore, in the ferroelectric-gate FETs, the memory window is theoretically equal to twice the coercive voltage [24]. However, in the practical cases, the memory window is not equivalent to double coercive voltage due to the voltage drop across an interlayer between the ferroelectric and the semiconductor. When a gate bias is applied to the ferroelectric gate structure, the unsaturated electric field applied to the ferroelectric film and the charge injection from the semiconductor to the interlayer can dominantly reduce the memory window because a high electric field is applied to the interlayer. Thus, it has usually suggested inserting a buffer insulator between the ferroelectric and the semiconducting channel, resulting in decreasing the electric field applied to the interlayer [25, 26]. In this work, the influence of coercive voltage and charge injection on device performance was investigated. It is found that the charge injection from the channel to the insulator layer dramatically influences on the memory window. The memory window's enhancement can be explained by a dual effect of the capping layer: (1) a reduction of the charge injection and (2) an increase of effective coercive voltage dropped on the insulator.

2. Experimental Details

To fabricate a FGT device, first Pt/Ti (100 nm/10 nm) film was deposited on a thermally grown SiO_2 (500 nm)/Si substrate by a radio-frequency magnetron sputtering as a bottom gate [27]. Then, PZT gate insulator (180 nm) was formed by the sol-gel method using alkoxide-based PZT (120/40/60) precursor solution (8 wt%, Mitsubishi Chemical Co.). This solution was spin coated and dried at 240°C in air for 5 min. The process was repeated 4 times to get the desire film thickness. After that, the PZT layer was crystallized at 600°C for 20 min in ambient air environment. Next, a LO layer was fabricated by spin coating using a nitrate-based precursor solution (0.1 mol/kg, Sigma-Aldrich Co.), and then slowly heated up to 550°C (10°C/min) and held for 10 min in O_2. In the following fabrication steps, Pt source and drain electrodes were sputtered at room temperature and patterned by a lift-off process. After that, an ITO layer (~30 nm) was deposited by spin-coating using carboxylate-based precursor solution (5 wt % SnO_2-doped, Kojundo Chemical Laboratory Co.) followed by annealing at 450°C for 30 min in air. Device region was patterned and isolated by the reactive ion etching. The channel length and width of the fabricated devices were 30 and 60 μm, respectively. For comparison, we also fabricated the conventional ITO/PZT sample by the solution process [23]. A cross-sectional structure of the fabricated FGT device is shown in Figure 1.

Cross-section high-resolution transmission electron microscope (HRTEM) image and selected area electron diffraction (SAED) patterns were obtained with a scanning TEM, JEM-ARM200F system (JEOL). Polarization-voltage (*P-V*) hysteresis loops of the PZT films were measured by a Ferroelectric Characterization Evaluation System (TOYO Corporation Model FCE-1). Capacitance-Voltage (*C-V*) measurements were carried out using a precision component analyzer (Wayne Kerr 6440B Model) at 1.0 kHz. Device characterization was carried out at room temperature by using a Semiconductor Parameter Analyzer (Agilent 4155C Model).

3. Results and Discussion

3.1. Structural and Electrical Properties of the Solution-Processed ITO/LO/PZT FGT Device. Figure 2 shows AFM images of the conventional PZT (Figure 2(a)) and new LO/PZT surface (Figure 2(b)). We found that the LO/PZT surface, which consisted of small and uniform grains, was much smoother than the conventional PZT surface. Namely, the RMS values of the conventional PZT and the new LO/PZT surface were 2.28 nm and 0.63 nm, respectively. Also, this difference in surface roughness can be clearly seen when comparing 3D-AFM images of the PZT and LO/PZT surface as shown in the insets. From this result one can expect that the carrier scattering at the interface between ITO and LO/PZT layers would be less than that in the conventional ITO/PZT structure.

The cross-sectional image of the ITO/LO/PZT structure by HRTEM exhibited an atomically flat interface with no defective layer (Figure 3). The thickness of the LO layer was as thin as 2-3 nm. In addition, the high angle annular dark-field scanning TEM (HAADF-STEM) image and the TEM-EDX line analysis crossing ITO/LO/PZT interfaces apparently showed high uniformity of PZT layer and negligible out-diffusion of Pb, Zr, and Ti elements. Also, two dimensional

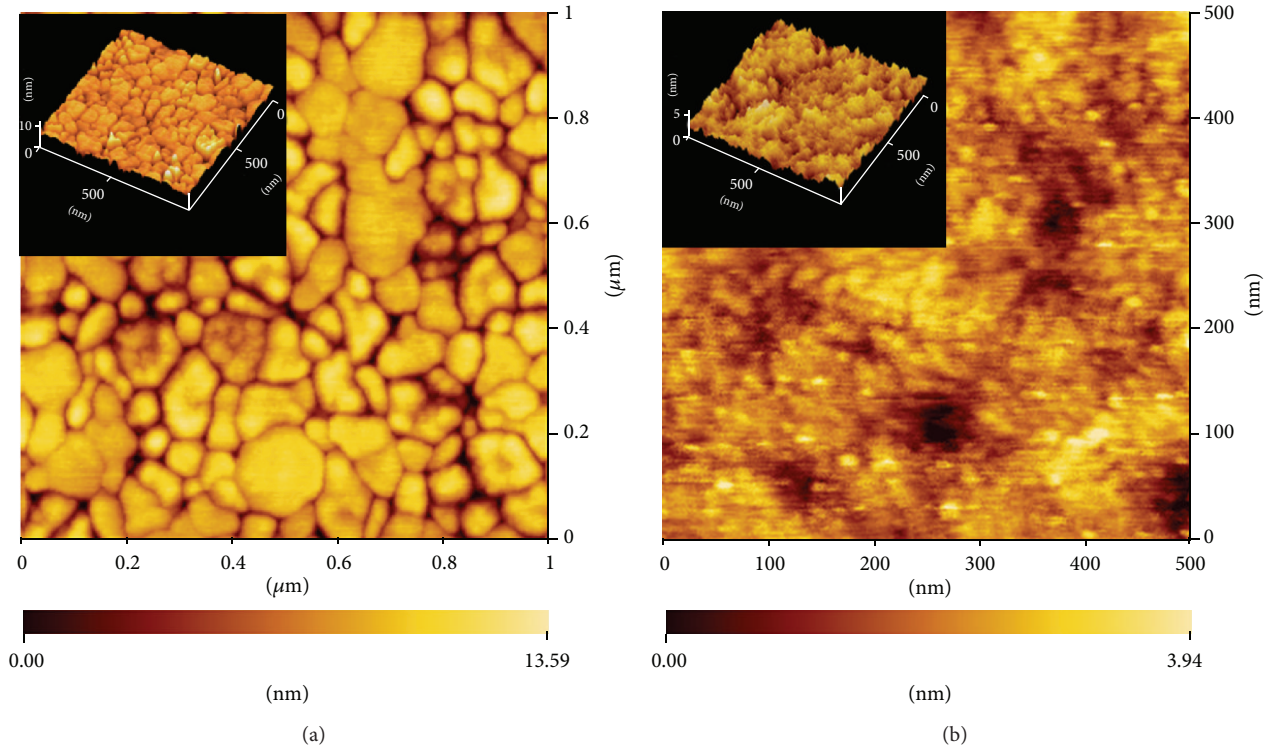

Figure 2: AFM images of (a) PZT and (b) LO/PZT surface. The insets of (a) and (b) are 3D-topography images, respectively.

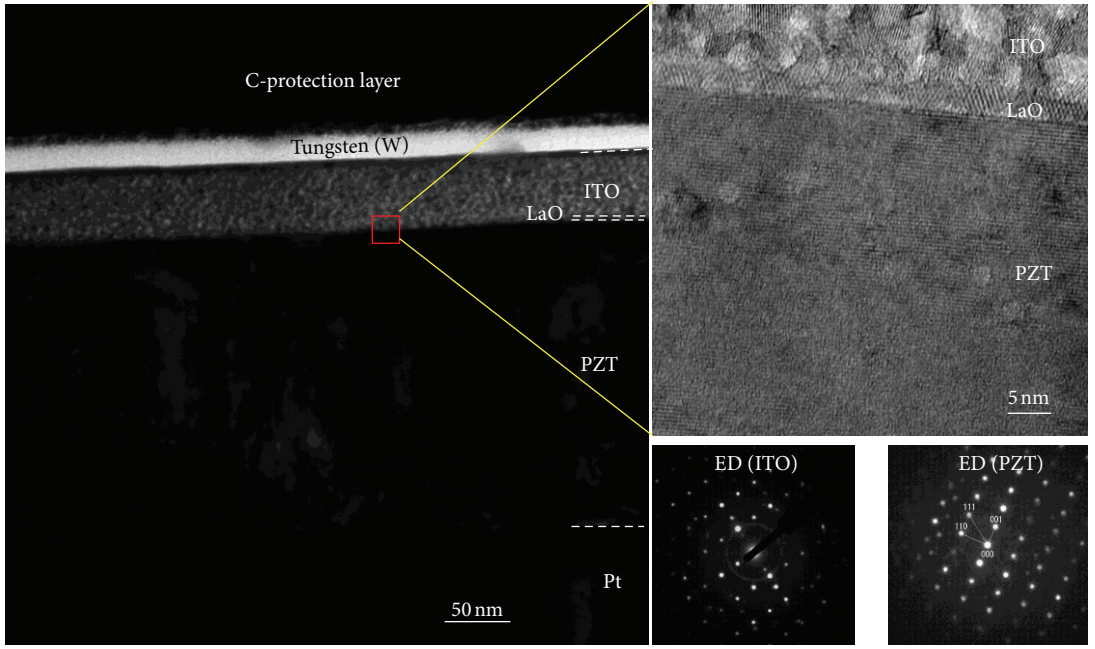

Figure 3: Cross-sectional HR-TEM images of the ITO/LO/PZT/PT stacked structure and electron diffraction patterns of ITO and PZT layers.

(2D) EDX element mapping exhibited homogeneous compositional distribution of the ITO and PZT layers (not shown here) [19]. In contrast, a HRTEM image at ITO/PZT interface revealed an amorphous interlayer having a thickness of 7–10 nm. In addition, approximately 10 at % loss of Pb and Ti atoms were observed in 10 nm thickness from the PZT surface by their diffusion into the ITO layer. Therefore, the ITO layer actually contains Pb atoms as impurity [19, 21]. The electron diffraction patterns of ITO and PZT layers indicate their polycrystalline structures, which are consistent with

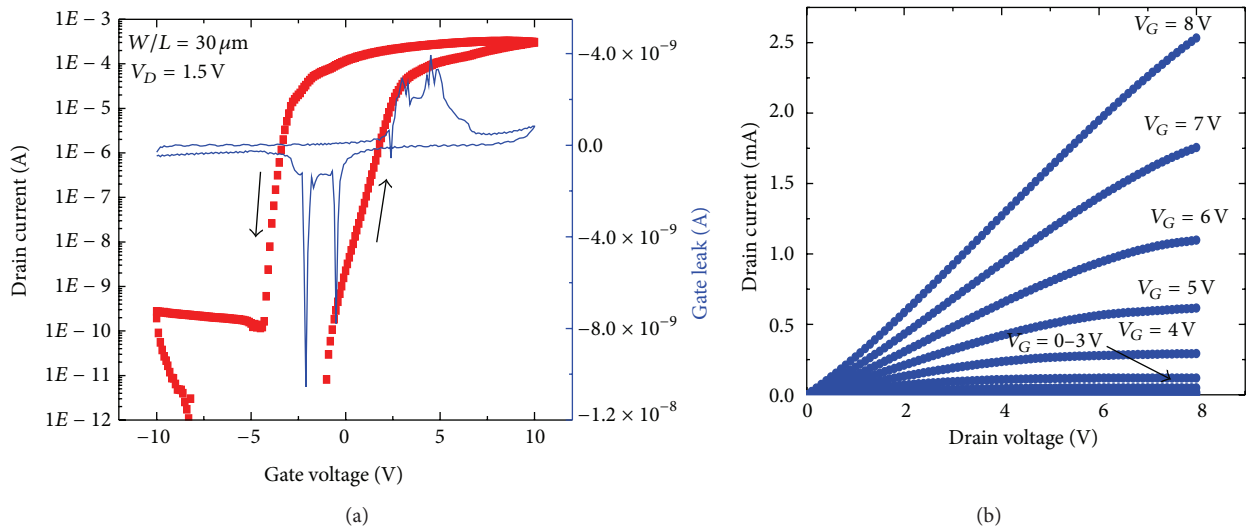

FIGURE 4: (a) Transfer and (b) output characteristics of the fabricated FGT device.

XRD analysis, with preferential orientation of (222) and (111), respectively.

Figure 4 shows the transfer (I_D-V_G) and output (I_D-V_D) characteristics of the fabricated FGT device. The I_D-V_G curve exhibited counterclockwise hysteresis loop due to ferroelectric polarization of the PZT as indicated by the arrows, which confirmed the nonvolatile memory function of this device. The I_D-V_D curve shows a typical n-type transistor behavior with a good drain current saturation. We can see that the gate leakage currents (in both negative and positive regions) are relatively small (~10 pA). The observed peaks in the gate leakage current resulted from the polarization currents of the ferroelectric PZT layer. Therefore, we may consider that the rounded behaviour in the transfer curve at the negative region is not mainly caused by the gate leakage current. Once the device is turned on, it is not completely switched off as the negative voltage applied, leading to the rounded characteristic. We speculate that carriers in some part of the channel layer might not be completely depleted.

In the conventional ITO/PZT structure, a relatively large I_{on}/I_{off} ratio was obtained but the drain current ratio, that is, the binary states, at a zero gate voltage, which is indispensable for nonvolatile memories, was not sufficiently large owing to a shift in the threshold voltage to the negative voltage side [19, 21, 23, 25]. On the other hand, the new ITO/LO/PZT structure presented an excellent I_{on}/I_{off} and a ΔV_{th} of more than 10^8 and 3.5 V, respectively, which are much better than those of previous reported FGTs [1–6]. The field-effect mobility of 15.0 $cm^2\ V^{-1}\ s^{-1}$ was estimated from the saturation region of the device's output characteristics, which is comparable to or higher than other reported oxide-channel TFTs by means of vacuum processes [1, 12]. Furthermore, the threshold voltage from a negative bias to a positive one was very close to a zero gate voltage, which indicated that the amount of space charge in the PZT film and at the ITO/LO/PZT interfaces was relatively low [12].

It was demonstrated that the LO layer acted as a good barrier film not only for preventing the interdiffusion between the ITO semiconductor and PZT insulator layers, but also for stabilizing the PZT surface structure. We speculate that La^{3+} ions are incorporated into PZT structure by substituting for Pb^{2+} ions, which effectively stabilizes PZT structure by preventing Pb evaporation and formation of oxygen vacancies. Consequently, the interdiffusion between ITO and PZT layers were suppressed resulting in good ITO/PZT interface properties [23].

3.2. Analysis on the Influence of Charge Injection on the Memory Window of the ITO/LO/PZT FGT Device. In the ferroelectric-gate structure, a differential form of Gauss's law describes the relationship between the maximum electric field in the semiconducting layer, E_{sc}, the ferroelectric displacement, D_{fe}, and any free charge, Q_i, which might reside near the ferroelectric/semiconductor interface [28]:

$$\varepsilon_{sc} E_{sc} = Q_i + D_{fe}, \tag{1}$$

where ε_{sc} is the dielectric constant of the semiconductor. Depending on the signs of D_{fe} and Q_i, the semiconducting layer may either be inverted, depleted, or accumulated. D_{fe} is known from ferroelectric hysteresis measurements. Typical values of E_{sc} calculated from (1) are so large that it is probable that some carriers will be injected into the ferroelectric. For our case, the relative dielectric constant of the semiconductor is approximately 10, and D_{fe} is 30 $\mu C/cm^2$, then E_{sc} is ~3 × 10^7 V/cm This injected "homocharge" is opposite in site to D_{fe}, and if it becomes trapped (as Q_i), E_{sc} will drop, slowing the injection process. Consequently, we might anticipate that interface charge could play a role in device operation.

Figure 5(a) shows the *P-V* hysteresis loops of the Pt/LO/PZT/Pt capacitor. As clearly seen, as increasing applied voltage both the coercive voltage and remnant polarization value increase due to switching of ferroelectric

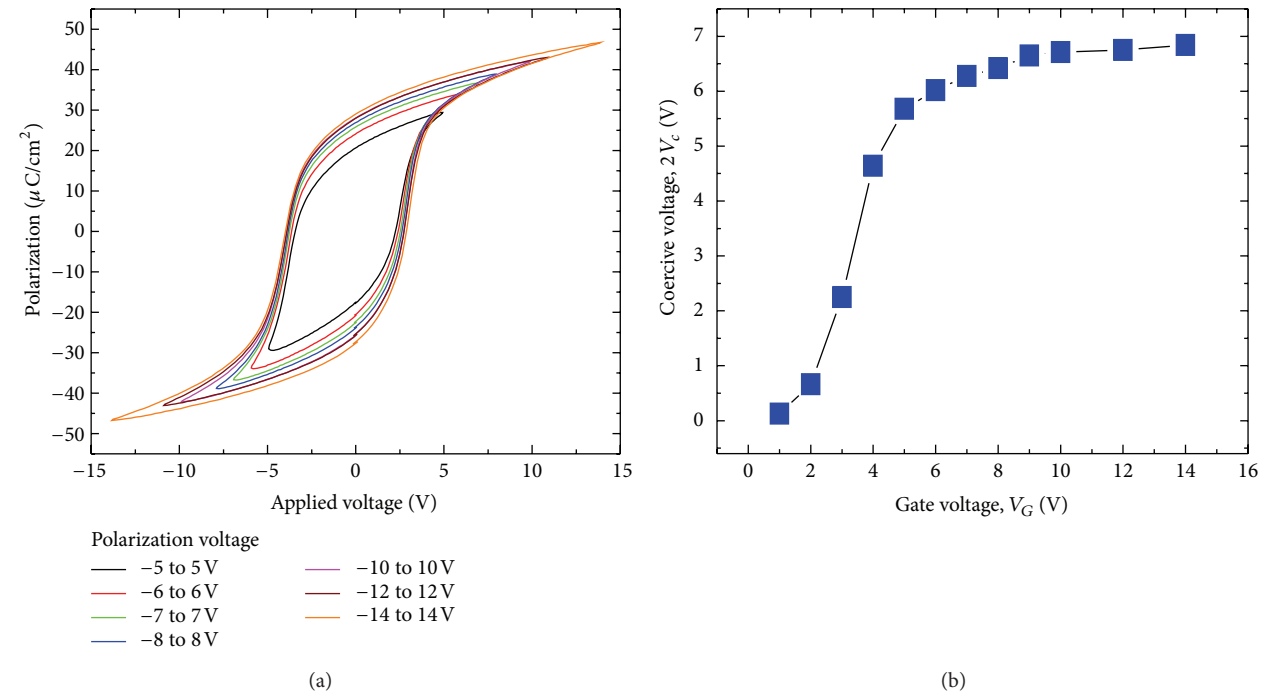

FIGURE 5: (a) *P-V* hysteresis loops and (b) the twice of the coercive voltages of the Pt/LO/PZT/Pt capacitor.

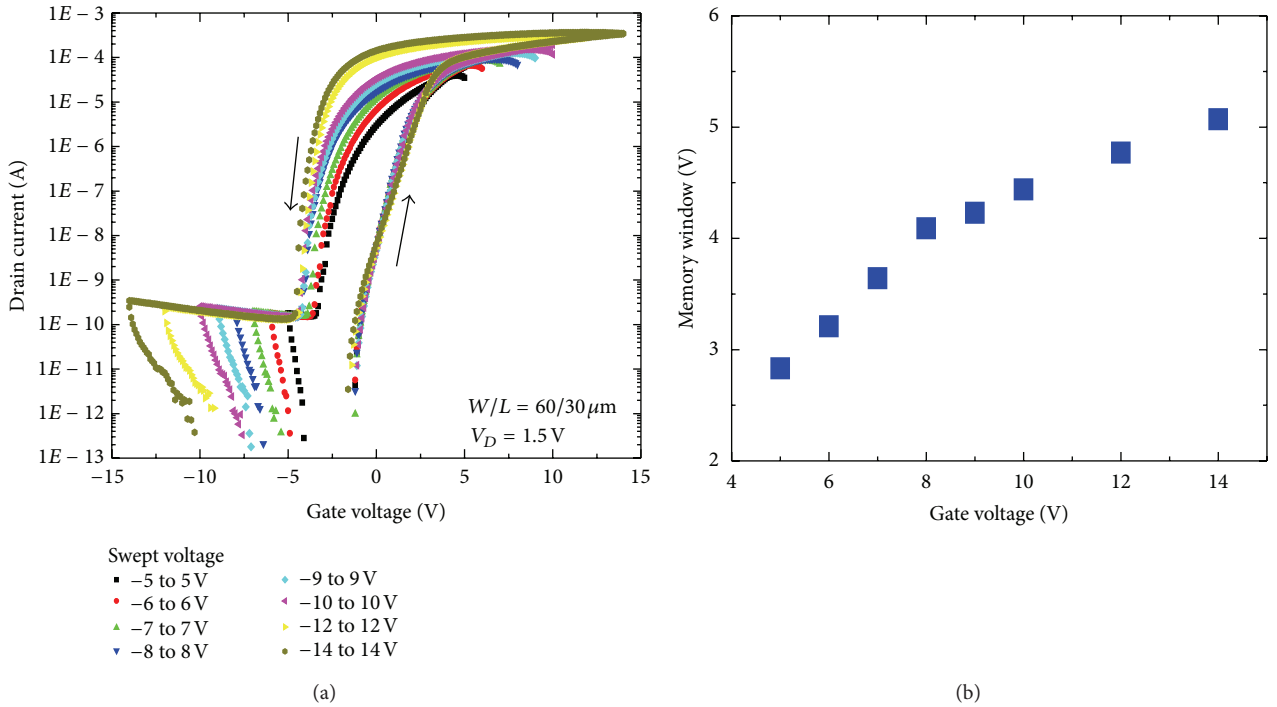

FIGURE 6: (a) Transfer curves and (b) memory window as a function of gate sweep voltage.

domains. A variation of the coercive voltage as a function of the applied voltage is summarized in Figure 5(b), which indicates that hysteresis loops get saturated at approximately 5 V.

Figure 6(a) shows the transfer characteristics of the ITO/LO/PZT FGT device when the gate voltage was swept from ±5 to ±14 V. Increasing the gate voltage, the memory window increases symmetrically, which reveals the excellent ferroelectric polarization switching property. Figure 6(b) summarizes the change of memory windows as a function of gate voltage.

As mentioned above, the memory is severely reduced by the charge injection from the ITO into the interlayer between ITO and PZT layers. The following relationship

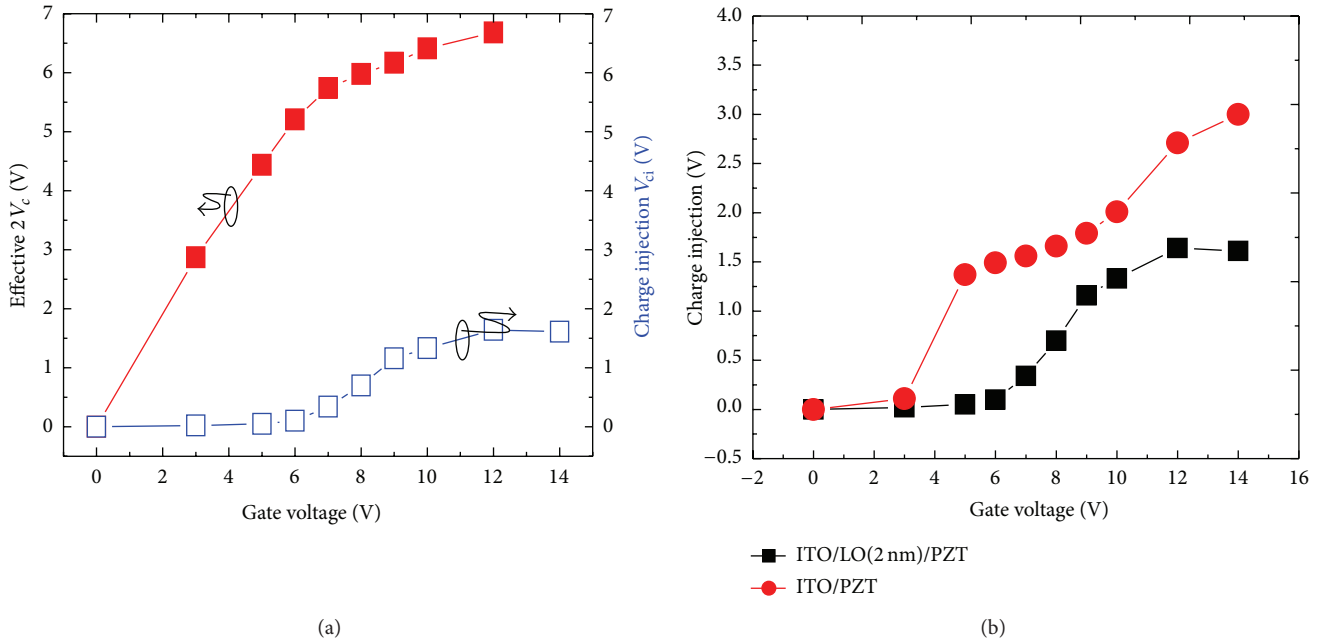

FIGURE 7: Effective coercive voltage ($2V_c$) applied to PZT films and reduction values ($2V_c - V_m$) of memory window by charge injection in the ITO/LO/PZT structure. The values of charge injection are $2V_c - V_m$ at the same gate voltage, where $2V_c$ is twice the coercive voltage at the real applied voltage on the PZT film only.

clearly expresses how much the memory window will be reduced:

$$V_m = 2V_c - V_{ci}, \tag{2}$$

where V_m is the memory window, $2V_c$ is the effective double coercive voltage, and V_{ci} is the flat band voltage shift due to charge injection. Here, the effective coercive voltage can be derived from Figure 5(a) after calculating the voltage distribution across the series capacitance consisting of the PZT, LO, and ITO layer. We have determined the effective voltage applied to the capacitor by following relations:

$$V_f = \frac{\varepsilon_s \varepsilon_i d_f}{\varepsilon_s \varepsilon_i d_f + \varepsilon_s \varepsilon_f d_i + \varepsilon_f \varepsilon_i d_s} V_G,$$

$$V_i = \frac{\varepsilon_s \varepsilon_f d_i}{\varepsilon_s \varepsilon_i d_f + \varepsilon_s \varepsilon_f d_i + \varepsilon_f \varepsilon_i d_s} V_G, \tag{3}$$

$$V_s = \frac{\varepsilon_i \varepsilon_f d_s}{\varepsilon_s \varepsilon_i d_f + \varepsilon_s \varepsilon_f d_i + \varepsilon_f \varepsilon_i d_s} V_G,$$

where V, ε, and d are the effective voltages applied to the capacitor, the dielectric constant, and the thickness, respectively. The subscripts of i, s, f, and G stand for the insulator (LO), semiconductor (ITO), ferroelectric (PZT), and gate, respectively.

To calculate the dielectric constants of the capacitors, we assumed a dielectric constant value of the 7 nm-thick interlayer between ITO and PZT films to be 5. The thickness and dielectric constant of the LO layer are 2 nm and 27, respectively. Based on the equivalent circuit of the ITO/LO/PZT structure, the calculated dielectric constants of PZT and ITO using the accumulation region of the *C-V* curve are about 457.6 and 50.8, respectively. Using these values and (3) we can calculate the electric field distribution in the series capacitor as follows: $V_f = 0.493V_g$ and $V_i = 0.246V_g$. Using (2) we can extract the $2V_c$ and the V_{ci} dependence on the gate voltage as shown in Figure 7(a).

Figure 7(a) shows a dependence of the effective coercive voltage and the charge injection on the gate voltage. It is found that the ITO/LO/PZT structure causes the memory window enhancement due to the increase in the $2V_c$ and the decrease in the V_{ci}. Interestingly, when the gate bias goes up to 7 V the $2V_c$ seems to be saturated and the V_{ci} starts to rise from zero. Increasing the gate voltage led to the slight change of V_{ci}. There was no severe charge injection observed even when the gate voltage rises up to 14 V, which can be confirmed by the measurement of the memory window as shown in Figure 6(b).

As for the conventional ITO/PZT structure, the calculated voltage distributions across the series capacitance consisting of the PZT, interlayer ($d_i \sim 5, t_i \sim 7$ nm), and ITO layer are $V_f = 0.189V_g$ and $V_i = 0.711V_g$. Therefore, most of the applied voltage dropped on the interlayer, which may cause severe charge injection from the semiconductor layer to it. As shown in Figure 7(b), the charge injection in the conventional structure was severely raised at a rather small V_g of about 4 V.

This result suggests that the memory window can be enhanced by adjusting the LO layer thickness or thickness ratio of LO to PZT layer. Inserting a thin LO layer, although the effect field on the PZT is reduced, the memory window of the ITO/LO/PZT structure increases since the electric field

applied to the interlayer decreases, resulting in the reduction of charge injection.

4. Conclusion

We fabricated and investigated operation of a solution-processed ITO-channel ferroelectric-gate thin-film transistor memory (FGT) which uses the LO as a capping layer. Good transistor characteristics such as a high "on/off" current ratio, high channel mobility, and a large memory window of 10^8, 15.0 $cm^2\ V^{-1}\ s^{-1}$, and 3.5 V were obtained, respectively. The impacts of effective coercive voltage and charge injection effect on the FGT's performance were also investigated. The experimental and theoretical analysis reveals that the memory window equals the difference between the effective coercive voltage ($2V_c$) ($2V_c$) applied to the ferroelectric film and the flat band voltage shift due to charge injection (V_{ci}). The memory window's enhancement can be explained by a dual effect of the capping layer: (1) a reduction of the charge injection and (2) an increase of effective coercive voltage dropped on the insulator.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this article.

Acknowledgments

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