Research Article

Study of Interface Charge Densities for ZrO$_2$ and HfO$_2$ Based Metal-Oxide-Semiconductor Devices

N. P. Maity, Reshmi Maity, R. K. Thapa, and S. Baishya

1 Department of Electronics & Communication Engineering, Mizoram University (A Central University), Aizawl 796004, India
2 Department of Physics, Mizoram University (A Central University), Aizawl 796004, India
3 Department of Electronics & Communication Engineering, National Institute of Technology, Silchar 788010, India

Correspondence should be addressed to N. P. Maity; maityniladri@rediffmail.com

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A thickness-dependent interfacial distribution of oxide charges for thin metal oxide semiconductor (MOS) structures using high-$k$ materials ZrO$_2$ and HfO$_2$ has been methodically investigated. The interface charge densities are analyzed using capacitance-voltage ($C$-$V$) method and also conductance ($G$-$V$) method. It indicates that, by reducing the effective oxide thickness (EOT), the interface charge densities ($D_{it}$) increases linearly. For the same EOT, $D_{it}$ has been found for the materials to be of the order of $10^{12} \text{cm}^{-2} \text{eV}^{-1}$ and it is originated to be in good agreement with published fabrication results at p-type doping level of $1 \times 10^{17} \text{cm}^{-3}$. Numerical calculations and solutions are performed by MATLAB and device simulation is done by ATLAS.

1. Introduction

A MOS device is generally fabricated by oxidizing a Si substrate and depositing a conducting film on the resulting amorphous SiO$_2$ layer, forming the gate. The fabrication process always introduces defects at the SiO$_2$- Si boundary that critically affects the device characteristics of both the diode and the transistor. Increasing the size of wafer and decreasing the size of device, that is device scaling, are sensible approaches to reduce the cost. According to International Technology Roadmap for Semiconductor (ITRS), the next generation Si-based MOS device will require oxide thickness $\sim 1 \text{ nm}$. With the ever-increasing requirement for speed and density of silicon integrated circuits (ICs), MOS device scaling has become a primary concern of the semiconductor manufacturing industry. But there are some essential scaling limits with the ultrathin oxide. The leakage current (tunneling current) increases exponentially with the reduction of gate insulator thickness that in turn results in intolerable power consumption and device performance problems. As a result, the scaling limit of SiO$_2$ depends on both the elementary physics and accessible technology. It has been aimed towards achieving higher speed, lower power, lower cost, and higher density. Since the scaling of MOS devices utilizing SiO$_2$ as gate material has reached its limit, there is a prospect in thinning the electrical oxide thickness by using high-$k$ dielectric material and/or metal gates to achieve a greater physical thickness and thus reducing the direct tunneling current while retaining a low oxide thickness [1–4]. Several insulator materials of gate in the lanthanum group exhibiting higher dielectric constant as shown in Table 1, in the range of 7–30, have been proposed as prospective candidates for gate dielectric and show outstanding results.

There are many requirements that need to be satisfied before a new material is acceptable to the semiconductor industry for its use as gate dielectric. Though high-$k$ dielectric materials look very promising, there are certain challenges and issues that have to be met before successful transition from SiO$_2$ to high-$k$. The key guidelines for selecting an alternative dielectric are permittivity, band gap, band alignment to Si, thermal stability, film morphology, interface quality, compatibility with the current or expected materials to be used in processing for MOS devices, process compatibility, and reliability. In attempt to replace conventional SiO$_2$ with new high-$k$ materials, HfO$_2$ and ZrO$_2$ have received
tremendous attention and are quite promising materials [5–8] considering their permittivity and conduction band offsets values.

High-\(k\) materials often suffer from poor electrical quality of the oxide dielectric-semiconductor interface and are often associated with lower dielectric breakdown voltages and decreased lifetimes. Moreover, with the introduction of high-\(k\) materials there occurs formation of interface charges. Due to the scaling, it has become very significant to consider the effect of generated traps in Si-SiO\(_2\) junction. The use of high-\(k\) gate dielectric generates a large number of interface traps at the surface channel and oxide trap charges in the gate dielectric bulk of MOS transistors, which would result in the degradation of device electrical characteristics. As the oxide thickness is reduced these interface trap charges become significant gradually. During the last three decades, gate oxide thickness was so large that this phenomenon was not noticeable, but nowadays it is a matter of importance to consider the interface states during MOS operation [9–12]. In this paper the interface charge densities have been measured and analyzed for thin MOS structure using ZrO\(_2\) and HfO\(_2\) high-\(k\) materials as gate dielectric.

### 2. Theoretical Analysis

Contributions are judged in terms of their extensive and debasing effect on the operational behavior of MOS devices; oxide-semiconductor interfacial traps must be considered as the most significant nonideality encountered in the MOS structure. Interface traps are allowed energy states in which electrons are localized in the vicinity of a material's surface. All of the bulk centers are found to add levels to the energy band diagram within the forbidden band gap. SiO\(_2\) is often treated as an ideal insulator, where there are no traps or states at the interface of Si/SiO\(_2\). But in real devices, the Si/SiO\(_2\) interface and bulk SiO\(_2\) are far from being electrically neutral. These may be caused by positive or negative charges at the Si/SiO\(_2\) interface or by mobile ionic charges and fixed charges trapped within the oxide and itself, which are often created during the fabrication process. In reality, there are two types of charges that are associated with oxide layer, namely, interface trap charge and oxide charge. These charges play an important role affecting the physical and electrical properties of a MOS device. The features that distinguish interface trap charge from oxide charge are that interface charge varies with gate bias whereas oxide charge is independent of gate bias. The two thus have different effects on C-V characteristics. There are three types of oxide charges associated with the SiO\(_2\)-Si system. They are fixed oxide charge, mobile oxide charge, and oxide trapped charge. All of these charges are very much dependent on the device fabrication process. Already in the pioneering work for understanding the physical properties of MOS structures, the capacitance-voltage (C-V) method was used to establish the main qualities of oxide-silicon interfaces.

Three insulator related parameters typically determined with C-V measurement are (1) oxide charge density, \(\rho_{ox}\), (2) interface trap density, \(Q_{it}\), and (3) gate semiconductor work function difference, \(\theta_{ms}\). They are determined from the flatband voltage:

\[
V_{FB} = \theta_{ms} - \frac{1}{\varepsilon_{ox}\varepsilon_o} \int_0^{t_{ox}} x \rho(x) \, dx, \tag{1}
\]

where \(\varepsilon_{ox}\) is the permittivity of the oxide, \(\varepsilon_o\) is the permittivity of the free space, and \(t_{ox}\) is the oxide thickness. The fixed charge density \(Q_f\) and interface trap density \(Q_{it}\) (function of surface potential, \(\theta_i\)) are assumed to be located at the SiO\(_2\)/Si interface and the remaining mobile ionic and oxide trap charge density, \(\rho_{ox}\), in the SiO\(_2\), leading to the flatband voltage expression for uniform oxide charge density,

\[
V_{FB} = \theta_{ms} - \frac{Q_f + Q_{it}(\theta_i)}{\varepsilon_{ox}\varepsilon_o} t_{ox} - \frac{\rho_{ox}}{2\varepsilon_{ox}\varepsilon_o} t_{ox}^2. \tag{2}
\]

On assuming that only \(Q_{it}\) is present in the oxide layer, then the equation becomes

\[
V_{FB} = \theta_{ms} - \frac{Q_{it}(\theta_i)}{\varepsilon_{ox}\varepsilon_o} t_{ox}. \tag{3}
\]

But the most accurate and very sensitive method to extract the \(D_{it}\) is the conductance method. Recently, the conductance method has been investigated and adapted for rigorously proving the electrical passivation of novel semiconductor-dielectric interfaces. The equivalent circuits [12] for conductance measurement in MOS capacitor are

<table>
<thead>
<tr>
<th>Material</th>
<th>(k)</th>
<th>Band gap, (E_g) (eV)</th>
<th>Band offset to Si (eV)</th>
<th>Crystal structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO(_2)</td>
<td>3.9</td>
<td>9</td>
<td>3.5</td>
<td>Amorphous</td>
</tr>
<tr>
<td>Si(_3)N(_4)</td>
<td>7</td>
<td>5.3</td>
<td>2.4</td>
<td>Amorphous</td>
</tr>
<tr>
<td>Al(_2)O(_3)</td>
<td>9.3</td>
<td>8.8</td>
<td>2.8</td>
<td>Amorphous</td>
</tr>
<tr>
<td>HfSiO(_4)</td>
<td>15</td>
<td>6</td>
<td>1.5</td>
<td>Amorphous</td>
</tr>
<tr>
<td>Y(_2)O(_3)</td>
<td>15</td>
<td>6</td>
<td>2.3</td>
<td>Cubic</td>
</tr>
<tr>
<td>ZrSiO(_4)</td>
<td>15</td>
<td>6</td>
<td>1.5</td>
<td>Amorphous</td>
</tr>
<tr>
<td>HfO(_2)</td>
<td>22</td>
<td>6</td>
<td>1.5</td>
<td>Monoclinic, tetragonal</td>
</tr>
<tr>
<td>ZrO(_2)</td>
<td>22</td>
<td>5.8</td>
<td>1.4</td>
<td>Monoclinic, tetragonal</td>
</tr>
<tr>
<td>Ta(_2)O(_5)</td>
<td>26</td>
<td>4.4</td>
<td>0.3</td>
<td>Orthorhombic</td>
</tr>
<tr>
<td>La(_2)O(_3)</td>
<td>30</td>
<td>6</td>
<td>2.3</td>
<td>Hexagonal, cubic</td>
</tr>
</tbody>
</table>
given in Figure I. Figure I(a) consists of the oxide (insulator) capacitance per unit area ($C_{ox}$), semiconductor capacitance per unit area ($C_s$), interface trap capacitance per unit area ($C_{it}$) and interface trap resistance per unit area ($R_t$). For the MOS interface charge analysis it is convenient to replace the circuit of Figure I(a) with Figure I(b): here $C_p$ is the equivalent parallel capacitance and the $G_p$ is the equivalent parallel conductance.

So the admittance of Figures I(a) and I(b) is given by

$$Y_a = j\omega C_s + \frac{j\omega D_{it}}{1 + j\omega \tau_{it}} \left(1 - j\omega \tau_{it}\right),$$

$$= j\omega C_s + \frac{j\omega D_{it}}{1 + (\omega \tau_{it})^2},$$

$$Y_p = j\omega C_p + G_p,$$

where $\omega = 2\pi f$ ($f$ is measured frequency), $C_{it} = qD_{it}$, and $q$ is the magnitude of electronic charge.

If the real part and imaginary part are compared, respectively, we get

$$\frac{G_p}{\omega} = \frac{q\omega \tau_{it} D_{it}}{1 + (\omega \tau_{it})^2},$$

Dividing $G_p$ by $\omega$ makes it symmetrical in $\omega \tau_{it}$ and $G_p/\omega$ is directly related to $D_{it}$. It is more effective to calculate $D_{it}$ [12], because it has only a parameter related to interface trap without including $C_s$. This equation considers the interface trap with single energy level in the band gap. For continuously distributed interface charge, we have to consider Figure I(c), consisting of the measured equivalent parallel conductance ($G_m$) and measured capacitance ($C_m$). Using this circuit, $G_p/\omega$ value (assuming negligible series resistance and tunnel conductance) is given,

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2(C_{ox} - C_m)^2}.$$  

$D_{it}$ can be calculated from the obtained $G_p/\omega$ versus $f$ graph from (5). At maximum $G_p/\omega$, the $\omega$ is the inverse of $\tau_{it}$; approximate expression of $D_{it}$ can thus be given in terms of the measured maximum conductance as

$$D_{it} = \frac{2}{q} \left[ \frac{G_p}{\omega} \right]_{\text{max}}.$$  

3. Results and Discussion

Five groups of p-substrate MOS devices have been analyzed consisting of two high-$k$ dielectric materials, ZrO$_2$ and HfO$_2$, having the dielectric constant of 22 for amorphous structure of the materials [13]. These materials were studied for different EOT at p-type doping level of $1 \times 10^{12}$ cm$^{-3}$. If a high-$k$ material can replace SiO$_2$, the dielectric thickness increases proportionally to keep the equal dielectric capacitance and EOT is the thickness of any dielectric material scaled by the ratio of its dielectric constant to the dielectric constant of SiO$_2$ ($k = 3.9$). $Q_{it}$ can be extracted from the slope of plot between flatband voltages and oxide thickness. By considering presence of only interface charge at the oxide-semiconductor interface the value of $Q_{it}$ has been calculated theoretically and through simulation. Figure 2 shows the plot of magnitude of the flatband voltage as function of EOT for the high-$k$ materials.

The graphs shown in Figure 2 clearly demonstrate the validity of our assumption in (3). The flat-band voltage of all the samples indicated negative value due to the existence of deep donor type surface states and positive interface charges. This noticeably indicates the presence of some parasitic charges at the interface. The deviation of simulated result from the theoretical result was found due to the high dielectric value of the materials. The theoretical interface charge $Q_{it}$ present in each of the MOS capacitor was $5 \times 10^{10}$ C at the interface. The simulated result obtained is shown in Table 2. Using the simulated $C$-$V$ and $G$-$V$ characteristics curve the values of the $C_m$ and $G_m$ have been measured,
The value of $D_{it}$ has been calculated using conductance method. It is a technique which replaces MOS capacitor with equivalent circuit model and calculates $D_{it}$. Using the $G$-$V$ curve conductance of the MOS has been calculated in depletion region of $-1$ V.

Figures 5(a) and 5(b) show the relationship of $G_{p}/\omega$ versus $f$ using ZrO$_2$ and HfO$_2$ high-$k$ material of EOT at 1.77 nm, 2.65 nm, and 3.54 nm, respectively. This figure shows that the local maximum of each curve indicates the magnitude of $D_{it}$. The peaks of the curves used for the oxide materials mean that the interface state energy levels are measured. Both $G_{p}/\omega$ and $G_{p}$ will peak as a function of bias voltage at gate terminal but only $G_{p}/\omega$ will peak as a function of frequency. $G_{p}/\omega$ will peak at a lower frequency when admittance is measured as a function of frequency with bias voltage at the gate as parameter or at the gate bias near to flatbands and when admittance is measured as a function of bias voltage at the gate with frequency as respectively, and the variation with frequency for the high-$k$ dielectric materials has been shown in Figures 3 and 4.

<table>
<thead>
<tr>
<th>Material</th>
<th>$Q_1$</th>
<th>$Q_2$</th>
<th>$Q_3$</th>
<th>$Q_4$</th>
<th>$Q_5$</th>
<th>$Q_6$</th>
<th>$Q_{avg}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZrO$_2$</td>
<td>1.355e11</td>
<td>1.400e11</td>
<td>1.436e11</td>
<td>1.314e11</td>
<td>1.266e11</td>
<td>1.363e11</td>
<td>1.356e11</td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>1.379e11</td>
<td>1.400e11</td>
<td>1.582e11</td>
<td>1.278e11</td>
<td>1.339e11</td>
<td>1.217e11</td>
<td>1.366e11</td>
</tr>
</tbody>
</table>
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Parameter. The characteristics of the graph are the same for these two materials and the \( G_p/\omega \) is maximum at \( 10^{10} \) Hz. \( D_n \) was calculated for the different EOT for ZrO\(_2\) and HfO\(_2\). The increase in \( D_n \) is observed as the EOT is reduced as shown in Table 3 for a particular frequency of 1 MHz. This depicts that \( D_n \) increases as the EOT reduces because density of trap charges is concentrated at the interface.

Figures 6(a) and 6(b) show the relationship between \( D_n \) and \( f \) for ZrO\(_2\) and HfO\(_2\) high-\( k \) material, respectively. The value of \( D_n \) has been calculated at different frequencies using (5). At smaller frequencies the \( D_n \) has a constant and high value. As the frequency reaches the inverse of interface trap time constant, the \( D_n \) starts decreasing and at very high frequencies the value goes to a saturation region. The high value of \( D_n \) at lower frequencies and a low value at higher frequencies are because trap charges are able to follow low frequencies and as the frequency increases trap charges cannot follow it so it does not contribute to \( D_n \) at the large

<table>
<thead>
<tr>
<th>Parameter</th>
<th>ZrO(_2) (cm(^{-2}) ev(^{-1}))</th>
<th>HfO(_2) (cm(^{-2}) ev(^{-1}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>EOT (nm)</td>
<td>( \begin{array}{c} 1.77 \quad 7.53E + 12 \quad 7.64E + 12 \ 2.65 \quad 6.18E + 12 \quad 6.26E + 12 \ 3.54 \quad 5.14E + 12 \quad 5.21E + 12 \end{array} )</td>
<td></td>
</tr>
</tbody>
</table>
frequencies. The $D_n$ is predicted by conductance method for HfO$_2$ with molecular beam deposition (MBD) process and for ZrO$_2$ with atomic layer deposition (ALD) technique which is in resemblance to the fabrication results [14] at p-type doping level of $1 \times 10^{17}$ cm$^{-3}$.

4. Conclusions

The flatband voltage of all the samples indicated negative value due to the existence of deep donor type surface states and positive interface charges, and these effects are highly responsible for variation in $D_n$ with EOT. The interface charge densities have been calculated using $C$-$V$ method as well as conductance method and it has been found that as the thickness of the oxide is reduced, the interface trap density increases for both HfO$_2$ and ZrO$_2$. This increase in $D_n$ by reducing the oxide thickness clearly demonstrates that the interface between oxide and silicon gets weaker.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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