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Research Article

A Split Island Layout Style of Butting/Inserted Substrate Pickups for NMOSFET ESD Reliability

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Butting/inserted pickup layout style could result in severe ESD degradation of NMOS devices beyond deep submicron technology. A split island layout style of butting/inserted substrate pickups is designed for a multifinger NMOS structure to enhance its ESD reliability. This layout style divides the substrate pickup diffusion bands along the whole polygate finger direction into segmented diffusion islands in the source area. This layout technique could improve the TLP second breakdown current of the 1.8 V butting pickup structure by 58~66% and 1.8 V/3.3 V inserted pickup case by 2.8 times. This style also shows excellent enhancement for the ESD/HBM levels of the 1.8 V and 3.3 V butting pickup case by 2.1~2.3 times and 18%~6 times, respectively, and the 1.8 V and 3.3 V inserted pickup case by 2.4~2.9 times and 13%~6 times, respectively. This simple technique could restore the ESD threshold level of the butting/inserted pickup layout style back to that of the normal GGNMOS without any further area consumption or fabrication cost.

1. Introduction

Since semiconductor technology advances continually, electrostatic discharge (ESD) issue has been a serious reliability problem for semiconductor components and systems. An NMOSFET has been the most popular ESD protection candidate long time ago. However, the ESD capability of the NMOS device encountered more challenges long time ago [1–3]. A gate-grounded NMOS (GGNMOS) can no longer fulfill the ESD protection mission easily. NMOS protection devices usually require their large width size to sustain ESD stress. This results in multifinger layout style commonly seen in practical IC I/O area. But it has a serious issue which is vulnerable to the ESD protection requirement. The conduction current is nonuniformly distributed along the width direction of the multifingers usually. Gate-coupling technique using the property that increases the gate bias can reduce the first trigger point of the NMOS device and enable uniform ESD current distribution [4–6]. However, it still has gate overdriven effect if the gate voltage coupled is much larger than its threshold voltage, and this leads to ESD degradation after all [7–9]. Substrate triggering and substrate-gate cotriggering techniques have also been developed to improve the gate driven weakness [8–12]. A simplest way to relieve the nonuniform current problem is to add substrate pickup diffusion inserted or butting into the source regions of the NMOS devices as in Figures 1(a) and 1(b). Unfortunately, substrate pickups butting or inserted in the source region still damage ESD reliability seriously beyond deep submicrometer technology. Such layout style has been strictly prohibited in practical ESD design applications by the technology design rules until now. This ESD degradation is mainly owing to the bypass and shortening of the effective substrate resistance by the butting/inserted action.

Therefore, a new split island substrate layout technique is proposed in this work to resolve the above problem.

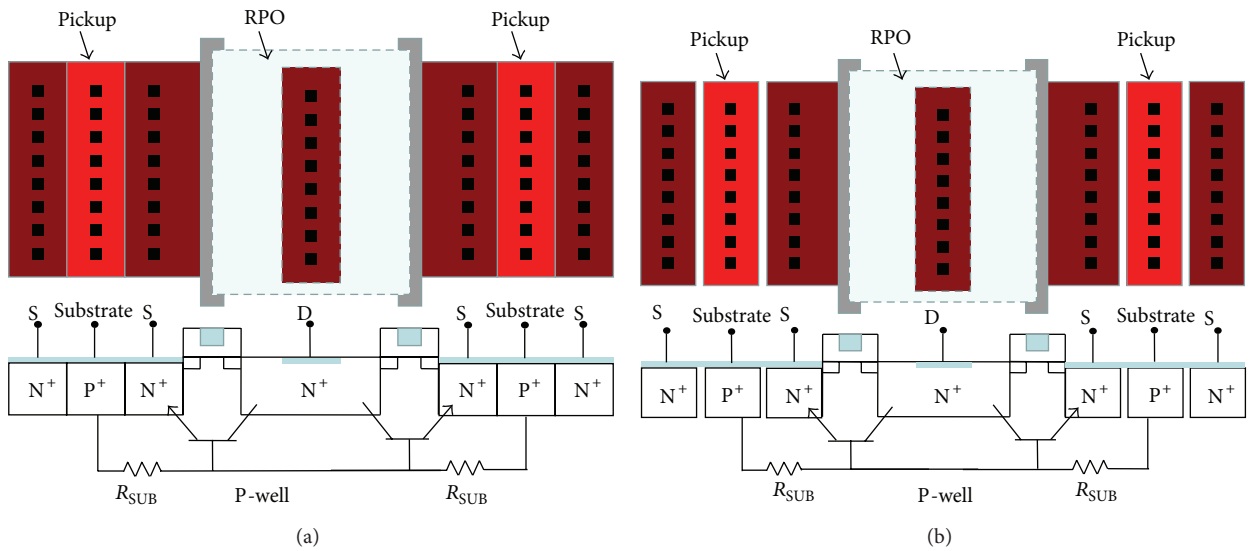

Figure 1: (a) The layout top and cross-sectional view of the multifinger ESD NMOS with butting substrate pickups. (b) The layout top and cross-sectional view of the multifinger ESD NMOS with inserted substrate pickups.

This simple layout technique divides the conventional substrate pickup bands into segmented diffusion islands in standard deep submicron CMOS technology. This layout style has been investigated and compared with the conventional butting/inserted pickup conditions as well as normal GGNMOS in detail. The split island layout with optimized dimension exhibits much better ESD performance and it can greatly improve the conventional pickup layout style. It requires neither further layout area consumption nor extra process cost.

2. Split Island Substrate Pickup Layout Scheme

Figures 1(a) and 1(b) show the top and cross-sectional view of an ESD NMOS device with conventional butting/inserted substrate pickup layout style in the source region. Both are also surrounded by their own outer P^+ pickup ring in general. The butting pickup diffusion regions are drawn in contact with the source diffusions and the inserted P^+ pickup regions are placed near the source diffusions with a minimum allowable spacing given by the technology rules. In the conventional multifinger NMOS device layout, the conduction current is usually unevenly distributed along the width direction of the multifingers. One possible cause of this problem is the nonuniform distribution of individual substrate resistance inherent in the real device layout. The butting/inserted pickup layout in Figures 1(a) and 1(b) provides a simple solution to the above problem. The layout style generates identical layout pattern and hence identical substrate resistance configuration for each individual polygate finger layout. Nevertheless, it still significantly degrades NMOS ESD performance beyond deep submicron technologies.

The proposed new layout technique divides the substrate pickup bands into split island style as illustrated in Figures 2(a)~2(d). Figures 2(a) and 2(b) show the split island layout of the butting and inserted substrate pickup condition for the multifinger NMOS device, respectively. The substrate pickup islands are spreading in the source diffusion and the number of these pickup islands is less in the peripheral part of the source blocks and more in the central part. The intention of the pickup island number modulation is to balance the intrinsic substrate resistance variation inherent in the multifinger layout. The intrinsic substrate resistance of the central part is higher than the peripheral part due to the outer pickup ring. More pickup island number in central part could possibly suppress the effective substrate resistance and less pickup number could raise the effective substrate resistance too. Such layout style is intended to lessen the variation of the intrinsic substrate resistance and promote, or at least not to further deteriorate, the current distribution in the multifinger layout. The substrate pickup islands occupy less area than the conventional pickup bands. This is expected to relieve the effective resistance bypassing and reduction of the effective substrate resistance.

In the experimental conditions, the typical diffusion size of the split island pickup is about 1.2 μm × 1.2 μm with one or two contacts in each pickup region. This size is slightly larger than the minimum allowable dimension by the technology rule. There are two pickup islands in the peripheral source region and 8 pickup islands in the second peripheral source region. There are 16 pickup islands in the central part. The length of P^+ split island pickup is varied as 1.2 μm, 2 μm, and 6 μm with full contacts to optimize the proper pickup size in Figures 2(c) and 2(d). The condition of larger split pickup islands also maintains the corresponding layout style in the peripheral and central parts as in Figures 2(a) and 2(b).

In addition, the spacing between P^+ pickup ring and the transistor main body is also varied from typical 4 μm to 40 μm and infinity, that is, no ring surrounding the main body. This variable is designed only in the 1.2 μm size condition to reveal the outer pickup ring effect on

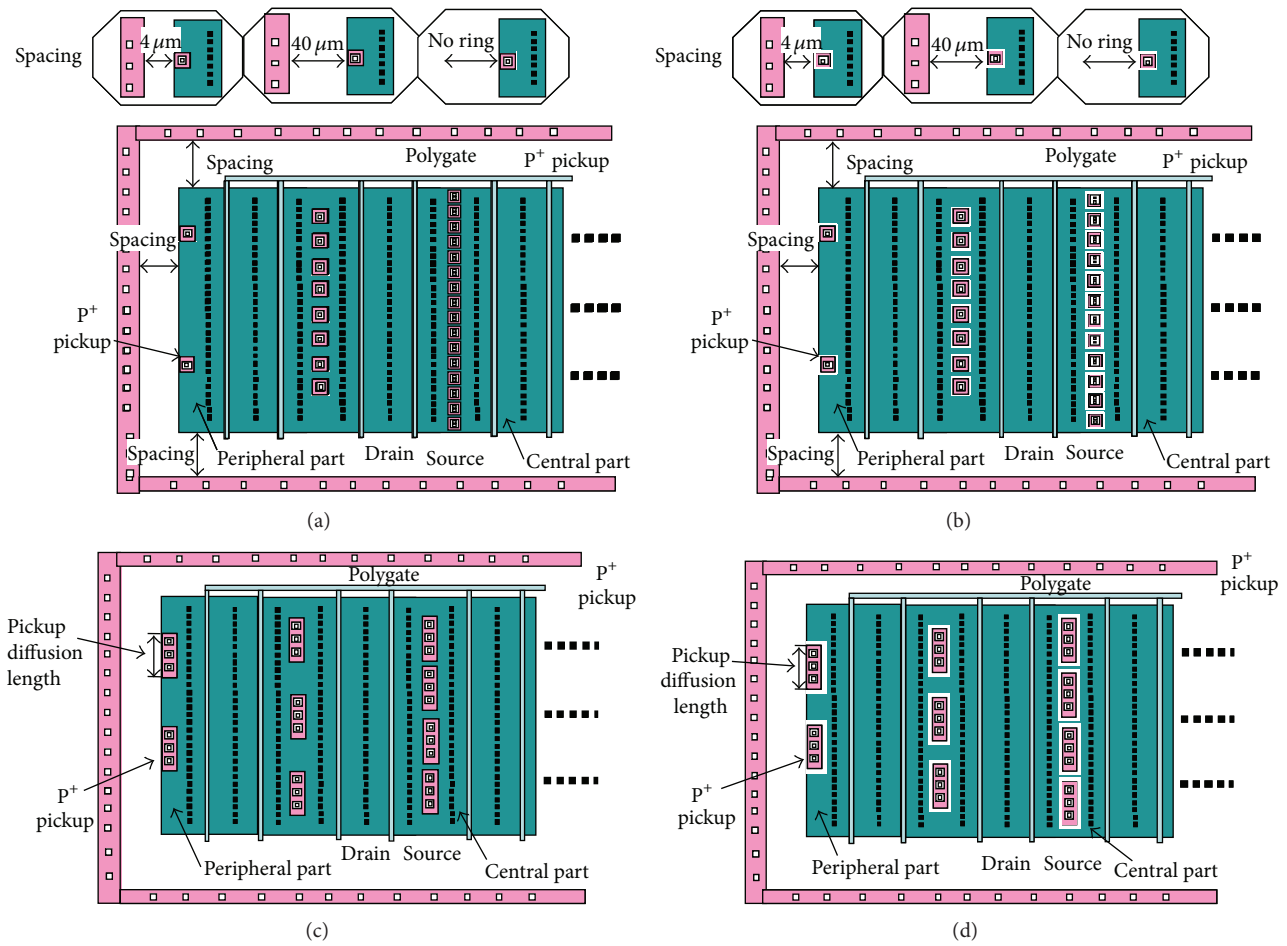

Figure 2: (a) The proposed split island layout of the butting substrate pickups for the multifinger NMOS devices. (b) The proposed split island layout of the inserted substrate pickups for the multifinger NMOS devices. (c) The proposed split island layout diagram of the butting substrate pickups with varied pickup length for the multifinger NMOS devices. (d) The proposed split island layout diagram of the inserted substrate pickups with varied pickup length for the multifinger NMOS devices.

the split island layout. The main parameters of the NMOS ESD protection devices are the channel width/length W/L = 360/0.18 μm with 10 polygate fingers of 36 μm long for 1.8 V power supply and W/L = 360/0.35 μm with 10 polygate fingers of 36 μm long for 3.3 V power supply. The drain contact-to-gate spacing of the transistors is 1.72 μm with silicide blocking mask. These structures were fabricated in standard 0.18 μm 1.8 V/3.3 V process technology. The whole device structures were stressed by STAR TLP (transmission line pulse) curve tracing machine. The TLP current pulse width is 100 ns with its rise time equal to 2.5 ns. The failure criterion is defined as the DC leakage current greater than 1 μA at maximum power supply voltages 2 V and 3.6 V after the TLP stress. The whole test devices were also measured by Human-Body-Model (HBM) ESD zapping for their ESD threshold evaluation.

3. Experimental Results and Discussion

Figures 3(a)~3(c) show TLP IV curve comparison among various 1.8 V/3.3 V butting/inserted pickup conditions and the normal GGNMOS. Because these plots contain many complex IV curves and are not easy to comprehend, their second breakdown current I_{t2} data were plotted again in Figures 4(a)~4(b) for detail inspection. In Figure 3(a), the notation "S40 μm" represents the 40 μm spacing between the outer pickup ring and the main transistor body. The notation "butt" represents the butting pickup condition. The notation "butt compare" represents the conventional butting pickup case as comparison. These notations are adopted just for display simplicity in the plot legend. The numbers, 1.2 μm, 2 μm, and 6 μm, represent P^+ pickup length conditions. The term "normal GGNMOS" is for the general grounded-gate NMOS case with only an outer pickup ring around it. I_{t2} is 3.04 A for the GGNMOS case and its IV curve clearly exhibits very severe nonuniform turn-on action. The 1.87 A I_{t2} value of the conventional butting case is much lower than that of the normal GGNMOS so that the butting pickup is regarded as a prohibited layout style. The 2 μm and 6 μm split island butting conditions have I_{t2} levels 3.1 A/2.95 A, and they demonstrate better ESD ability than the butting comparison case by 58~66% and are similar to the normal GGNMOS. However,

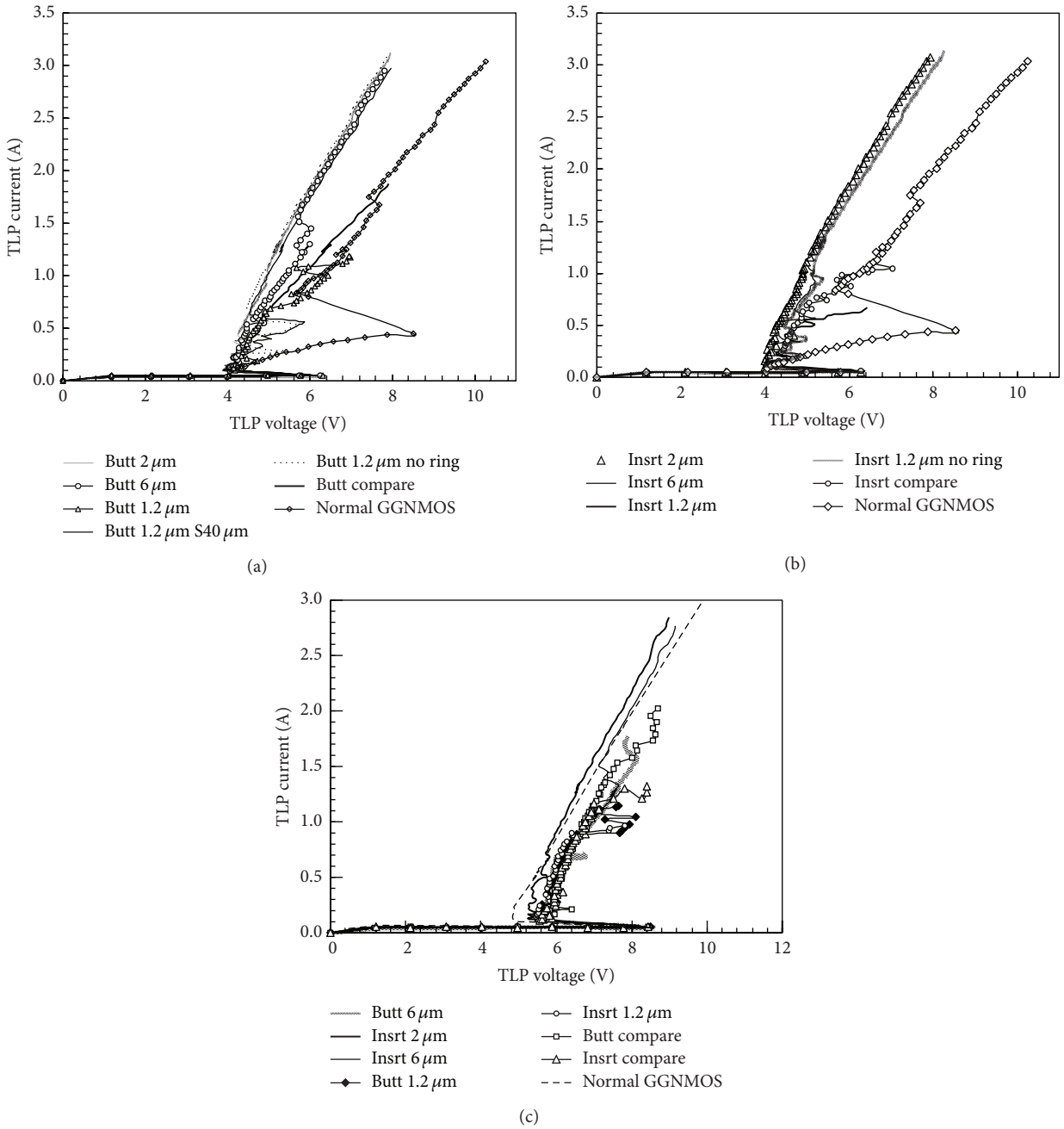

Figure 3: (a) TLP *I-V* curve comparison among the GGNMOS and various butting pickup conditions with 1.8 V power supply. (b) TLP *I-V* curve comparison among the GGNMOS and various inserted pickup conditions with 1.8 V power supply. (c) TLP *I-V* curve comparison among the normal GGNMOS and various butting/inserted pickup conditions with 3.3 V power supply.

the 1.2 μm butting case has the lowest I_{t2} level 1.19 A among all. All of them still reveal multiple snapback actions clearly but with a minor extent than the GGNMOS. Many of them also show voltage fluctuation during initial turn-on curve tracing. This implies somewhat more unstable turn-on behavior. The behavior might be related to the substrate resistance shunting property and hence difficult turn-on action. At last, most *IV* curves of the split island butting layout reveal steeper line slope apparently, which implies smaller on-resistance for the new layout style. The 1.8 V butting pickup case with its length over 2 μm could possess better I_{t2} capability than the butting comparison one. Furthermore, the special conditions of the outer pickup ring spacing 40 μm and no outer pickup ring also exhibit the same I_{t2} values 3.0 A as those of the GGNMOS and split island butting cases. So the split island layout with large ring spacing and without ring can perform ESD protection very well.

Next, Figure 3(b) shows TLP *IV* curve comparison among various 1.8V inserted pickup conditions and the normal GGNMOS, and their I_{t2} data were also plotted again

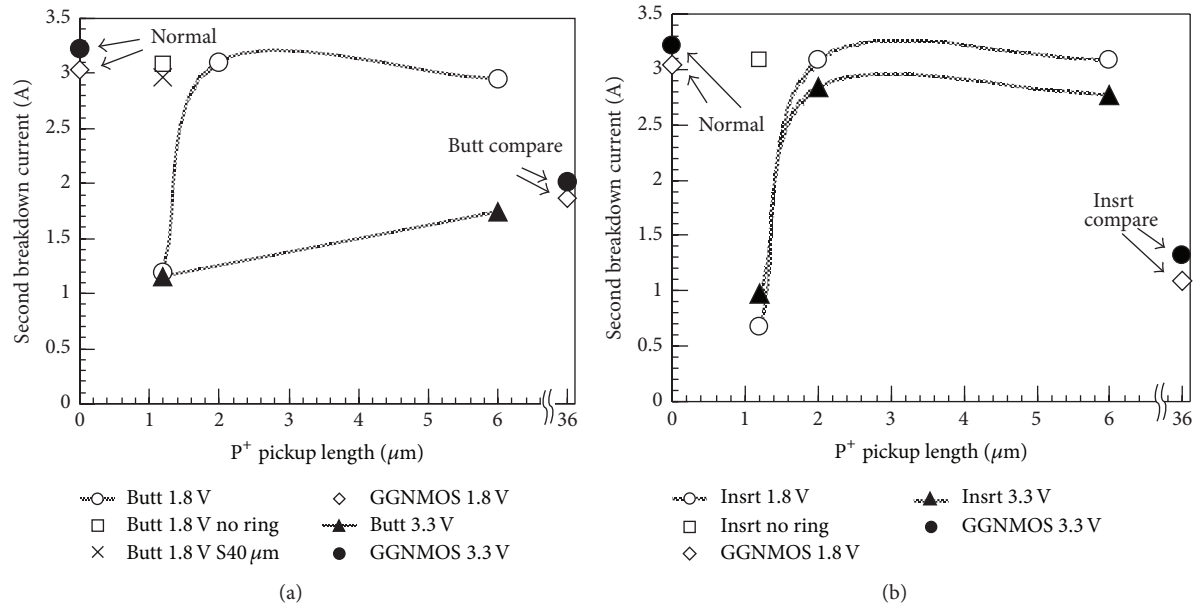

FIGURE 4: (a) TLP I_{t2} comparison among the GGNMOS and various butting substrate pickup styles with respect to the pickup length. (b) TLP I_{t2} comparison among the GGNMOS and various inserted substrate pickup styles with respect to the pickup length.

in Figure 4(b). The notation "insrt" represents the inserted pickup condition. This notation is adopted again just for display simplicity in the plot legend. I_{t2} value of the inserted comparison case is only 1.09 A. The 2 μm and 6 μm inserted pickup conditions demonstrate I_{t2} levels around 3.08 A, and they are far superior to the conventional inserted one by 2.8 times. Only the 1.2 μm inserted case shows 0.67 A I_{t2} that is worse than the inserted comparison one. Similar to the butting layout style, the inserted split island layout also reveals unstable voltage fluctuation during initial snapback action. This perhaps implies difficult turn-on due to substrate resistance shunting during initial snapback stage. It is also observed that most *IV* curves of the inserted split island cases exhibit steeper line slope and lower on-resistance as compared with the normal GGNMOS and inserted comparison one.

Finally, the various 3.3 V butting/inserted pickup conditions are compared in Figure 3(c) and their I_{t2} data replotted in Figures 4(a) and 4(b) for clear illustration. In the TLP figure, the 3.3 V GGNMOS demonstrates the best I_{t2} value 3.22 A among all. The butting comparison condition has I_{t2} value of 2.02 A and the inserted comparison one 1.32 A. Unfortunately, the 3.3 V butting conditions could only show poor 1.15~1.74 A I_{t2} ability. They are worse than 2.02 A I_{t2} of the 3.3 V butting comparison one. The split island layout seems not to provide improvement in this occasion. Similar to the 1.8 V results, the 3.3 V split island layout still reveals unstable initial snapback behavior, yet the tendency becomes minor. The normal GGNMOS *IV* curve demonstrates an ideal smooth shape. Higher holding voltage for the split island conditions is observed in Figure 3(c). The split island conditions also reveal slightly higher line slope and lower on-resistance compared with the normal GGNMOS one. In Figure 4(a), it is noted that the data of 3.3 V butting structure with 2 μm pickup size is not available until now because of some unknown technical error in this experiment. Thus the feasibility of 3.3 V split island layout style is not certain based on the present results. On the other hand, the 3.3 V inserted cases with 2 and 6 μm sizes both illustrate 2.77~2.84 A I_{t2}. This new layout could indicate excellent I_{t2} improvement over 1.32 A of the 3.3 V inserted comparison one by 2.1~2.2 times. As a whole, I_{t2} levels of the conventional butting/inserted comparison layout could only reach about 62%~63% and 34%~41% I_{t2} magnitude of the normal GGNMOS, respectively. As shown in Figures 4(a) and 4(b), most of the butting/inserted pickup size from 2 to 6 μm could overcome the conventional weakness and restore the electrical characteristics back to the normal status with the only exception of the unknown 3.3 V butting result. The 1.8 V split island butting cases enhance I_{t2} characteristics by 58~66% and 1.8 V/3.3 V split island inserted cases enhance I_{t2} characteristics by 2.8 times. The 1.2 μm size conditions with large pickup spacing and no outer ring could also provide the same grade of improvement.

The holding voltage V_H and on-resistance R_{on} characteristics are further illustrated in Figures 5(a) and 5(b) in detail. In Figure 5(a), V_H and R_{on} data with respect to P^+ pickup length are compared among various 1.8 V butting/inserted pickup styles. For V_H part, V_H data were extracted from the intercept on x- (voltage) axis from *IV* straight line extrapolation. V_H results are the same for most of the measured structures. The split island layout results in the same V_H as those of normal GGNMOS and butting/inserted comparison ones. The butting/inserted pickup structures do not change their V_H characteristics a lot. Only two 1.2 μm butting/inserted conditions exhibit higher V_H values. They are the weakest experimental conditions. Next for R_{on} part, the most split island conditions show lower R_{on} than

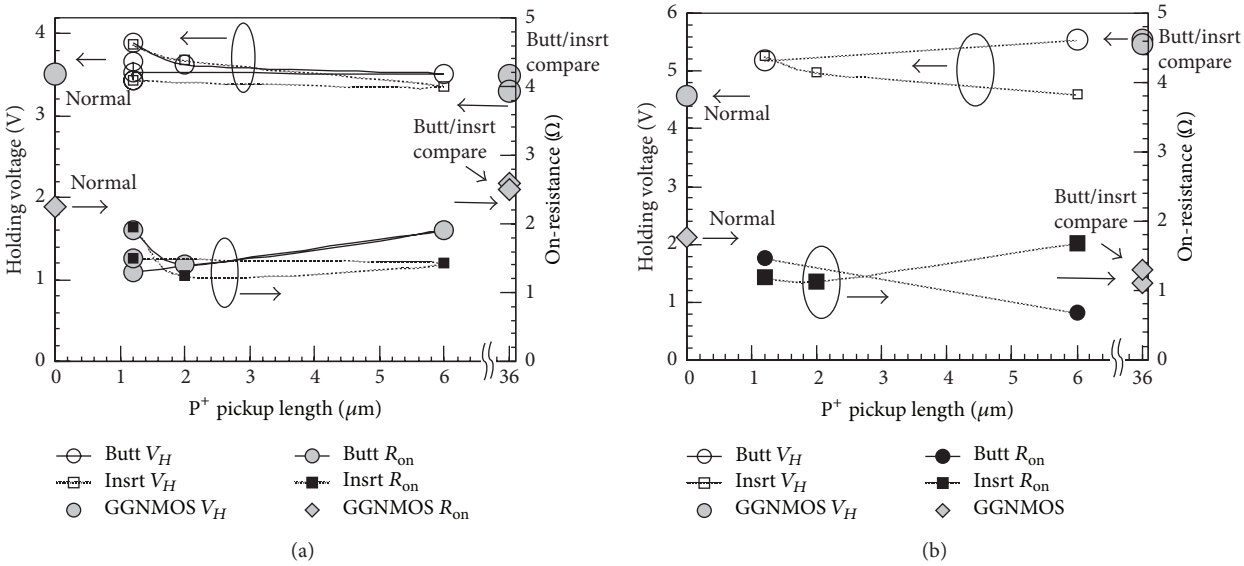

Figure 5: (a) The holding voltage and on-resistance comparison among the 1.8 V GGNMOS and various butting/inserted pickup styles with respect to the pickup length. (b) The holding voltage and on-resistance comparison among the 3.3 V GGNMOS and various butting/inserted pickup styles with respect to the pickup length.

the normal GGNMOS and butting/inserted comparison ones. The lower R_{on} result can also be observed apparently in Figures 3(a)~3(c). Once again, the abnormal higher R_{on} data belong to the two weak 1.2 μm cases in Figure 5(a). This apparently illustrates the invalidation of the small size split island layout in ESD performance.

Next the discussion turns to the 3.3 V results as shown in Figure 5(b). V_H levels of the all butting/inserted conditions are slightly higher than that of the normal GGNMOS and their R_{on}'s are slightly lower than the normal GGNMOS. V_H of the 3.3 V conditions is higher than that of the normal GGNMOS while the 1.8 V conditions are similar to the normal GGNMOS. The smaller R_{on} is another benefit of the butting/inserted layout style. On the whole, V_H and R_{on} show slightly contrary pickup length dependence. As V_H increases with the increase of P^+ pickup length, R_{on} decreases with respect to the pickup length. In contrast, R_{on} increases as V_H decreases with respect to P^+ pickup length.

Finally, the study focus turns to the ESD/HBM measurement results as shown in Figures 6(a) and 6(b). Figure 6(a) illustrates the ESD/HBM failure threshold with respect to P^+ pickup length for the normal GGNMOS and various butting conditions. For 1.8 V butting part, the average ESD threshold data remain almost the same with the increase of the pickup length and also similar to that of the normal GGNMOS. They are far superior to the butting comparison ones by 2.1~2.2 times. For the 3.3 V butting part, the average ESD values exhibit a pickup length dependence of hump shape with a maximum value around 2 μm. Unlike the 1.8 V result, their ESD ability cannot reach the normal GGNMOS but they are at least slightly higher than the comparison ones for either 1.2 μm or 6 μm length by 18%~94%. Nevertheless, the best ESD threshold is 6 times higher than the comparison one. It is also noted that the comparison data exhibits wide variation range from 1.2 kV to 4 kV.

Next, Figure 6(b) shows the ESD endurance with respect to P^+ pickup length for various inserted pickup conditions. The ESD threshold behaviors demonstrate similar trend as that of the butting conditions. The 1.8 V conditions show the same ESD robustness with the increase of the pickup length and are similar to the normal GGNMOS. They are much better than the comparison one by 2.4~2.6 times. The 3.3 V conditions demonstrate hump distribution once again. However, the short pickup 1.2 μm length now has higher average ESD threshold while the 6 μm length has only the same ESD threshold as that of the 3.3 V comparison ones. The 3.3 V maximum ESD threshold is greatly superior to the comparison one by 6.4 times. It is surprising that the 3.3 V 1.2 μm inserted case exhibits extremely large fluctuation of the ESD robustness from minimum 1.2 kV to maximum over 8 kV. This implies severe performance variation inherent in the 1.2 μm inserted pickup structure. The 1.8 V 1.2 μm inserted structure without pickup ring also shows large ESD fluctuation from 5.4 kV to over 8 kV. Furthermore, the 1.8 V inserted comparison data range from 0.6 kV to 4 kV. These results all imply the fluctuation weakness of the butting/inserted layout even with short P^+ pickup length.

The electrothermal device simulation was further performed to highlight the operation feature of the butting/inserted structure. Figures 7(a) and 7(b) compare the 2D total current distribution at the same drain current for the normal GGNMOS and the butting pickup structures, respectively. In the normal GGNMOS device, the substrate pickup region is defined at the left bottom corner and connected in series with a lumped 200 Ω resistance to resemble the real situation. The device was stressed by an arbitrarily selected drain current level close to the butting case I_{t2}. In this circumstance, most of the current vectors flow from the drain to the source with only few to the substrate pickup. The substrate current is 4.2 mA with the peak lattice temperature 880°K near the drain

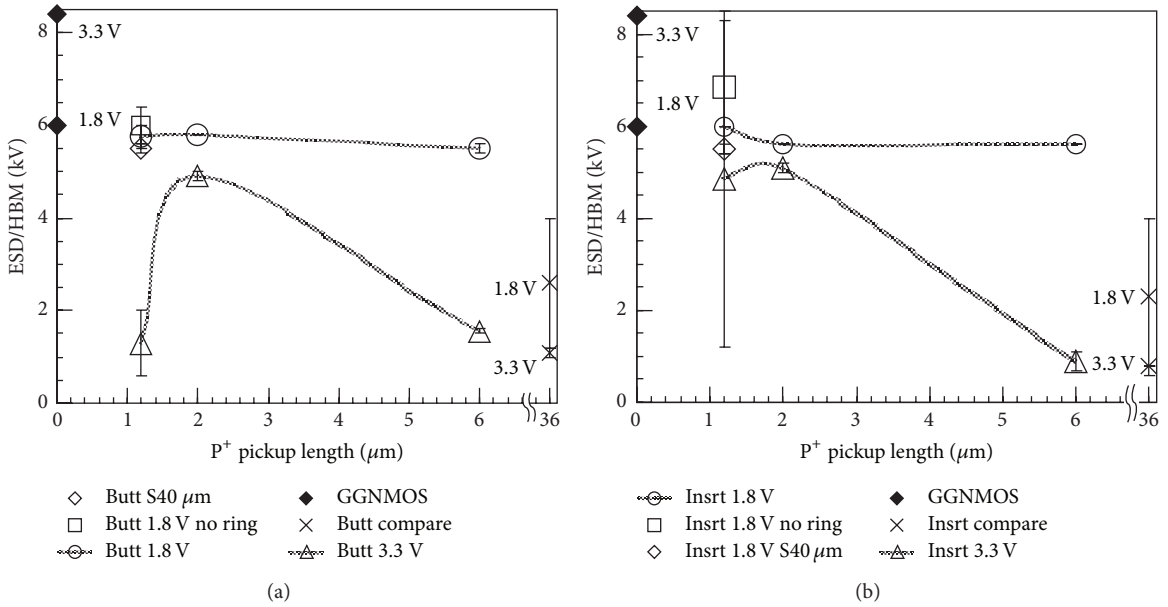

Figure 6: (a) The ESD/HBM failure threshold versus pickup length comparison among the normal GGNMOS and various butting pickup conditions. (b) The ESD/HBM failure threshold versus pickup length comparison among the normal GGNMOS and various inserted pickup conditions.

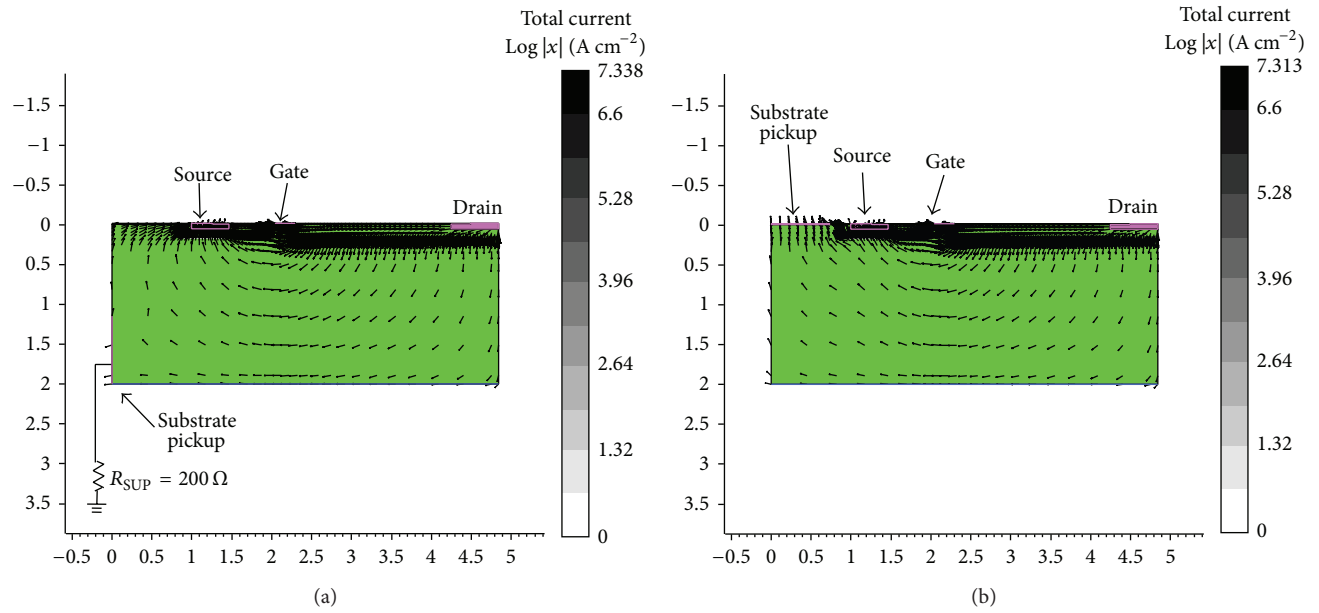

Figure 7: (a) The simulated 2D current distribution of the normal GGNMOS structure. Its substrate current is 4.22 mA with peak lattice temperature 880°K. (b) The simulated 2D current distribution of the butting structure. The substrate current of the butting structure is 325.9 mA with peak lattice temperature 1167°K. Similar simulated inserted structure has substrate current 298.1 mA with peak lattice temperature 1104°K.

gate edge. On the other hand, the butting structure was also stressed by the same drain current. Figure 7(b) demonstrates that more current vectors of the butting structure crowd beneath the substrate contact. Its substrate current now becomes 325.9 mA with its lattice temperature up to about 1167°K. Another similar structure with inserted pickup has a minimum spacing between P^+ pickup region and the source diffusion. This device was stressed by the same current once again.

The resulting substrate current becomes 298.1 mA with lattice temperature about 1104°K. From this analysis, it is clearly observed that the butting/inserted pickup diffusion region may lead to bypass or shunt effect of the normal substrate resistance, or equivalently, a much lower effective substrate resistance. A large portion of the drain current is directed to the substrate pickup by this bypass route so that the substrate current is much larger than that of the normal device by 100 times. This will not create sufficient

emitter-base voltage drop for effective turn-on of the parasitic bipolar transistor. In contrast, the substrate current of the normal one is quite small but it is enough to create the emitter-base turn-on voltage 0.7 V. Thus, the parasitic BJT under the butting/inserted device cannot turn on effectively to conduct most stress current. The lattice temperature is then much higher than that of the normal one. The butting pickup condition bypasses the current more completely, so its substrate current is the largest and lattice temperature is the highest among all. The simulation is based on the simplified 2-dimensional circumstance; although it may not be very exact or accurate, it still reveals the key feature of the butting/inserted pickup layout situation.

Furthermore, I_{t2} and ESD characteristics roughly exhibit pickup length dependence of a hump shape especially for the 3.3 V power. There is a missing of 2 μm 3.3 V butting condition in Figure 4(a) but the same trend as other curves is still expected. As the pickup length becomes smaller, the substrate current will localize in relatively small scale of peripheral length when compared with the total channel width as indicated by the simulation. The nonuniform crowding current results in early failure around these small pickup areas. On the other hand, as the pickup length becomes longer, the bypass state of the butting/inserted layout approaches that of the conventional butting/inserted one. Hence the ESD performance of the split island layout is restored back to the conventional comparison one. After trade-off between the above two factors, the ESD/I_{t2} curves illustrate maximum levels in the central range of P^+ pickup length. In addition, Figures 5(a) and 5(b) also reveal another minor tendency. When V_H rises according to the pickup length, the corresponding R_{on} falls. On the contrary, the corresponding R_{on} increases as V_H decreases with respect to the pickup length. In this study, R_{on} property comes from the butting/inserted pickup variation, or equivalently substrate resistance. R_{on} varies according to the change of substrate resistance. Smaller substrate resistance might require higher applied voltage outside, that is, V_H, to reach the same turn-on/emitter-base voltage drop 0.7 V of the parasitic bipolar action under the MOSFET.

The other benefit of the split island layout technique reflects the uniform current distribution phenomenon. The dedicated layout modulation of the pickup island number has shown its effect on this benefit as observed in Figures 3(a)~3(c) and 5(a)~5(b). The split island conditions exhibit steeper *IV* curve slopes and smaller R_{on}. The more uniform the ESD current is distributed along the channel width, the wider the effective channel width becomes and hence the smaller R_{on} would be observed. However, the simple split island layout is still not powerful enough as the substrate-gate-triggering NMOS (SGTNMOS) technique [12] which could create up to about 30% improvement. The large ring spacing and no ring conditions in 1.8 V power supply also reveal better I_{t2} and ESD characteristics. The no ring structure removes the central/peripheral dependence of the parasitic substrate resistance, so nonuniform current distribution is eliminated considerably. For the butting/inserted 1.2 μm cases with the outer guard ring around them, nonuniform current distribution plus small size island pickup layout produces poor ESD performance of the 1.2 μm conditions similar to the butting/inserted comparison ones.

At this point, the butting/inserted layout optimization should be evaluated by TLP I_{t2} and ESD characteristics together in comprehensive manner. Although the pickup length dependence of the TLP I_{t2} seems to share a similar tendency as the ESD characteristics, I_{t2} data still have some discrepancies from the ESD measurement ones. The 1.8 V 1.2 μm length condition reveals very low I_{t2} current while it has quite well ESD threshold. This discrepancy may be attributed to the wide fluctuation nature of the butting/inserted layout style. This can be clearly observed by the 1.8 V butting comparison case in Figure 6(a), the 1.8 V inserted comparison case, and the 3.3 V 1.2 μm inserted cases in Figure 6(b). In contrast, other split island conditions show quite small ESD threshold variation. The ESD performance variation should be a serious concern as high priority in practical applications. More importantly, ESD/HBM measurements should be the final judgment means for ESD reliability evaluation. From this point of view, the optimized pickup length should range from 2 μm to 6 μm for 1.8 V butting/inserted layout and around 2 μm or a little bit larger than 2 μm for 3.3 V power supply. Design of the 1.8 V power supply possesses a wider layout window than that of 3.3V. Either the large ring spacing or no ring condition is not practical for real applications although both could perform well. Because of no further split conditions between 2 μm and 6 μm, no further decision could be made at present time about the appropriate upper limit of the pickup length. It would require additional experiments in the future. Therefore, based on the above experimental and analysis results, the optimized split island layout of the butting/inserted pickups could provide a simple solution for ESD performance enhancement without any layout area consumption or manufacturing cost.

4. Conclusions

A split island layout technique for butting/inserted substrate pickups has been developed to improve ESD degradation problem of multifinger ESD NMOS transistors. This new layout style has been tested and verified by both TLP and ESD/HBM measurement to prove its effectiveness. The optimized split island layout structure could improve the TLP second breakdown current of the 1.8/3.3 V butting/inserted pickups by 58%~2.8 times. At the same time, this technique could enhance the corresponding ESD/HBM robustness by 13%~6 times. The split island layout style provides a simple method of ESD robustness improvement without any additional layout area or fabrication cost.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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References

[1] A. Amerasekera and C. Duvvury, "The impact of technology scaling on ESD robustness and protection circuit design," in *Proceedings of the EOS/ESD Symposium*, pp. 237–245, 1993.

[2] D. L. Lin, "ESD sensitivity and VLSI technology trends: thermal breakdown," in *Proceedings of the 15th EOS/ESD Symposium*, pp. 73–81, 1993.

[3] C. Duvvury, R. A. McPhee, D. A. Baglee, and R. N. Rountree, "ESD protection reliability in one micron CMOS technologies," in *Proceedings of the 24th Annual Proceedings Reliability Physics (IRPS '86)*, pp. 199–205, 1986.

[4] C. Duvvury and C. Diaz, "Dynamic gate coupling of NMOS for efficient output ESD protection," in *Proceedings of the 30th Annual International Reliability Physics Symposium*, pp. 141–150, San Diego, Calif, USA, April 1992.

[5] K.-H. Oh, C. Duvvury, K. Banerjee, and R. W. Dutton, "Analysis of nonuniform ESD current distribution in deep submicron NMOS transistors," *IEEE Transactions on Electron Devices*, vol. 49, no. 12, pp. 2171–2182, 2002.

[6] T. L. Polgreen and A. Chatterjee, "Improving the ESD failure threshold of silicided n-MOS output transistors by ensuring uniform current flow," *IEEE Transactions on Electron Devices*, vol. 39, no. 2, pp. 379–388, 1992.

[7] J. Z. Chen, E. A. Amerasekera, and C. Duvvury, "Design methodology and optimization of gate-driven NMOS ESD protection circuits in submicron CMOS processes," *IEEE Transactions on Electron Devices*, vol. 45, no. 12, pp. 2448–2456, 1998.

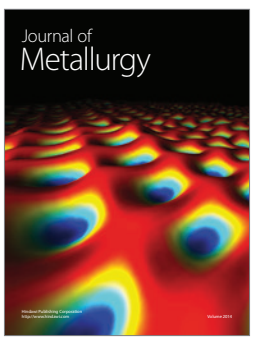
[8] T. Y. Yang and M. D. Ker, "Investigation of the gate-driven effect and substrate-triggered effect on ESD robustness of CMOS devices," *IEEE Transactions on Device and Materials Reliability*, vol. 1, no. 4, pp. 190–203, 2002.

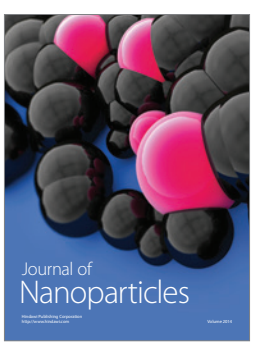
[9] K. H. Oh, C. Duvvury, K. Banerjee, and R. W. Dutton, "Gate bias induced heating effect and implications for the design of deep submicron ESD protection," in *Proceedings of the International Electron Devices Meeting (IEDM '01). Technical Digest*, pp. 951–954, 2001.

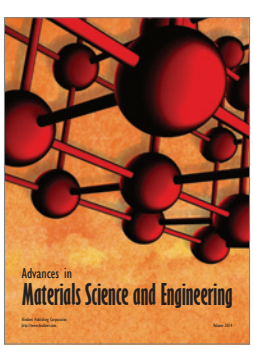
[10] A. Amerasekera, C. Duvvury, V. Reddy, and M. Rodder, "Substrate triggering and salicide effects on ESD performance and protection circuit design in deep submicron CMOS processes," in *Proceedings of the International Electron Devices Meeting (IEDM '95)*, pp. 547–550, December 1995.

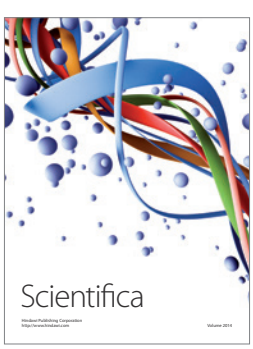
[11] M.-D. Ker, T.-Y. Chen, and C.-Y. Wu, "Design of cost-efficient ESD clamp circuits for the power rails of CMOS ASIC's with the substrate-triggering technique," in *Proceedings of the 10th Annual IEEE International ASIC Conference and Exhibit*, pp. 287–290, September 1997.

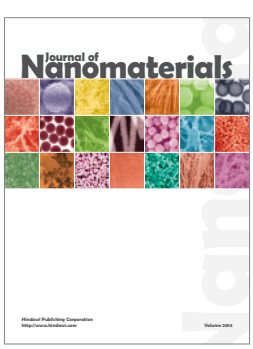
[12] C.-Y. Huang and F.-C. Chiu, "A substrate-and-gate triggering NMOS device for high ESD reliability in deep submicrometer technology," *Advances in Materials Science and Engineering*, vol. 2013, Article ID 905686, 7 pages, 2013.

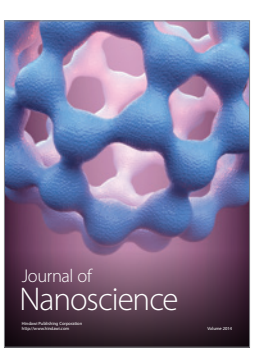


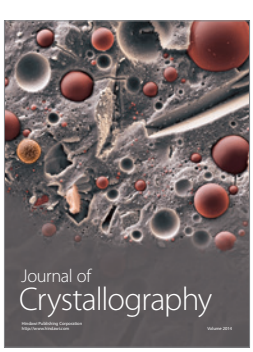


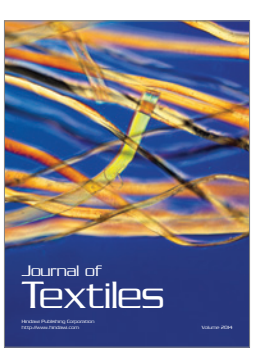












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