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Research Article

Main Parameters Characterization of Bulk CMOS Cross-Like Hall Structures

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A detailed analysis of the cross-like Hall cells integrated in regular bulk CMOS technological process is performed. To this purpose their main parameters have been evaluated. A three-dimensional physical model was employed in order to evaluate the structures. On this occasion, numerical information on the input resistance, Hall voltage, conduction current, and electrical potential distribution has been obtained. Experimental results for the absolute sensitivity, offset, and offset temperature drift have also been provided. A quadratic behavior of the residual offset with the temperature was obtained and the temperature points leading to the minimum offset for the three Hall cells were identified.

1. Introduction

The Hall effect sensors have been used for a long time to detect the magnetic field, to measure the currents, in DC motors, and to serve different low-power applications in the industry [1, 2]. Their low cost integration and robustness make them ideal candidates for these applications. Nowadays, they have been largely optimized (from performance and cost-effectiveness perspectives) and are employed on a large scale. Both regular bulk [3] and Silicon on Insulator (SOI) [4, 5] CMOS technologies Hall sensors have been produced.

As presented by the author recently in various papers, the optimal choice of the device geometry and dimensions is crucial in the establishment of a high performance sensor [3, 5]. These sensors are affected by offset. An extensive study of the Hall cells offset is made by the author in [6].

The offset voltage is an unavoidable parasitic voltage that adds to the Hall voltage. The fabrication process of Hall effect sensors could result in nonzero offset, with values exceeding the accepted limit for specific applications.

If the voltage offset is not correctly assessed and minimized, it could impede the precision with which we can determine the Hall voltage. The most important generating causes for the offset are the imperfections in the fabrication process of the Hall device, such as any misalignment of the contacts or nonuniformity in material resistivity and thickness. The offset could be also produced by a combination of mechanical stress and piezoresistance effect [2]. In order to minimize the offset different techniques are used such as, one of the most used techniques nowadays, the connection-commutation or spinning-current technique [2].

Other works looked into different aspects of offset of Hall cells [6–10]. However, it is in the Ph.D. thesis of the author in 2013 that has served the purpose of an exhaustive analysis of the Hall cells offset and the proposal of various models to assess it.

The present paper is organized in five sections. Section 2 summarizes the basic definitions for Hall cells, while Section 3 focuses on the three-dimensional physical simulation methodology. In Section 4, the Hall cells model and their geometrical parameters of the studied devices, experimental results regarding their main parameters such as the input resistance, absolute sensitivity, and offset temperature drift are also provided at this point. The results are included and discussed in Section 5, with more experimental results regarding the single-phase and four-phase residual offset.

A discussion of the temperature points for minimum offset is offered. The paper concludes and presents the future perspectives in Section 6.

2. Definitions

This section summarizes the basic definitions for Hall devices behavior. A Hall effect device is characterized by the Hall voltage V_{HALL}, given as follows:

$$V_{\text{HALL}} = \frac{Gr_H}{nqt} I_{\text{bias}} B, \tag{1}$$

where G is the geometrical correction factor, r_H is the Hall scattering factor, I_{bias} is the biasing current, n is the carrier density, q is the elementary charge, t is the thickness of the active region, and B is the magnetic field induction [2]. In the case of silicon, r_H is usually 1.15.

The sensitivity is one of the most important figures of merit related to a sensor. In general, the sensitivity is defined as the change in output resulting from a given change in input. Firstly, according to [2], the absolute sensitivity of a Hall magnetic sensor is given by the equation below:

$$S_A = \left| \frac{V_{\text{HALL}}}{B} \right| = \frac{Gr_H}{nqt} I_{\text{bias}}. \tag{2}$$

It is worth noting that, for Hall cells fabricated in the same process, the geometrical correction factor G (a number between 0 and 1) improves the absolute sensitivity [4]. At this moment, we can also note that, in order to increase the sensitivity of a Hall sensor, either a lower doping concentration n in the active region should or a smaller depth t of the active profile be used.

3. On the Three-Dimensional Physical Simulations

In the optimization stages of the CMOS Hall devices, different geometries have been designed and integrated in both regular bulk and SOI technological processes. Three-dimensional physical simulations of magnetic field influence on the semiconductors were previously performed by the author in [5], in order to assess the device performance.

3.1. Carrier Transport in Semiconductors. Assuming low injection, the classical carrier transport model for an n-type semiconductor [11] is based on the continuity equations:

$$\begin{aligned} \text{div}\vec{J}_n &= q\left\{\frac{1}{\tau_p}(p - p_0) + \frac{\partial n}{\partial t} - \left(\frac{\partial n}{\partial t}\right)_{\text{gen}}\right\}, \\ \text{div}\vec{J}_p &= -q\left\{\frac{1}{\tau_p}(p - p_0) + \frac{\partial p}{\partial t} - \left(\frac{\partial p}{\partial t}\right)_{\text{gen}}\right\}, \end{aligned} \tag{3}$$

where q is the elementary electronic charge, $\vec{J}_n$ is the electron current density, $\vec{J}_p$ is the hole current density, and n, p represent particle densities for electrons and holes, respectively. In the above equations, $(\partial n/\partial t)_{\text{gen}}$ represents the generation rate of particle densities due to incident light. Logically, $\vec{J} = \vec{J}_n + \vec{J}_p$ is the total current density. We mention here that for the case of p-type layer, in the equations above, the term $(1/\tau_p)(p - p_0)$ passes into $(1/\tau_n)(n - n_0)$, while τ_p is the hole relaxation time and τ_n is the electron relaxation time.

In physics, the differential equations (4) describe the conservation of electric charge.

The particle densities expressions in terms of Fermi energy level $E_{F,n}$ and $E_{F,p}$ are as presented in the following relations:

$$\begin{aligned} n &= n_i \exp\left\{\frac{qV - E_{F,n}}{kT}\right\} \\ p &= n_i \exp\left\{\frac{E_{F,p} - qV}{kT}\right\}, \end{aligned} \tag{4}$$

where V denotes the electrostatic potential, n_i is the intrinsic carrier concentration, T is the absolute temperature, and k is the Boltzmann constant.

For a complete description of semiconductor physical behavior, we also have to take into account the following equations:

$$\text{div}\left(\vec{D}\right) = \rho - \rho_{\text{trap}} \tag{5}$$

$$\vec{E} = -\text{grad}V. \tag{6}$$

Regarding the penultimate equation, ρ is the space charge and ρ_{trap} is the charge density contributed by traps and fixed charges. In the common acceptation, the electric field induction $\vec{D} = \varepsilon\vec{E}$, where $\vec{E}$ is the electric field and ε is the electric permittivity of the material. In the last equation V represents the electrostatic potential.

Replacing (6) in (5) and for a space charge ρ specified as $\rho = q(p - n + N)$ with $N = N_D - N_A$ denoting the fully ionized net impurity distribution, we get a partial differential equation of elliptic type:

$$\Delta V = -\frac{1}{\varepsilon}\left[q\left(p - n + N_D - N_A\right) + \rho_{\text{trap}}\right], \tag{7}$$

where N_D is the concentration of ionized donors and N_A is the ionized acceptors concentration. Finally we can say that the electrostatic potential V is the solution of the Poisson equation in (7).

Using the Synopsys Sentaurus TCAD software [12] that is able to solve the Poisson equation, both electrons and holes continuity equations, three-dimensional physical simulations of Hall cells were performed.

4. Hall Cells Model

This part includes the models developed for Hall cells behavior analysis, including offset modeling. Before entering the modeling approach, a few numerical values obtained through experimental measurements, for the main parameters of the integrated Hall cells in discussion, are presented.

Table 1: Hall cells dimensions.

Geometry	Basic	L	XL
n-well length L (μm)	21.6	32.4	43.2
n-well width W (μm)	9.5	14.25	19
Contacts length s (μm)	8.8	13.55	18.3

Table 2: Hall cells main parameters.

Geometry	Basic	L	XL
R_{input} (kΩ), for $T = 300$ K, $B = 0$ T	2.3	2.3	2.3
S_A (V/T), for $I_{\text{bias}} = 0.5$ mA	0.041	0.041	0.041
Offset drift (μT/$^\circ$C)	0.409	0.264	0.039

More than dozen different Hall devices have been integrated in a 0.35 μm XFAB CMOS technology. The present work is intended to emphasize a study on three Hall structures (basic, L, and XL). In Table 1 one could find the details on the considered cross-like Hall cells dimensions. The basic Hall cells are chosen as reference, while L and XL are scaled up dimensions of the first one.

To characterize the behavior of the Hall cells in discussion, they have been measured for Hall voltage, sensitivity, offset, and so forth. Table 2 presents the input resistance, absolute sensitivity, and offset drift for the basic, L, and XL Hall cells.

With respect to the measurements in Table 2, we mention that it is expected for the three Greek-cross Hall cells to have the same input resistance and absolute sensitivity, because all these are directly proportional to the length-to-width ratio, which is obviously the same for the three cells considered. However, the big difference and what produces the most important result in terms of the offset is the fact that XL Hall cells have a much lesser offset that the others. The offset drift for each cell is an average on more than dozen cells of the same type.

4.1. Three-Dimensional Physical Model of Cross-Like Hall Cells. These Hall cells have been subsequently analyzed using three-dimensional physical models, to numerically assess the values of their main parameters. Using TCAD Synopsys from Sentaurus tool [12], which solves the Poisson equation, both electrons and holes continuity equations, three-dimensional physical models of the Hall structures have been developed.

Figure 1 depicts the basic Hall cell meshed structure, with the information on the donor concentration. The CMOS Hall cells are basically orthogonal structures which use an n-well active region (red zone) in a p-substrate (blue zone), with four electrodes (pink zones). Similar models have been developed for the L and XL Hall cells.

4.2. Hall Cells Conduction Current Investigation. The investigation into the conduction current density is important in building the whole picture of a functioning Hall device.

In Figure 2, one could see the conduction current density meshed structure, depicted for the basic Hall cell. Figure 3 presents, for the simulated basic Hall cell, the conduction current between the a and c contacts. In order to illustrate this, an Ox cut has been made between the two contacts.

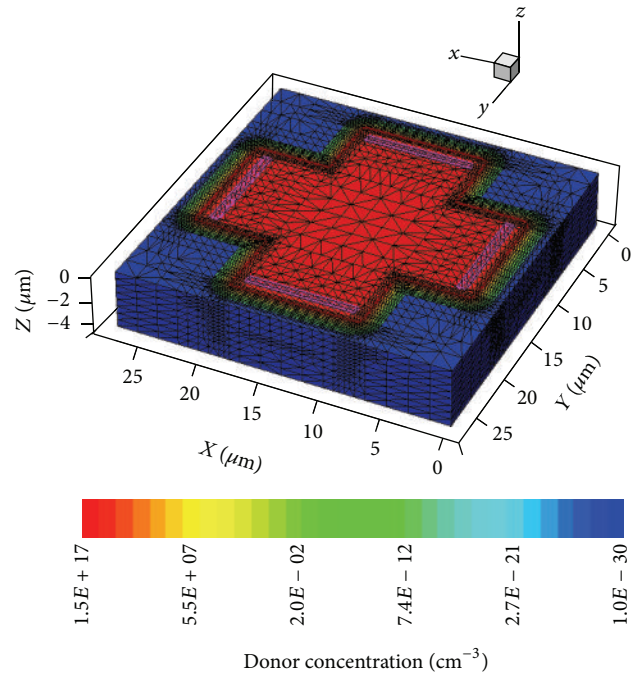


Figure 1: The meshed structure of basic Hall cell, with donor concentration.

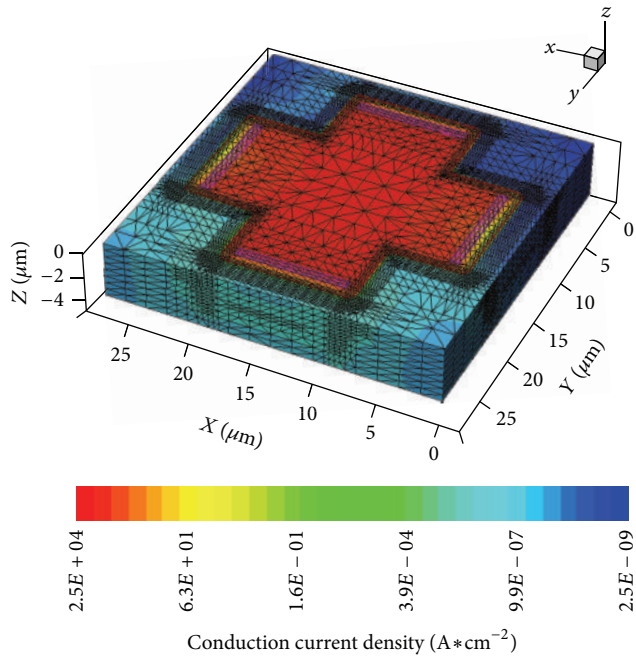


Figure 2: Conduction current density for basic cell.

4.3. Electrostatic Potential of the Cross-Like Hall Cells. Figures 4–6 present the electrostatic potential distribution of the basic, L, and XL Hall cells, where the biasing has been made

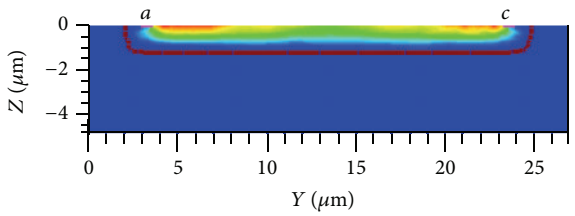


FIGURE 3: Conduction current density for basic cell with emphasis on the bias contacts *a* and *c*.

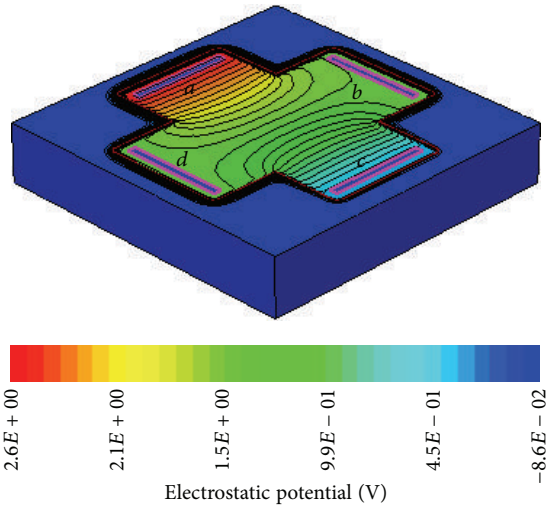


FIGURE 4: The electrostatic potential of basic Hall cell.

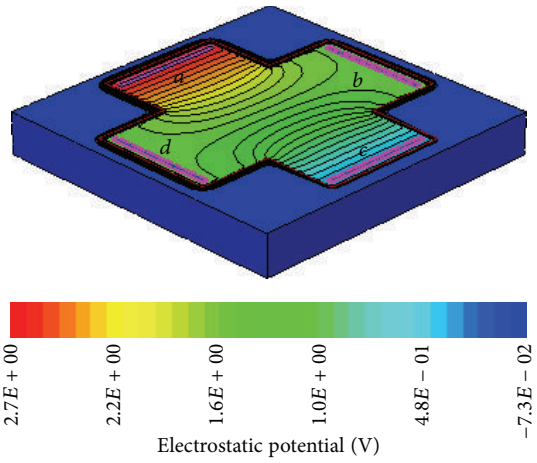


FIGURE 5: The electrostatic potential of L Hall cell.

on the *a* contact ("red zone"). A $V_{bias} = 1$ V was considered in this case.

In the simulations (see Figures 4–6), in order to obtain the electrostatic potential, a magnetic field induction $B = 0.5$ T was considered. We can see that under the influence of the magnetic field, the carriers are deviated under the Lorentz force and a nonzero voltage appears between the opposite contacts, giving birth to the Hall voltage.

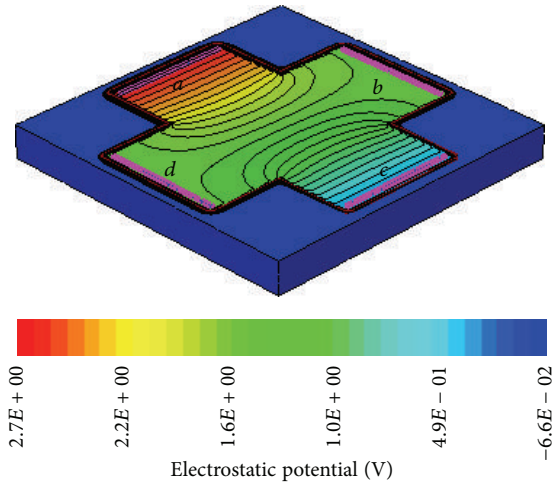


FIGURE 6: The electrostatic potential of XL Hall cell.

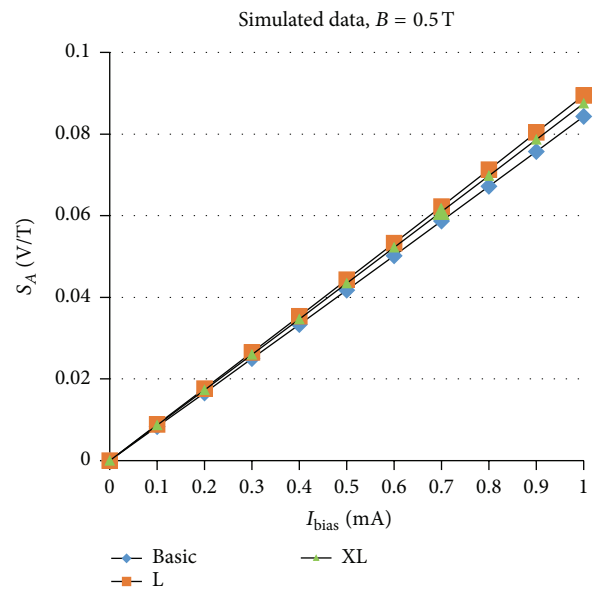
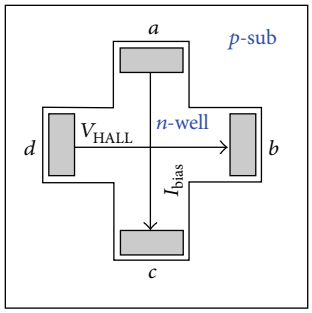


FIGURE 7: Simulated absolute sensitivity versus biasing current, for basic, L, and XL Hall cells.

4.4. Hall Cells Absolute Sensitivity. The absolute sensitivity is one of the most important performance parameters of the Hall cells. Simulations have been performed on the three Hall cells and their absolute sensitivity was numerically evaluated. The absolute sensitivity in Figure 7 was obtained for a magnetic field induction of $B = 0.5$ T. We can see that the simulation results are in accordance to the measured data from Table 2.

5. Results and Discussion

In the Hall cells offset analysis, new approaches (including 3D models and nonhomogeneous circuit models with new elementary cells) have been developed by the author during her Ph.D. work and presented in various papers [13]. This section includes experimental results for Hall cells offset.



Phases	I_{bias}	V_{HALL}
Phase 1	a to c	b to d
Phase 2	d to b	a to c
Phase 3	c to a	d to b
Phase 4	b to d	c to a

Figure 8: Greek-cross Hall cells polarization scheme and different phases.

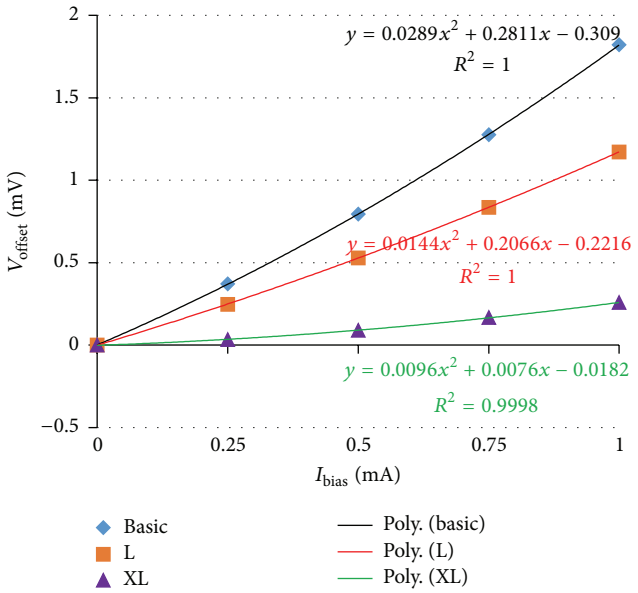


Figure 9: Measured single-phase offset versus biasing current for the integrated cross-like Hall cells.

5.1. Hall Cells Offset Measurements. The offset is a parasitic effect that adds to the Hall voltage, through the relation

$$V_{output} = V_{HALL}(B) + V_{offset}. \quad (8)$$

There are different sources of offset, for the Hall cells. Offset voltage can be generated by imperfections in the fabrication process, misalignment of contacts, nonuniformity of material resistivity and thickness, and mechanical stress in combination with the piezoresistance effect [2]. This paper focuses on the analysis of the Hall cells misalignment (asymmetry) offset, for cross-like Hall structures.

Previous measurements performed on the Hall devices for offset evaluation released information about how this quantity changes with the shape. In order to obtain the offset, a polarization of the type in Figure 8 is used. When there is no magnetic field ($B = 0$), an offset voltage (nonzero) appears instead of the Hall voltage.

Numerical values of the offset, for the three cross-like integrated Hall cells considered, are displayed in Figure 9, with respect to the biasing current. These measured offset

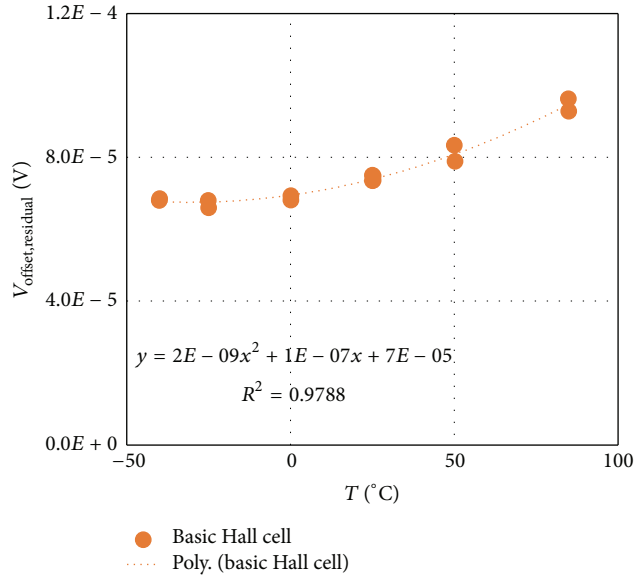


Figure 10: Measured residual offset versus temperature for the basic Hall cell.

curves with the biasing current have been fitted with second-order polynomials. We also mention that this is the measured single-phase offset, so it is before averaging it on several phases.

As it has been extensively analyzed by the author in her Ph.D. thesis, the offset decreases with the scaling of the Greek structure. Therefore, we can observe that the XL cell has the lowest single-phase offset, with an ordering of the decreasing offset values with the scaling of the dimensions, respectively, basic, L, and XL Hall cells.

5.2. Hall Cells Offset Temperature Drift Measurements. This section presents the measurements regarding the residual offset temperature variation, for the three Hall cells.

The residual offset measured at this point is the average of the four phases:

$$V_{offset,residual} = \frac{1}{4}\sum_{i=1}^{4}(-1)^{i+1}V_i, \quad (9)$$

where V_i is the individual offset of each phase, measured in V.

The residual offset is therefore obtained as a result of 4-phase averaging. The four phases of a Hall device polarization are shown in Figure 8. They will be employed in the spinning-current technique to reduce the Hall cells offset.

Figures 10–12 present the experimental results of the residual four-phase offset temperature variation, for the three considered Hall cells. Around dozen of different Hall samples have been tested. A temperature interval from −40 to 85°C was considered and several temperatures cycles (heating and cooling) have been performed. This is why in Figures 10–12 several temperature points appear twice. However, where the measurements for the same temperature point are the same, the results overlap.

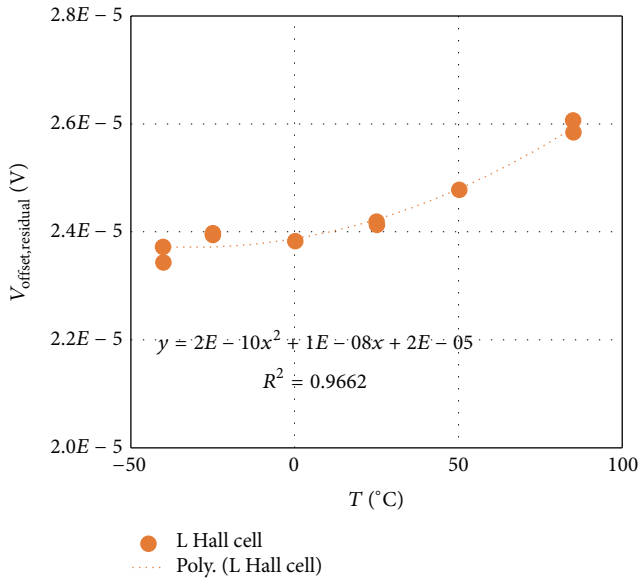


Figure 11: Measured residual offset versus temperature for the L Hall cell.

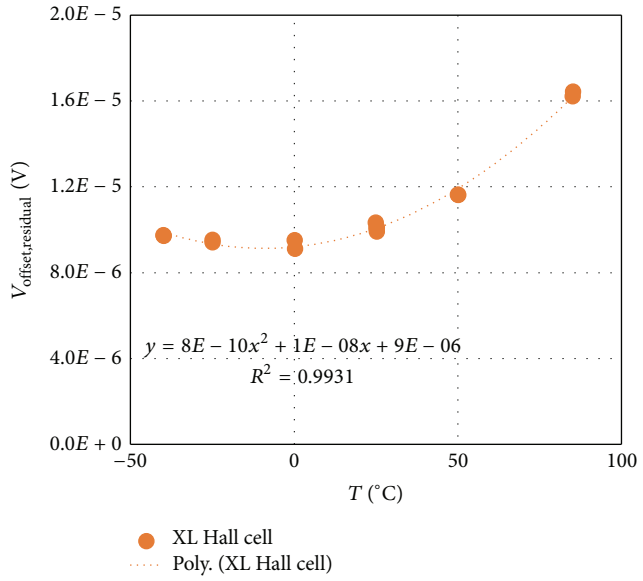


Figure 12: Measured residual offset versus temperature for the XL Hall cell.

By looking at the experimental results in Figures 10–12, we can observe the fact that the XL cells exhibit the lowest offset values for the considered temperature interval.

Also, we have fitted the experimental results of the residual voltage temperature dependence, for the three cross-like Hall cells considered for analysis, with second-order parabolic functions, of the form

$$f(x) = ax^2 + bx + c \quad (*). \tag{*}$$

The correlation coefficient, R^2, expresses how well the fitting equation describes the data. The closer R^2 is to 1, the better the fit.

Table 3: Fitting parameters.

Geometry	a (V^2/°C^2)	b (V/°C)	c (V)	R^2
Basic	$2E-9$	$1E-7$	$6.95E-5$	0.9788
L	$2E-10$	$1E-8$	$2.39E-5$	0.9662
XL	$8E-10$	$1E-8$	$9.2E-6$	0.9931

Table 4: Minimum points.

Geometry	X_{min} (°C)	Y_{min} (V)
Basic	−25	$6.83E-5$
L	−25	$2.41E-5$
XL	−6.25	$9.17E-6$

The fitting parameters of the three curves, according to the fitting equation in (∗), as well as the R^2 are depicted in Table 3. It is to be mentioned that the parabolic fitting of the measured data is a very good one, taking into account the values of R^2 approaching 1. This means that the respective parabolic functions fit best the experimental data. We immediately see that all three functions have minimum points.

Because it is important to know the temperature for which we obtain the minimum offset, we have calculated the minima of these three functions. The coordinates of the minimum points are (X_{min}, Y_{min}). These coordinates $(X_{min} = -b/2a, Y_{min} = -\sqrt{b^2 - 4ac}/4a)$, where the a, b, and c coefficients are the ones in Table 3, have been calculated and are included in Table 4, for the three Hall cells.

We can observe that the minimum is obtained at −25°C for basic and L Hall cells and at −6.25°C for XL Hall cell, respectively. The minimum offset obtained is $6.83E-5$ V for the basic cell, $2.41E-5$ V for L cell, and $9.17E-6$ V for XL cell. It is worth mentioning that the XL Hall cell exhibits an offset value more than seven times lower than the basic cell and more than twice less than the L cell.

6. Conclusion and Future Perspectives

The work in this paper offered a characterization of the cross-like Hall cells integrated in a regular bulk 0.35 μm XFAB CMOS technological process, from the point of view of their main parameters. The basic, L, and XL cells are included in this analysis. Experimental results for the absolute sensitivity, resistance, offset, and offset temperature drift are obtained.

To attain the objective of a complete analysis of the Hall cells, three-dimensional physical models have also been used. Therefore, the input resistance, Hall voltage, and absolute sensitivity have been also numerically estimated.

For the three cross-like Hall cells, the single-phase offset biasing current dependence and the variation of the four-phase residual offset with the temperature have been studied. A second-order parabolic dependence of the residual offset with the temperature was observed. The fitting coefficients have been extracted and the coordinates of the minima have been calculated. The temperatures guaranteeing the minimum offset have been identified for the three Hall cells.

The minimum residual four-phase offset voltage is obtained at −25°C for basic and L Hall cells and at −6.25°C for XL Hall cell, respectively. The minimum offset obtained is $6.83E - 5$ V for the basic cell, $2.41E - 5$ V for L cell, and $9.17E - 6$ V for XL cell.

The experimental results offer the resolution that the lowest offset belongs to the Hall cell with the highest dimensions (XL Hall cell). The residual offset of this cell is more than seven times lower than for basic cell and more than twice less than the offset of the L cell.

The next step is to estimate and measure the offset for SOI Hall cells, which have been recently integrated by the author.

Competing Interests

There are no competing interests related to this paper.

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References

[1] E. Ramsden, *Hall-Effect Sensors—Theory and Applications*, Elsevier, New York, NY, USA, 2nd edition, 2006.

[2] R. S. Popovic, *Hall Effect Sensors*, Institute of Physics Publishing, Bristol, UK, 2nd edition, 2004.

[3] M.-A. Paun, J.-M. Sallese, and M. Kayal, "Evaluation of characteristic parameters for high performance hall cells," *Microelectronics Journal*, vol. 45, no. 9, pp. 1194–1201, 2014.

[4] N. Singh and H. V. Estrada, "A high sensitivity Hall sensor fabricated on a SOI wafer using surface micromachining technique," in *Micromachining and Microfabrication Process Technology XIV*, M.-A. Maher, J.-C. Chiao, and P. J. Resnick, Eds., vol. 7204 of *Proceedings of SPIE*, pp. 1–8, 2009.

[5] M.-A. Paun, "Three-dimensional simulations in optimal performance trial between two types of hall sensors fabrication technologies," *Journal of Magnetism and Magnetic Materials*, vol. 391, Article ID 60172, pp. 122–128, 2015.

[6] S. Fischer and J. Wilde, "Modeling package-induced effects on molded Hall sensors," *IEEE Transactions on Advanced Packaging*, vol. 31, no. 3, pp. 594–603, 2008.

[7] T. Kaufmann, M. C. Vecchi, P. Ruther, and O. Paul, "A computationally efficient numerical model of the offset of CMOS-integrated vertical Hall devices," *Sensors and Actuators, A: Physical*, vol. 178, pp. 1–9, 2012.

[8] O. Paul, R. Raz, and T. Kaufmann, "Analysis of the offset of semiconductor vertical Hall devices," *Sensors and Actuators, A: Physical*, vol. 174, no. 1, pp. 24–32, 2012.

[9] A. Udo, M. Mario, and H. Michael, "Drift of magnetic sensitivity of smart Hall sensors due to moisture absorbed by the IC-package," in *Proceedings of the 3rd IEEE International Conference on Sensors*, pp. 455–458, Vienna, Austria, October 2004.

[10] Ch. S. Roumenin and S. V. Lozanova, "A novel offset reduction method using a two-outputs silicon parallel-field Hall device," in *Proceedings of the Electronics*, pp. 1–8, Bulgaria, September 2006.

[11] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, John Wiley & Sons, New York, NY, USA, 3rd edition, 2007.

[12] Synopsys TCAD Software Tools Online Documentation, http://www.synopsys.com/Tools/TCAD.

[13] M.-A. Paun, J.-M. Sallese, and M. Kayal, "A circuit model for CMOS hall cells performance evaluation including temperature effects," *Advances in Condensed Matter Physics*, vol. 2013, Article ID 968647, 10 pages, 2013.