

Research Article

Thermal Analysis of Si/GaAs Bonding Wafers and Mitigation Strategies of the Bonding Stresses

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In order to effectively reduce the thermal stresses of Si/GaAs bonding wafers during their annealing process, first of all, based on E. Suhir's bimaterial thermal stress theory, the thermal stresses in the wafer bonding interfaces are analyzed and the thermal stress distribution formulas are obtained. Then, the thermal stress distribution curves of Si/GaAs bonding interfaces are investigated by finite element method (FEM) and are compared with the results from E. Suhir's bimaterial thermal stress theory. Finally, some effective strategies are proposed to reduce the thermal stresses in the bonding interfaces.

1. Introduction

Wafer bonding is an important technology of the semiconductor process, in which wafers are directly attached under certain conditions. This technique can be mainly divided into three processes: surface treatment, prebonding, and annealing. During the annealing process, thermal stresses of prebonding wafers occur due to the different thermal expansion coefficients of the bonding materials. When the thermal stresses are too large, they will seriously affect bonding, resulting in a decrease in the quality and performance of the structure, even causing the wafers to be damaged. Thus, analyzing the mechanism and mitigation strategies of thermal stresses is of great importance to improve the quality of devices.

In this study, stresses in the wafer bonding interfaces are analyzed according to E. Suhir's bimaterial thermal stress theory [1] and the analytical solution of thermal stress distribution in Si/GaAs wafer bonding interfaces is calculated. In ANSYS Workbench finite element analysis, the simulation solution of the thermal stresses is obtained and then compared with the results from the analytical solution.

There are various methods to analyze thermal stresses of bonding wafers. In [2–7], the thermal stresses of bonding materials were analyzed by using a two-dimensional plane

structure. But they did not analyze the annealing process from the three-dimensional point of view and could not reflect the thermal deformation and thermal stress distribution. The references [2, 4, 6–9] analyzed the effect of annealing temperature on thermal stresses, while the influence of wafer thickness on thermal stresses was analyzed by [2, 5–7, 10]. The references [11, 12] analyzed the effect of annealing temperature on bonding strength. The influence of wafer thickness on bonding strength was analyzed by [13]. But only one or two measures were proposed to reduce the thermal stresses considering the annealing temperature or wafer thickness; the analysis of the factors which affect the thermal stresses was not comprehensive yet.

Planar and cross-sectional distributions of thermal stresses in the bonded InP/Si pairs were analyzed by the two-dimensional finite element method in [14]; the authors analyzed the effect of annealing temperatures and wafer thicknesses on the thermal stresses by an analytic method. But [14] did not combine theory and finite element analysis to discuss the measures to reduce the thermal stresses, and the distributions of thermal stress were not concrete. In view of the research results and limitations mentioned above, this paper aims at the bonding problems of Si and GaAs. The thermal stresses of the bonding wafers are analyzed through both E. Suhir's bimaterial thermal stress theory

and three-dimensional finite element simulation. The visual displacement contours and the stress curve diagrams are obtained and the approaches to mitigate the adverse effect of thermal stresses are proposed and studied.

Besides the thermal-mismatch stresses, the lattice-mismatch stresses are the other type of stresses in the bimaterial semiconductor. E. Suhir compared these two types of stresses by the theoretical derivation and several examples in [15]. As for the lattice-mismatch stresses, an effective and physically meaningful analytical predictive model was developed to evaluate the lattice-mismatch stresses in a semiconductor film grown on a circular substrate by E. Suhir in [16], and it was concluded that the shearing stress of the theory-of-elasticity prediction was larger than that of the strength-of-material one.

As mentioned above, the thermal-mismatch stresses and the lattice-mismatch stresses are two types of stresses. This paper focuses on the thermal-mismatch stresses of the Si/GaAs bonding wafer by Suhir's bimaterial thermal stress theory [1] and three-dimensional finite element simulation. As for the lattice-mismatch stresses of the Si/GaAs bonding wafer and the comparison between its lattice-mismatch stresses and the thermal-mismatch stresses, they will be discussed in the near future.

2. Model and Analytical Equation of the Thermal Stresses

In this study, we mainly discuss the bonding condition of Si and GaAs. Set the thickness of Si to $50 \mu\text{m}$, Young's modulus to $E_1 = 1.66 \times 10^{11} \text{ Pa}$, Poisson's ratio to $\mu_1 = 0.29$, and the coefficient of thermal expansion to $\alpha_1 = 2.6 \times 10^{-6} \text{ K}^{-1}$. Set the thickness of GaAs to $300 \mu\text{m}$, Young's modulus to $E_2 = 8.526 \times 10^{10} \text{ Pa}$, Poisson's ratio to $\mu_2 = 0.31$, and the coefficient of thermal expansion to $\alpha_2 = 6.4 \times 10^{-6} \text{ K}^{-1}$. Both of the radii of two wafers are 5 mm. Both the upper and the side surfaces of Si and the side surface of GaAs are all unconstrained, while the lower surface of Si and the upper surface of GaAs are bound constraints. And the wafers are placed on a rigidity plane. The temperature changes from 300°C to 20°C . The temperature change is set to be uniform, the bonded wafer interface is without cavity, the thermal expansion coefficient is linear, elastic, and isotropic, and material parameters are independent of time and temperature [2]. Meanwhile, assume that the wafers are free of stress at their initial annealing temperature (300°C).

When the temperature changes, the shearing stresses $\tau(x)$, peeling stresses $p(x)$, and normal stresses (radial normal stresses $\sigma(x)$ and circumferential normal stresses $\psi(x)$) are generated near the surface of the bonding wafers. The shearing stresses and normal stresses are parallel to the bonding interfaces, and the peeling stresses are perpendicular to the bonding interfaces. Figure 1 shows the stresses distribution during the annealing process, and the circumferential normal stress is perpendicular to the xoz plane.

Figure 1 is the schematic diagram of the bonding structure of two circular wafers with the same diameter and the total thickness is h (the thickness of Si is h_1 and the thickness

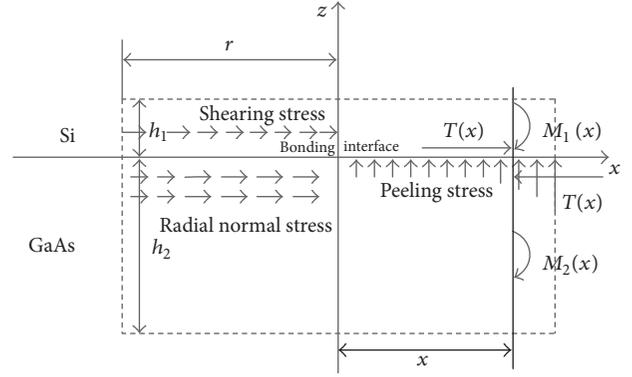


FIGURE 1: Schematic diagram of stress distribution of the wafers during the annealing process.

of GaAs is h_2). $T(x)$ is the shearing force (the direction of the force is parallel to the bonding interfaces) per unit width (z -axis) of the wafer bonding interfaces. The thickness of the bonding wafers is small, so the shearing force can be regarded as a uniform distribution in the direction of wafer thickness, so

$$T(x) = \int_{-r}^x \tau(\xi) d\xi. \quad (1)$$

In this equation, $\tau(\xi)$ is the shearing stress per unit length (x -axis) of bonding interfaces and r is the radius of the wafers.

To investigate the force and equilibrium of the bonding wafers at the cross section, the moment balance equations of the x cross section are

$$\begin{aligned} M_1(x) - \frac{h_1}{2} T(x) &= 0, \\ M_2(x) - \frac{h_2}{2} T(x) &= 0, \end{aligned} \quad (2)$$

where $M_1(x)$ and $M_2(x)$ are two bending moments at the x cross section of the wafers:

$$\begin{aligned} M_1(x) &= \frac{E_1^* h_1^3}{12\rho(x)}, \\ M_2(x) &= \frac{E_2^* h_2^3}{12\rho(x)}, \end{aligned} \quad (3)$$

where the effective Young moduli of the two wafers are $E_1^* = E_1/(1 - \mu_1^2)$ and $E_2^* = E_2/(1 - \mu_2^2)$, E_1 and E_2 are Young's moduli of the two wafers, μ_1 and μ_2 are Poisson's ratios of the two kinds of materials, and $\rho(x)$ is the radius of curvature of the bonding wafers.

According to Suhir's bimaterial thermal stress theory, the shearing stresses in the bonding interfaces are [17]

$$\tau(x) = \frac{K\Delta\alpha\Delta T}{\lambda} e^{-K(r-x)}, \quad (4)$$

where $K^2 = \lambda/k$, $\lambda = (E_1 h_1 + E_2 h_2)\eta / (E_1 h_2 + E_2 h_1)h_1 h_2 + (h_1 + h_2)^2 / 4D$, where $\eta = h_1/E_1^* + h_2/E_2^*$ is the lateral (z -axis) flexibility coefficient of the wafers, $D = D_1 + D_2$, where

$D_1 = E_1 h_1^3 / 12(1 - \mu_1^2)$ and $D_2 = E_2 h_2^3 / 12(1 - \mu_2^2)$ are the coefficients of bending stiffness of two wafers, $k = k_1 + k_2$, where $k_1 = 2(1 + \mu_1)h_1 / 3E_1$ and $k_2 = 2(1 + \mu_2)h_2 / 3E_2$ are the longitudinal (z -axis) flexibility coefficients of two wafer bonding interfaces, $\Delta\alpha = \alpha_2 - \alpha_1$, where α_1 and α_2 are the thermal expansion coefficients of the two kinds of materials, and ΔT is the high and low temperature difference during the annealing process.

The peeling stresses are [17]

$$p(x) = \kappa m \frac{\Delta\alpha\Delta T}{\lambda} \left\{ n e^{-\beta(r-x)} \left[\sin(\beta(r-x)) + \left(\frac{K}{\beta} - 1 \right) \cos(\beta(r-x)) \right] + e^{-K(r-x)} \right\}, \quad (5)$$

where $\kappa = (h_1 D_2 - h_2 D_1) / 2D$, $\beta = (D / 4\eta D_1 D_2)^{1/4}$, $m = 4\beta^4 K^2 / (K^4 + 4\beta^4)$, and $n = K^2 / 2\beta^2$.

The radial normal stresses (tensile stress or compressive stress) are determined by the shearing force $T(x)$ and bending moment $M_i(x)$ ($i = 1, 2$) of the wafers. Combining formulas (1), (3), and (4), we can get the expression of the radial normal stresses of Si and GaAs bonding interfaces [18]:

$$\begin{aligned} \sigma_1(x) &= -\frac{T(x)}{h_1} - \frac{E_1^*}{\rho(x)} \times \frac{h_1}{2} \\ &= -\frac{\Delta\alpha\Delta T}{\lambda h_1} \left(1 + \frac{3hD_1}{h_1 D} \right) [1 - e^{-K(r-x)}], \end{aligned} \quad (6)$$

$$\begin{aligned} \sigma_2(x) &= \frac{T(x)}{h_2} + \frac{E_2^*}{\rho(x)} \times \frac{h_2}{2} \\ &= \frac{\Delta\alpha\Delta T}{\lambda h_2} \left(1 + \frac{3hD_2}{h_2 D} \right) [1 - e^{-K(r-x)}], \end{aligned} \quad (7)$$

where “+” indicates that the radial normal stress is tensile stress and “-” indicates that the radial normal stress is compressive stress. This is because the thermal expansion coefficient of GaAs is larger than that of Si. In the cooling process, the shrinkage of GaAs is larger than the shrinkage of Si, leading to GaAs being subjected to tensile stress and Si being subjected to compressive stress.

3. Finite Element Thermal Analysis of the Structure

In this study, the finite element method is utilized to analyze the bonding stresses between Si and GaAs and the stress curves are obtained. The result is compared with that from Suhir's bimaterial thermal stress theory in the two-dimensional space. Further, the finite element method is extended to three-dimensional space, and the visual displacement contours of the structure are given.

The circular structure model is established by SolidWorks, as shown in Figure 2, and the local finite element model is shown in Figure 3. The plane of the circular disk structure is a horizontal plane (xoy plane), and the z -axis is perpendicular to the disk structure. Hexahedral meshes are

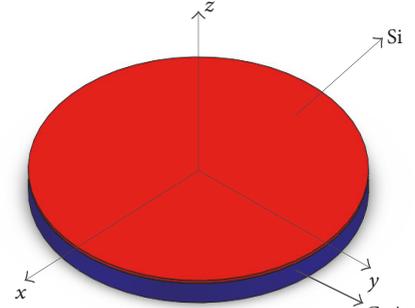


FIGURE 2: Overall schematic diagram of the disk structure.

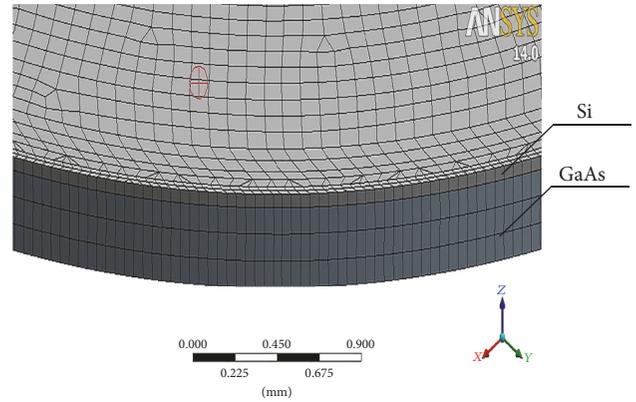


FIGURE 3: The schematic diagram of the local finite element.

used in the overall structure, and the mesh density on the edge of the structure is increased by the manual intervention in order to get a more accurate result.

We can obtain the curves of the shearing stress, peeling stress, and radial normal stresses in the bonding interfaces at 20°C by theoretical expression of the thermal stresses and FEM software ANSYS Workbench, respectively, as shown in Figures 4, 5, and 6.

Figures 4, 5, and 6 show that the shearing stress, peeling stress, and radial normal stresses of the bonding interfaces change obviously in the edge area of the wafers (radius 4.5 mm–5 mm). It can be seen from the figures that the distributions and variation trends of the thermal stresses from the theoretical solution are similar to those from the simulation solution. In addition, the theoretical solution curves of shearing stress and finite element simulation solution of shearing stress are basically coincident, and mutual verifications are obtained. But the relative error of the maximum radial normal stress of Si is $(110 - 87.41) / 110 = 20.5\%$, while the relative error of the maximum radial normal stress of GaAs is $(75.1 - 54.9) / 75.1 = 26.9\%$. The reasons of that are some approximate calculations in the theoretical solution and the certain errors in the simulation solution. By the finite element simulation analysis, the shearing stresses and peeling stresses of the two kinds of materials are exactly the same; this is consistent with the results of formulas (4)

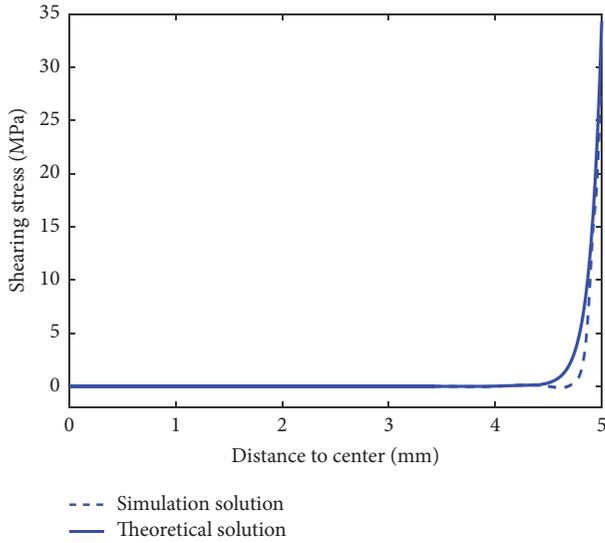


FIGURE 4: Theoretical solution and simulation solution distributions of the shearing stress.

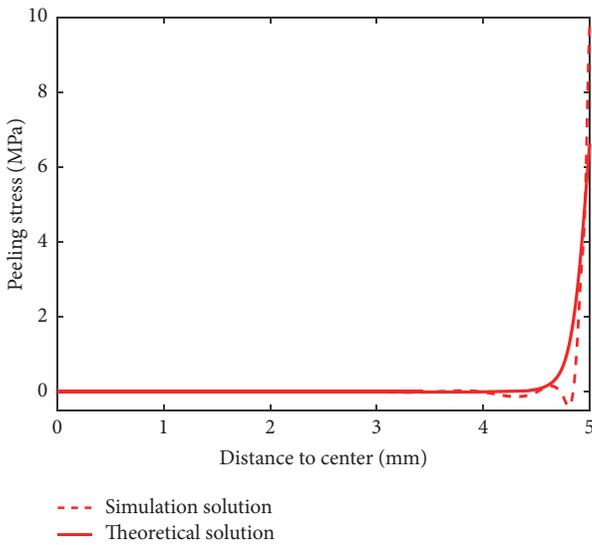


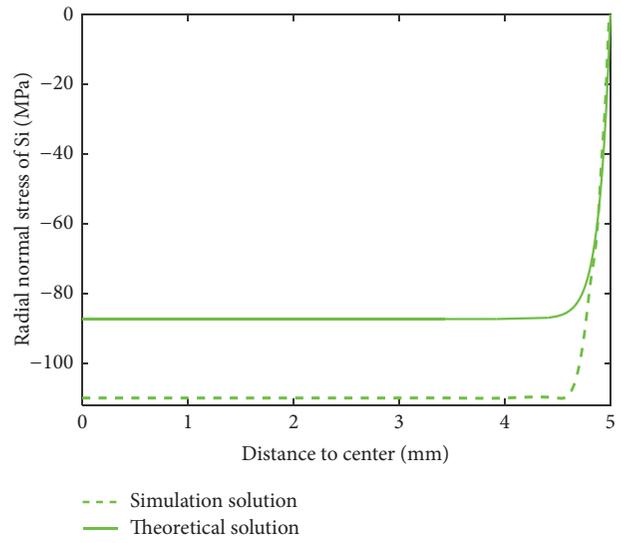
FIGURE 5: Theoretical solution and simulation solution distributions of the peeling stress.

and (5) in the second section. Therefore, only one shearing stress and one peeling stress are analyzed. The radial normal stresses and circumferential normal stresses are the same, which are perpendicular to each other and parallel to the bonding interfaces, so it is only necessary to analyze the radial normal stresses.

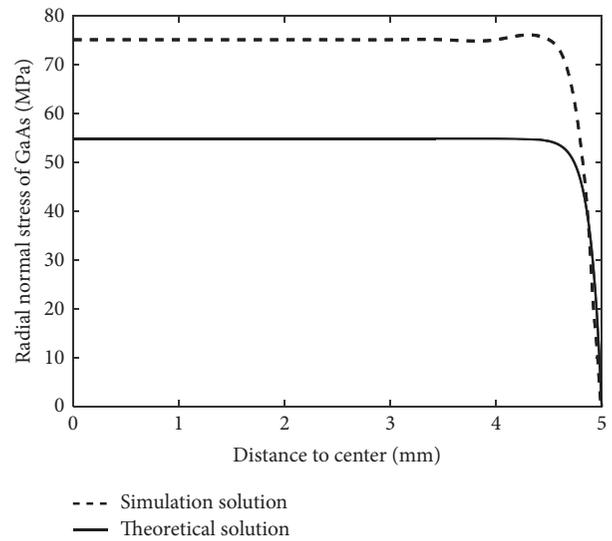
4. Thermal Deformation Analysis of the Structure

As shown in Figure 7, when the temperature of the structure is changed from 300°C to 20°C, the displacement contours in the x -axis and z -axis are generated

During the annealing process, as the temperature decreases from 300°C to 20°C, the bonding wafers in x



(a) Radial normal stress of Si



(b) Radial normal stress of GaAs

FIGURE 6: Theoretical solution and simulation solution distributions of the radial normal stresses.

direction and z direction shrink due to cold contraction, resulting in negative displacement in x direction. As shown in Figure 7(a), the displacement direction is $-x$ on the positive half axis of x , and the displacement is negative. The displacement direction is $+x$ on the negative half axis of x , and the displacement is positive. The maximum displacement values of x direction and y direction are both 0.010519 mm, and their ratio to the radius is $0.010519/5 = 0.0021$. In the bonding structure, Si is the upper layer and the lower layer is GaAs. The linear expansion coefficient of GaAs is $6.4 \times 10^{-6} \text{ K}^{-1}$, which is larger than that of Si, resulting in the shrinkage of GaAs being bigger than that of Si during the cooling process and the bonding structure protruding upwards. The maximum displacement in z direction is 0.037991 mm and its ratio to the wafer thickness is $0.037991/0.35 = 0.1085457$. It can be seen that the relative

TABLE I: Radial normal stresses away from the edge region of the bonding interfaces with different radii.

Radii (mm)	5	10	20	30	40	50
Radial normal stresses (MPa)						
Lower surface of Si	-113.4	-113.5	-113.4	-113.5	-113.5	-113.5
Upper surface of GaAs	71.5	71.6	71.5	71.6	71.5	71.5

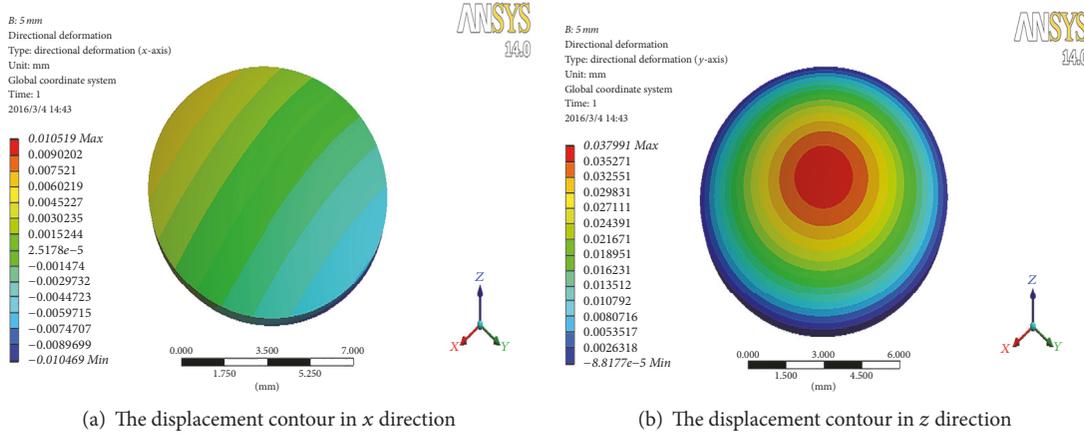


FIGURE 7: The displacement contours of the wafers.

displacement of the wafers in the axial direction is larger than that in the radial direction, but both of them are small.

As shown in Figure 7(a), the radial and circumferential displacement values at the edge of the wafers are larger, and the wafer interface is easier to slip and promotes the diffusion of dislocations. Thus, the shearing stresses and peeling stresses in the bonding interfaces are almost zero in the center of the wafers and increase dramatically in the edge area. From Figure 7(b), due to the effect of the bending moment, the central region of the structure protrudes upwards, the bending moment from the center to the edge is reduced to 0. The normal stresses are mainly affected by the bending moment and the shearing force, which confirms the trend from the center to the edge.

5. Mitigation Strategies of Thermal Stresses in the Bonding Interfaces

5.1. *Analysis of Different Radius Bonding Structures.* From the above analysis, it can be clearly seen that the normal stresses (the radial normal stresses and circumferential normal stresses) are the main factors of the failure of the central region in the wafers and the shearing stresses and peeling stresses are the main reasons for the failure of the edge in the wafers. According to these features, the radial normal stresses away from the edge region of the wafers are studied with different radii. The radii are arranged as 5 mm, 10 mm, 20 mm, 30 mm, 40 mm, and 50 mm, respectively, as shown in Table 1.

Based on the finite element simulation analysis, it can be found that the radial normal stresses away from the edge of different radius structures are basically unchanged, while the shearing stresses and peeling stresses are basically zero in

the central area. Therefore, in the actual production process within a certain radius, in order to effectively reduce the thermal stresses of the structure, the radii of wafers can be increased, that is, larger than the 10% required, and then the thermal stresses can be reduced by means of cutting the edge of the wafers.

5.2. *Effect of the Annealing Temperature.* According to the theoretical analysis of the second section, the annealing temperature affects the thermal stresses of the bonding interfaces. From the above modeling results, it is noted that the peeling stresses and shearing stresses at the edge area are the largest ones, while the normal stresses at the edge area are the minimum. The peeling stresses and shearing stresses away from the edge area are zero, while the normal stresses get their maximum at the edge area. Figure 8 shows the curves of maximum thermal stresses in the bonding interfaces at room temperature with different annealing temperatures (data from Si/GaAs bonding wafers with a radius of 10 mm).

As shown in Figure 8, it is noted that the magnitude of thermal stresses increases linearly with the increase of annealing temperature. The higher the annealing temperature is, the greater the thermal stresses are. Therefore, reducing the annealing temperature is one of the effective methods to reduce the thermal stresses under the condition that the wafers can be properly bonded.

5.3. *Effect of the Thicknesses of Si and GaAs.* Figure 9 shows the curves of maximum value of thermal stresses (shearing stresses, peeling stresses, and radial normal stresses) in the Si/GaAs bonding interfaces with a radius of 10 mm at 20°C with the various wafer thicknesses when the annealing temperature is 300°C.

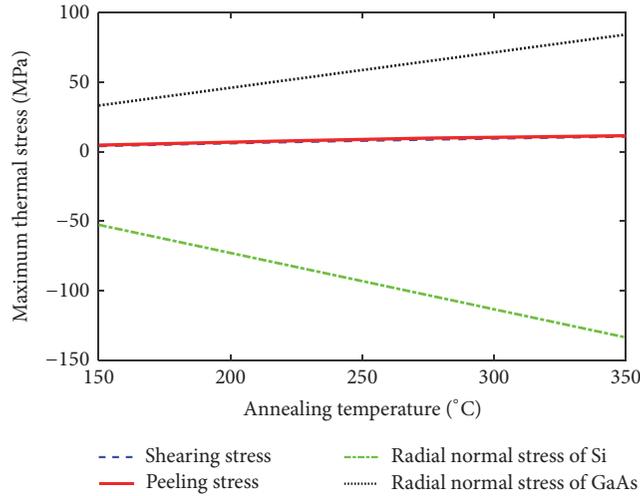


FIGURE 8: Maximum thermal stresses at different annealing temperatures.

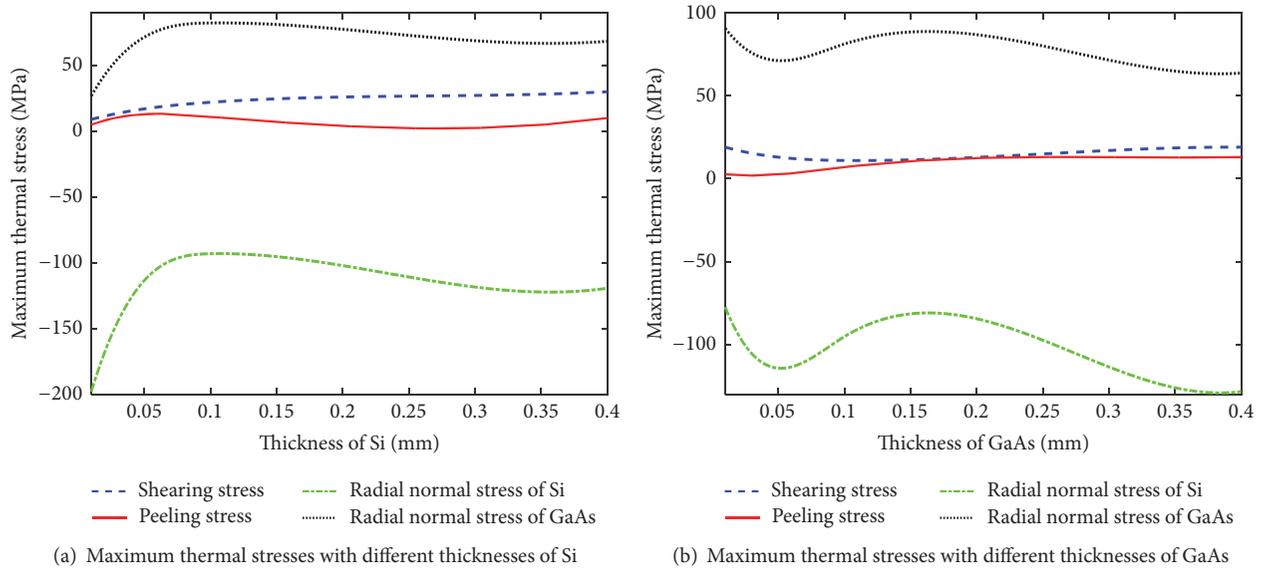


FIGURE 9: The diagrams of maximum thermal stresses in bonding interfaces with different thicknesses.

Figure 9(a) indicates that when the thickness of GaAs is 0.3 mm, the maximum values of thermal stresses change with the increase of the thickness of Si. Figure 9(b) shows that the maximum values of thermal stresses vary with the change of the thicknesses of GaAs when the thickness of Si is 0.05 mm.

It can be seen from Figure 9 that when the thickness of GaAs is 0.3 mm, the thermal stresses increase gradually as the thickness of Si increases from 0.01 to 0.05 mm. The shearing stress and peeling stress are almost unchanged in the range of 0.05 to 0.4 mm. The radial normal stresses decrease slowly as the thickness of Si increases from 0.1 to 0.4 mm.

As the thickness of Si is 0.05 mm, the thermal stresses have local minimum as the thickness of GaAs is 0.05 mm. The shearing stress and peeling stress are almost constant in the 0.1–0.4 mm range. The radial normal stress decreases when the thickness of Si increases from 0.15 to 0.4 mm.

From Figure 9(a), it can be seen that when the thickness of GaAs is 0.3 mm and the thickness of Si is 0.05 mm, the radial normal stress is relatively small and the peeling stress and shearing stress increase slightly. From Figure 9(b), it is noted that when the thickness of Si is 0.05 mm and the thickness of GaAs is 0.1 mm, the radial normal stress is relatively small, and the peeling stress and shearing stress increase slightly. These two structures can effectively alleviate the adverse effect of thermal stresses in the bonding interfaces.

6. Conclusion

In this study, the thermal stresses in the bonding interfaces are analyzed by Suhir's bimaterial theory. The thermal stress distribution in the bonding interfaces is obtained and the results are compared with the FEM simulation solutions.

Based on the comparison, the following conclusions can be made:

- (1) By analyzing the thermal stresses (the shearing stresses, peeling stresses, and normal stresses) in the bonding interfaces, the theoretical analysis is consistent with the FEM simulation results. The shearing stresses and peeling stresses are zero in most areas of the center, but they only increase abruptly in the edge region. The radial normal stresses are certain values in most areas of the center, and they gradually reduce to zero in the edge region. In view of the analysis above, in a certain radius, in order to effectively reduce the thermal stresses, we can make wafer radius 10% larger than that required, and then the thermal stresses can be reduced by means of cutting the edge of the wafers.
- (2) Under the condition that the wafers can properly be bonded, decreasing the annealing temperature is an effective approach to reduce the thermal stresses.
- (3) As the thickness of Si is 0.05 mm and the corresponding thickness of GaAs is 0.1 mm or the thickness of GaAs is 0.3 mm and the corresponding thickness of Si is 0.05 mm, the radial normal stresses are relatively small, and the peeling stresses and shearing stresses increase slightly, which can greatly reduce the thermal stresses in the bonding interfaces. Therefore, the adverse effect of thermal stresses on bonding can be mitigated by changing the thickness of the two bonding wafers.

7. Future Work

The anticipated future work should include but might not be limited to the following major efforts:

- (1) This paper aims at a bonding wafer with a thin Si on top of a thick GaAs for a solar cell specially. A reversed scenario with a thin GaAs on top of a thick Si in the common practical applications will be researched in the next research paper.
- (2) This paper focuses on the thermal-mismatch stresses in the bonding wafer for a solar cell. However, it is a meaningful subject to explore the lattice-mismatch stresses and the comparison between the lattice-mismatch stresses and the thermal-mismatch stresses in bonding wafers in the next research paper.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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