

Research Article

Effects of Die-Attach Quality on the Mechanical and Thermal Properties of High-Power Light-Emitting Diodes Packaging

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The reliability of high-power light-emitting-diode (LED) devices strongly depends on the die-attach quality because voids may increase junction temperature and total thermal resistance of LED devices. Die-attach material has a key role in the thermal management of high-power LED package by providing low-contact thermal resistance. Thermal and mechanical analyses were carried out by experiments and thermal simulation. The quantitative analysis results show that thermal resistance of die-attach layer (thermal resistance caused by die-attach material and voids in die-attach layer) plays an important role in total thermal resistance of high-power LED packaging according to the differential structure function of thermal transient characteristics. The increase of void fraction in die-attach layer causes the increases of thermal resistance of die-attach layer; the thermal resistance increased by 1.95 K/W when the void fraction increased to 62.45%. The voids also make an obvious influence on thermal stress and thermal strain of chip; the biggest thermal stress of chip was as high as 847.1 MPa compared to the 565.2 MPa when the void fraction increases from being void-free to 30% in the die-attach layer.

1. Introduction

High-power LED is promising candidate for fourth-generation lighting source due to its high brightness, long life, energy-saving, bright in color, and so on [1–5]. The reliability of electronics restricts the wider application of high-power LED. Poor heat dissipation can influence high-power LED's reliability such as the service life and the light efficiency [6–8]. And there are some papers showing that if the temperature of the LED device rises to 2°C, the reliability can be reduced 2%–10% [8, 9]. The life will reduce 50% if the temperature of the LED device rise 10°C. [3]. Improving the ability of thermal management and reducing the chip junction temperature have become a paramount thing to improve the performance of high-power LED. Therefore, the problem of heat dissipation is a major challenge for LED packaging [10]. Many researchers mainly studied on thermal design of LED packaging and the development of new packaging materials to improve the heat dissipation performance of high-power LED devices [11–13]. Die-attach material is worth

studying because thermal resistance of die-attach layer plays an important role in thermal resistance of LED packaging [14, 15].

Au/Sn eutectic, silver paste, and solder paste are often used as die-attach material in the LED package. Au/Sn bonding has the best mechanical and thermal properties, because Au/Sn eutectic has the lowest contact thermal resistance in the above three die-attach materials [16]. In order to improve the heat dissipation performance of LED devices, it is urgent to search for a new die-attach material. Three different die-attach materials, which are silver paste, solder paste, and add a little of carbon nanotubes in solder paste, solder paste with a little carbon nanotubes, have higher thermal conductivities than silver paste and solder paste, which is advantageous for heat dissipation. So solder paste with a little of carbon nanotubes is advantageous to reduce interface thermal resistance in the LED package [17]. Kim et al. [18] described several common die-attach materials for LED packaging; they studied die-attach materials based on a series of experiment methods, such as thermal transient analysis, and cross-sectional

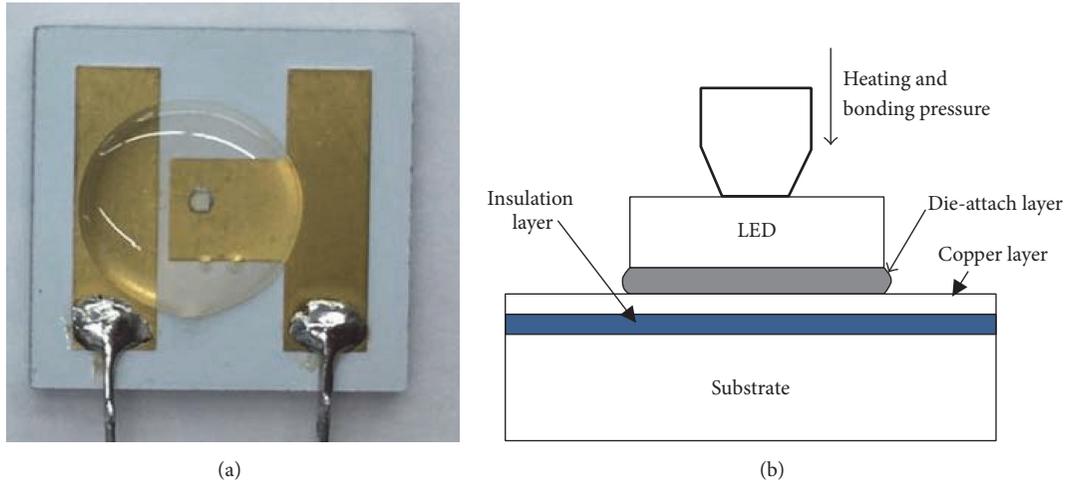


FIGURE 1: Packaged HP-LED and eutectic process diagram.

analysis. The results show that reliability of packaged electronics strongly depends on die-attach quality. Poor die-attach quality can also cause failure of LED devices, the defect in die-attach layer can be found by T3Ster thermal transient tester and scanning electron microscope (SEM) [19].

Generally, study found that voids have an important influence on thermal resistance of LED devices, but it failed to quantitatively analyze voids in die-attach layer. In this study, the effects of void fraction in the die-attach layer to the thermal and mechanical (thermal stress and strain) properties of LED are carried out by experiments and simulation.

2. Experiment, Results, and Discussion

In this experiment, LED packaging is chip on board (COB). The substrate is aluminum with insulation layer. The LED chip is about 1 mm * 1 mm * 0.16 mm. The die-attach material is solder paste (Sn 96.5 wt%, Ag 3.0 wt%, Cu 0.5 wt%). The packaged LED modules are as shown in Figure 1(a).

In this experiment, eutectic process is used to interconnect the LED devices; the process diagram is as shown in Figure 1(b).

In order to achieve the same void fraction with varying thickness under the bonding pressure, an experiment with different die-attach layer thickness is carried out. In this experiment, the solder paste is coated by screen printing method for one time, two times, and three times, respectively. And then the LED devices with almost the same void fraction are selected to test the thermal resistance and thickness of the die-attach layer.

Experiment tests for packaged HP-LED modules were carried out by thermal resistance test (T3Ster), cross-sectional analysis, and X-ray.

2.1. Effect of Different Void for Thermal Resistance of Die-Attach Layer. Figures 2 and 3 show the effect of void fraction to the thermal resistance of die-attach layer. Bonding pressures are 0 N, 0.3 N, 0.6 N, 1.2 N, and 2 N, respectively.

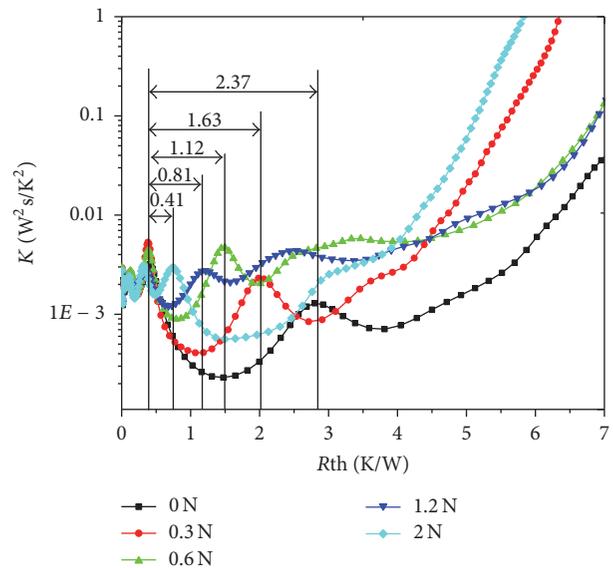


FIGURE 2: Thermal resistance of LED die-attach layer with different bonding pressure.

Different bonding pressure corresponds to different void fraction in die-attach layer as shown in Figure 3. Figure 2 shows different void fraction resulting in thermal resistance of die-attach layer which are 2.37°C/W, 1.63°C/W, 1.12°C/W, 0.81°C/W, and 0.41°C/W, respectively. It was found that thermal resistance of die-attach layer increases with the increase of void fraction in die-attach layer.

The X-ray results of the LED device were tested as Figure 3 and the void fraction of die-attach layer was automatic calculated by the equipment software.

The relatively white areas in Figure 3 are the voids; the more area of the higher brightness white areas, the higher void fraction in the die-attach layer; the void fraction of die-attach layer with different bonding pressure is shown in Table 1.

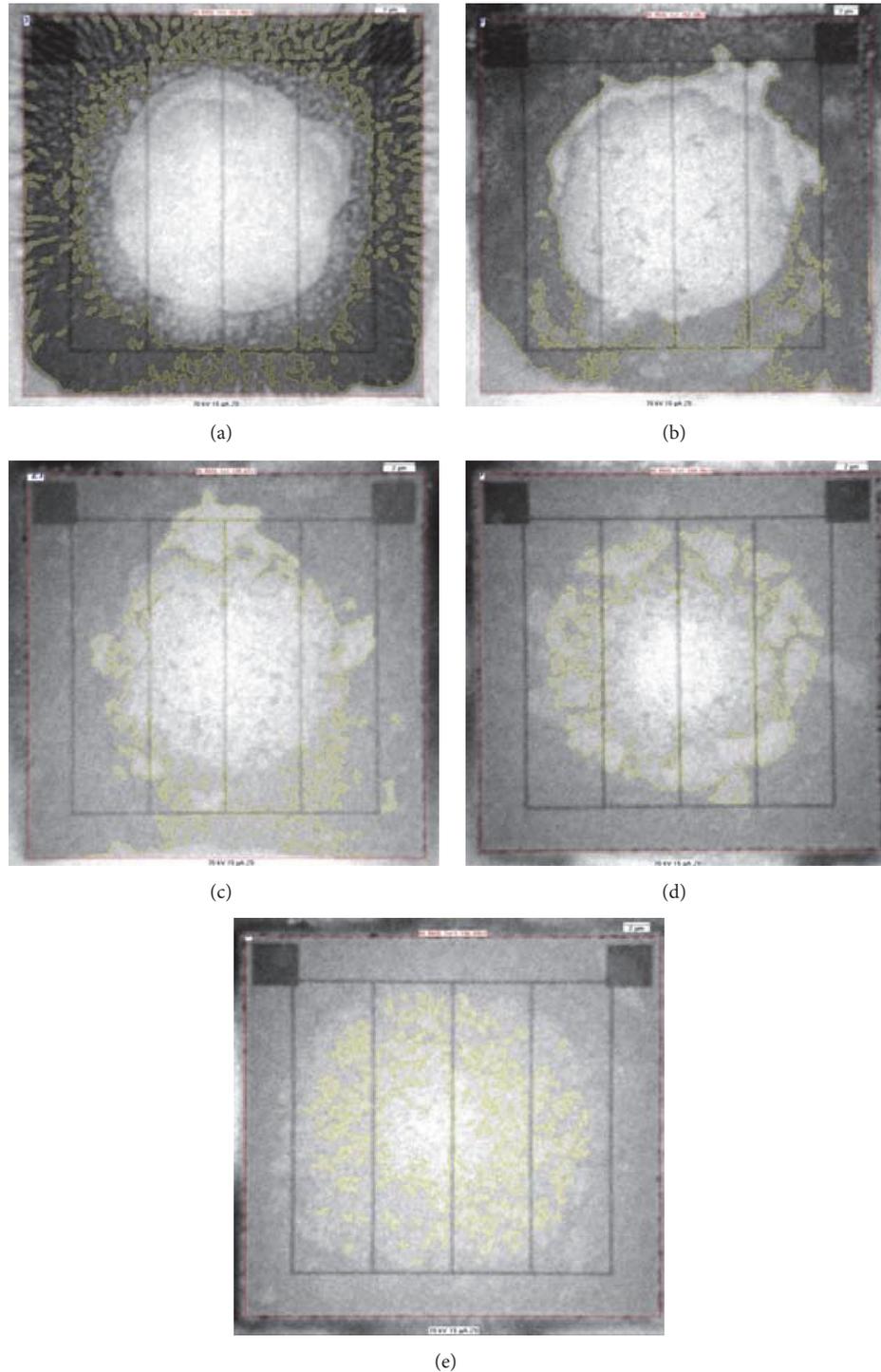


FIGURE 3: The X-ray results of voids in die-attach layer of high-power LED with different bonding pressure: (a) 0 N, (b) 0.3 N, (c) 0.6 N, (d) 1.2 N, and (e) 2 N.

Table 1 shows that the void fraction was as high as 62.45% when the bonding pressure was 0 N, while it was only 16.53% when the bonding pressure was 2 N. These results show that the void fraction was decreased significantly with the increase of bonding pressure.

LED devices with different bonding pressure were cut and polished to obtain cross-sectional images. The optical microscope images are as shown in Figure 4.

The thicknesses of die-attach layer with different bonding pressure are 38.8 μm , 29 μm , 16.7 μm , 14.6 μm , and 8.4 μm

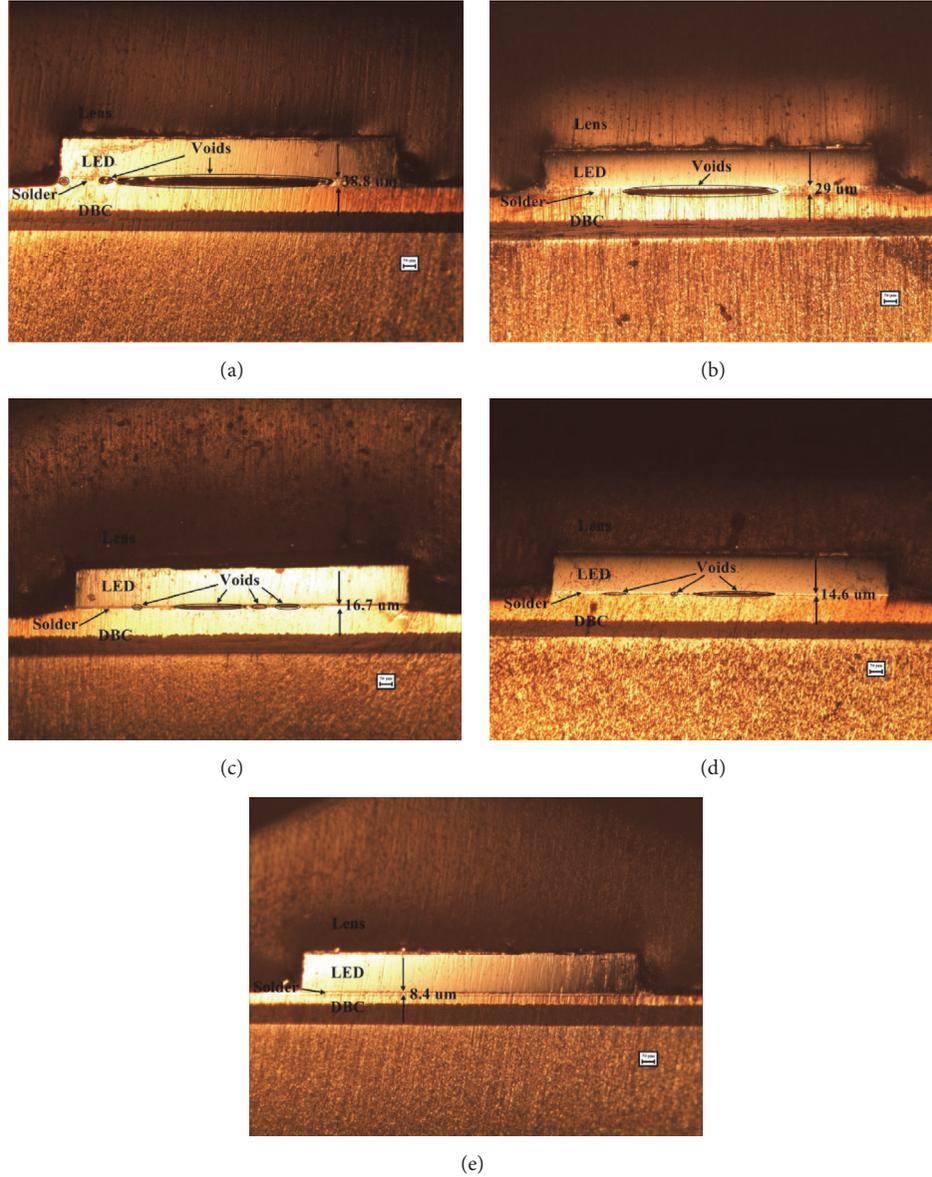


FIGURE 4: Thickness and voids of die-attach layer with different bonding pressure: (a) 0 N, (b) 0.3 N, (c) 0.6 N, (d) 1.2 N, and (e) 2 N.

TABLE 1: Void fraction of die-attach layer under different bonding pressure.

Pressure of bonding (N)	Void fraction (%)	Thickness of die-attach layer (μm)	Volume of die-attach (mm ³)
0	62.45%	38.8	0.0146
0.3	52.60%	29	0.0137
0.6	39.67%	16.7	0.0101
1.2	29.76%	14.6	0.0103
2	16.53%	8.4	0.007

respectively. Figure 4 shows that the bigger the bonding pressure, the thinner the die-attach layer. It is obvious that the void fractions decrease with the increase of bonding pressure.

The thermal resistance of material is related to thermal conductivity coefficient of material, heat transfer area, and thickness of material as shown

$$R_{th} = \frac{L}{KA}, \quad (1)$$

where K and L are the thermal conductivity coefficient and thickness of the die-attach material and A is the heat transfer area.

By (1) and Table 2, the thicknesses of die-attach layer change from 38.8 μm to 8.4 μm and the thermal resistance of material reduced about 0.35°C/W, but thermal resistance of die-attach layer reduced 1.96°C/W. The thermal resistance of material accounted for only a relatively small proportion of the whole thermal resistance of die-attach layer.

Bonding pressure increase leads to a thickness decrease of die-attach layer as shown in Figure 5. A much more number

TABLE 2: Thermal resistance of LED packaged with different bonding pressure.

Void fraction	Thickness of die-attach layer (μm)	Thermal resistance of material (calculated) ($^{\circ}\text{C}/\text{W}$)	Thermal resistance of die-attach layer (experiment) ($^{\circ}\text{C}/\text{W}$)	Thermal resistance caused by voids in die-attach layer (calculated) ($^{\circ}\text{C}/\text{W}$)
62.45%	38.8	0.45	2.37	1.95
52.60%	29	0.34	1.63	1.29
39.67%	16.7	0.19	1.12	0.93
29.76%	14.6	0.17	0.81	0.64
16.53%	8.4	0.1	0.41	0.31

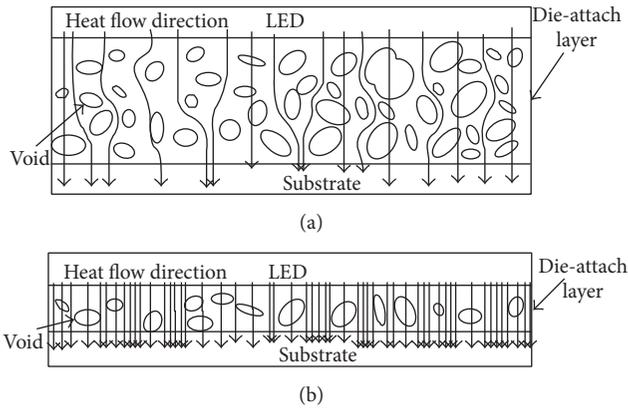


FIGURE 5: (a) The diagram of heat transfer when bonding pressure is 0 N and (b) the diagram of heat transfer when bonding pressure is 2 N.

of bubbles are discharged from die-attach layer with the added pressure which lead to the void fractions decreases. The, more heat is conducted to the substrate because thermal conductivity of air is very small. So it is an effective method to improve the thermal resistance of die-attach layer by reducing void fraction in the die-attach layer.

For the LED device with about 7% void fraction, the die-attach layer varies from $5.63 \mu\text{m}$ to $7.41 \mu\text{m}$ and the thermal resistance of the die-attach layer increases from $9.27^{\circ}\text{C}/\text{W}$ to $10.14^{\circ}\text{C}/\text{W}$, such as Figure 6. The variation is not obvious, as, in (1), the thermal conductivity of the die-attach layer, the void fraction (area), and the thickness all can be the reason. In the experiments, the thermal conductivity of the die-attach layer is as high as $67 \text{ W}/(\text{mK})$ and K is relatively the main influencing factor. The void fraction is only about 7%, the heat dissipation can be efficient so the $\sim 2 \mu\text{m}$ thickness cannot induce distinct increase of the thermal resistance of the die-attach layer.

3. Finite Element Analysis, Results, and Discussion

In the thermal simulation, the dimensions of the LED chip and substrate are $1 \text{ mm} \times 1 \text{ mm}$ and $18 \text{ mm} \times 18 \text{ mm}$, respectively. The heat generation rate is $4.375 \times 10^9 \text{ W}/\text{m}^3$ which is loaded on the chip ($1 \text{ W} \times 0.7/(1 \text{ mm} \times 1 \text{ mm} \times 0.16 \text{ mm})$), assuming that the ambient temperature is 20°C

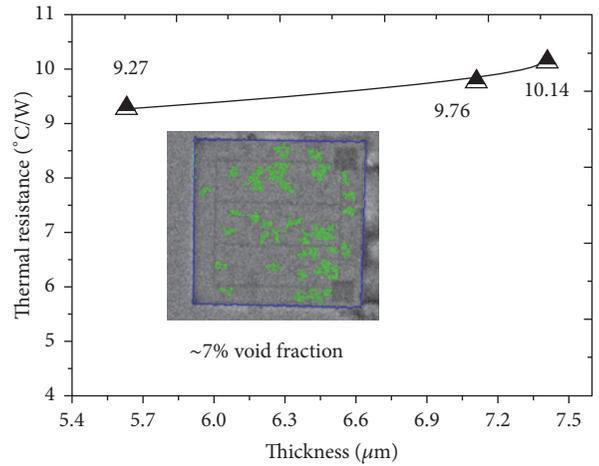


FIGURE 6: The thermal resistance varies with the thickness of die-attach layer under the bonding pressure.

TABLE 3: Composition and thermal parameter of LED modules.

Composition	Chip	Die-attach layer	Al	Copper	Lens
Thermal conductivity (W/mK)	180	51	236	385	0.3
Thickness (mm)	0.16	0.02	1	0.07	
Coefficient of thermal expansion ($10^{-6} \text{ }^{\circ}\text{C}^{-1}$)	7.5	25	23	16.4	8
Young's modulus (GPa)	410	26	71.7	110	55
Poisson's ratio	0.14	0.365	0.33	0.34	0.25

AND the air convection coefficient is $10 \text{ W}/(\text{m}^2 \text{ K})$. The physical parameters of LED modules are as in Table 3.

In order to investigate the influences of the void fraction to the mechanical properties of LED modules, finite element simulations are carried out. Figure 7(a) shows a temperature distribution of LED modules and the die-attach layer was shown as in Figure 7(b).

The heat generated by chip conducted to the substrate from chip is mainly through the die-attach layer and then to the environment by air convection. If the die-attach layer entrapped a lot of voids, the heat conduction will be seriously affected as shown in Figure 5(a).

Figures 8(a) and 8(c) show that the biggest thermal stress and thermal strain of the LED chip were only 565.2 MPa and

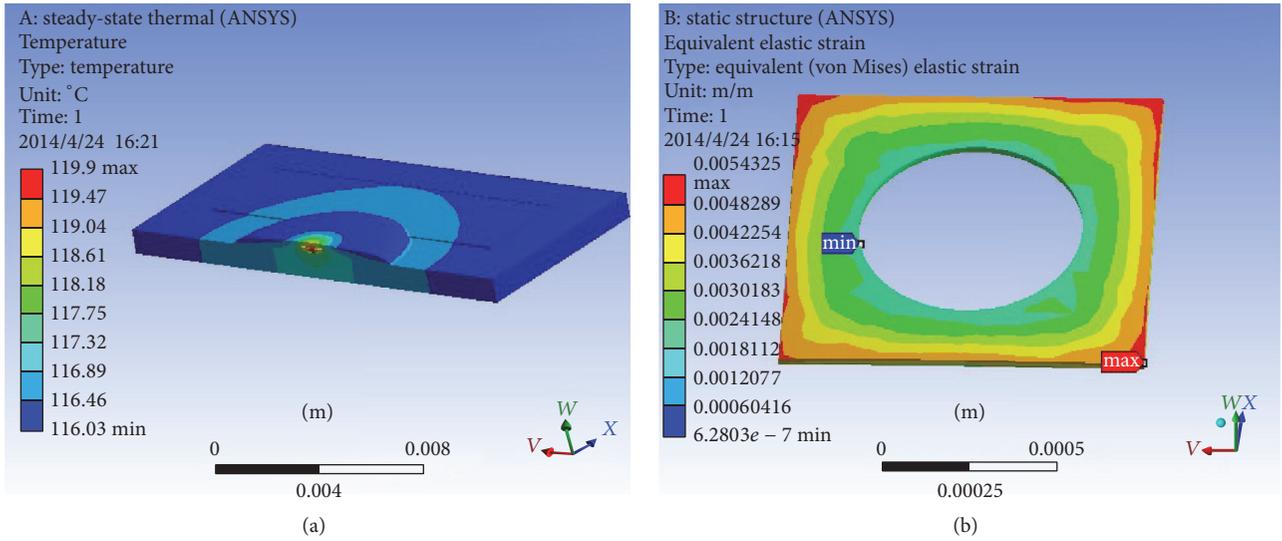


FIGURE 7: (a) The temperature field distribution by finite element simulation and (b) the thermal strain distribution of die-attach layer.

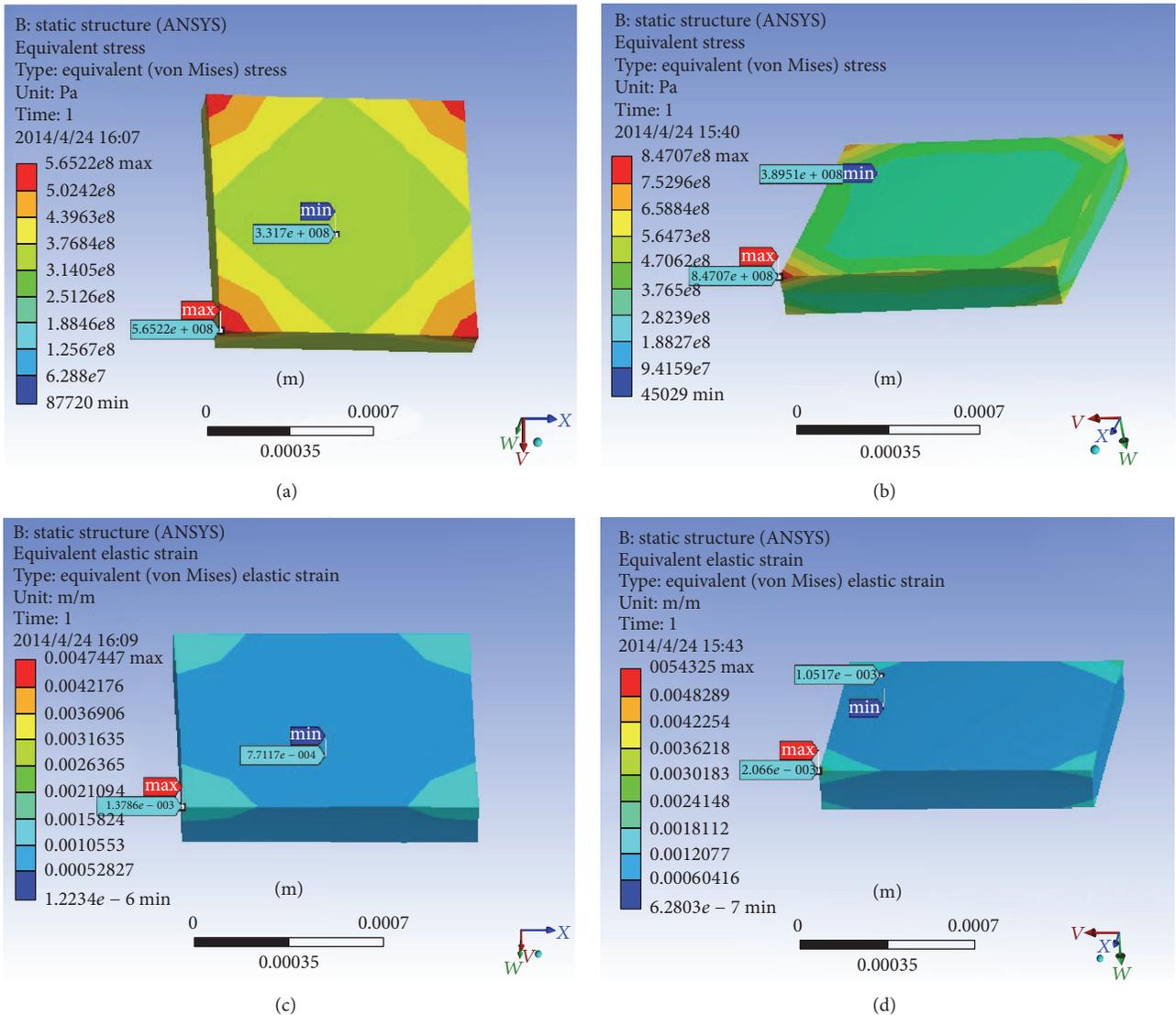


FIGURE 8: The thermal stress and thermal strain distribution of the LED chip with different void fraction in die-attach layer.

0.14% for void-free die-attach layer. The biggest thermal stress and thermal strain of the LED chip were as high as 847.1 MPa and 0.21%, when the void fraction of the die-attach layer increases to 30% as shown in Figures 8(b) and 8(d). It was found that the biggest thermal stress and thermal strain of the LED chip with void-free die-attach layer are smaller than that of the LED chip with much voids in die-attach layer. The LED package with smaller thermal stress and thermal strain will show a relatively higher performance and reliability.

4. Conclusion

This paper investigated the influences of the void fraction in die-attach layer to the thermal and mechanical performances of high-power LED devices. The test results show that thermal resistance of die-attach layer decreases with the increase of void fraction in die-attach layer. With the void fraction in die-attach layer changing from 62.45% to 16.53%, a decrease of thermal resistance of die-attach layer is as much as 1.96°C/W. Finite element simulation results show that the biggest thermal stress and thermal strain of chip with void-free die-attach layer are smaller than that with voids in die-attach layer. So the die-attach quality will show a noticeable effect to the performance of LED modules. The results show that the improvement of the voids fraction will decrease the thermal resistance of die-attach layer, which is an effective method to enhance the thermal and mechanical performance of high-power LED.

Competing Interests

The authors declare that there are no competing interests regarding the publication of this paper.

Acknowledgments

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