

Research Article

Frequency Dependence of C-V Characteristics of MOS Capacitors Containing Nanosized High- κ Ta₂O₅ Dielectrics

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Received 8 December 2016; Revised 24 April 2017; Accepted 3 May 2017; Published 28 May 2017

Academic Editor: Antonio Riveiro

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Capacitance of metal-insulator-Si structures containing high permittivity dielectric exhibits complicated behaviour when voltage and frequency dependencies are studied. From our study on metal (Al, Au, W)-Ta₂O₅/SiO₂-Si structures, we identify serial C-R measurement mode to be more convenient for use than the parallel one usually used in characterization of similar structures. Strong frequency dependence that is not due to real variations in the dielectric permittivity of the layers is observed. Very high capacitance at low frequencies is due to the leakage in Ta₂O₅ layer. We found that the above observation is mainly due to different leakage current mechanisms in the two different layers composing the stack. The effect is highly dependent on the applied voltage, since the leakage currents are strongly nonlinear functions of the electric field in the layers. Additionally, at low frequencies, transition currents influence the measured value of the capacitance. From the capacitance measurements several parameters are extracted, such as capacitance in accumulation, effective dielectric constant, and oxide charges. Extracting parameters of the studied structures by standard methods in the case of high- κ /interfacial layer stacks can lead to substantial errors. Some cases demonstrating these deficiencies of the methods are presented and solutions for obtaining better results are proposed.

1. Introduction

High permittivity dielectrics (high- κ) are nowadays extensively studied as a replacement of silicon dioxide in various microelectronics devices [1–4], like gate dielectrics [5], memory devices [6], and so forth.

Between the high- κ dielectrics tantalum pentoxide (Ta₂O₅) [7] has been identified as very good solution for dynamic random access memories (DRAM) [8]. In this work we specifically study the case of Ta₂O₅.

An unavoidable interfacial layer few nanometers thick (typically between 1 nm and 4 nm), grown between the Si substrate and Ta₂O₅ due to the thermodynamic instability of the Ta₂O₅/Si interface, appears [9, 10]. The situation is similar to most of the other high- κ dielectrics: TiO₂, HfO₂ [11], LaScO₃ [12], GdScO₃ [13], Er₂O₃ [14], and so forth.

Interfacial layer influences the properties of the dielectric film that has to be studied as a stacked layer (high- κ /interfacial layer). We previously developed a comprehensive model for I-V characteristics of Ta₂O₅/SiO₂ structures [15, 16]. In [17] we showed that the frequency dependence of the effective series capacitance of metal-Ta₂O₅/SiO₂-Si structures can be successfully described by a five-element model.

The main aim of this paper is to study the frequency dependence of the effective series capacitance of nanosized dielectrics (10 nm or thinner) and to test the applicability of the model previously developed and applied on thicker films (50 nm) [17]. C-V characteristics for various frequencies were measured both in serial and in parallel measurement mode. The observed differences between them are discussed. Previously [18], we reported preliminary results on the above discussed issues. In [19] we elaborated the issue of determination

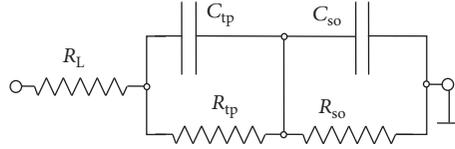


FIGURE 1: Equivalent circuit for metal-Ta₂O₅/SiO₂-Si structures [17].

of interface state densities in metal-dielectric-Si structures containing high- κ dielectrics. The issue of hysteresis-like flat band voltage instabilities in Al/Ta₂O₅-SiO₂/Si structures has been studied in detail in [19]. It has been shown that under defined conditions repeatable patterns of C - V characteristics are obtained. Thus obtained C - V characteristics can be effectively used in determination of equivalent oxide thickness and fast interface state densities using the C - V curves obtained when sweeping the voltage from negative to positive bias. In the present work we study in detail the issue of analysis of capacitance measurement data obtained in serial and parallel mode for the case of metal (Al, Au, W)-Ta₂O₅/SiO₂-Si structures.

2. Fabrication of the Samples

The samples studied here were fabricated on p-type (1 0 0) 15 Ω cm Si substrates. After chemical cleaning, a Ta film was deposited on Si by sputtering of a Ta target in Ar atmosphere. Subsequently, the Ta film was oxidized in dry O₂ at 600°C. More details on the sample preparation can be found in [8]. The above oxidation temperature was chosen so as to be low enough to minimize the substrate oxidation in order to prevent the formation of tantalum silicides. The thickness of thus obtained Ta₂O₅ films and the refractive index were measured ellipsometrically ($\lambda = 632.8$ nm). Layers with a thickness of about 10 nm were used in this study. The refractive index was found to be 2.1. The test structures were metal-insulator-silicon capacitors with three different metal gates: Al, W, and Au. The gate areas (S) were $1.96 \cdot 10^{-3}$ cm² for Au and $2.5 \cdot 10^{-3}$ cm² for Al and W. W layers were sputtered in Ar to a thickness of 300 nm under the following conditions: power density of 3.1 W cm⁻² and gas pressure 3 Pa. Al and Au electrodes were obtained by thermal evaporation using a conventional technique.

In the first part of the study, we measured the capacitance in C_s - R_s (serial) mode in the frequency range from 100 Hz to 1 MHz, with the use of a HP 4284 A LCR-meter. The measurements were done with substrates in accumulation with an ac signal level of 24 mV at a gate bias ranging from -2 V to -3 V. For the second part of the study, high-frequency C - V measurements, both in serial and parallel (C_p - R_p) mode, were performed at frequencies ranging from 3 kHz to 1 MHz, in the voltage range from -3 V through +1 V, starting from the left (the most negative gate voltage) and ending at the right (maximum positive voltage). Repeated measurements under identical conditions gave practically the same results, showing that no substantial wearout took place during the measurements.

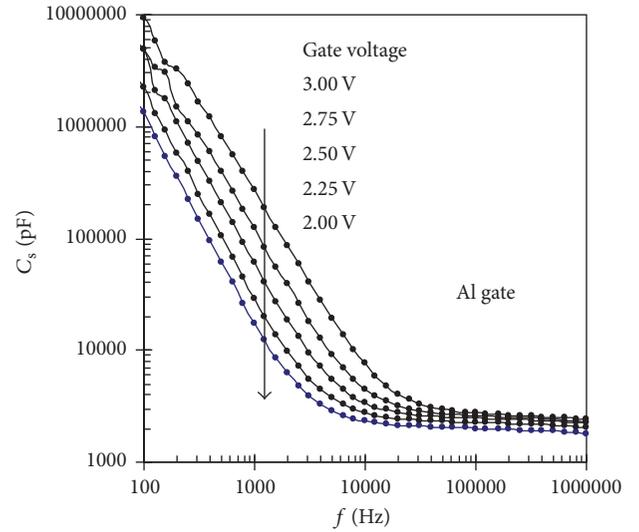


FIGURE 2: C_s - f characteristics in the case of an Al gate.

3. Frequency Dependence of the Effective Series Capacitance

First, we studied the dependence of the effective serial resistance of metal-Ta₂O₅/SiO₂-Si structures on the frequency, at a given gate bias voltage. Model developed in [17] was used to explain the obtained results. More details on the model and its application can be found in the same work. The equivalent circuit composed of five elements [17] is shown in Figure 1. C_{so} and the R_{so} are capacitance and parallel resistance of the interfacial silicon oxide layer, while C_{tp} and R_{tp} are capacitance and parallel resistance of the bulk tantalum oxide layer. Capacitances in the model are constant values, while the resistances depend on the bias voltage. R_L is the serial (load) resistance of the structure.

Effective serial capacitance of the considered five-element circuit is expressed by [17]

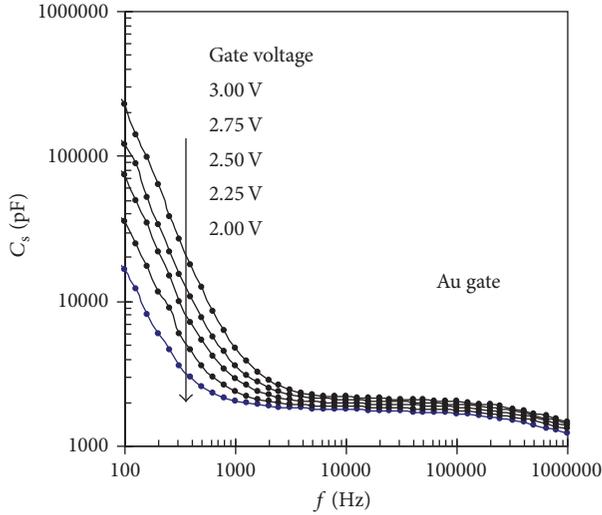
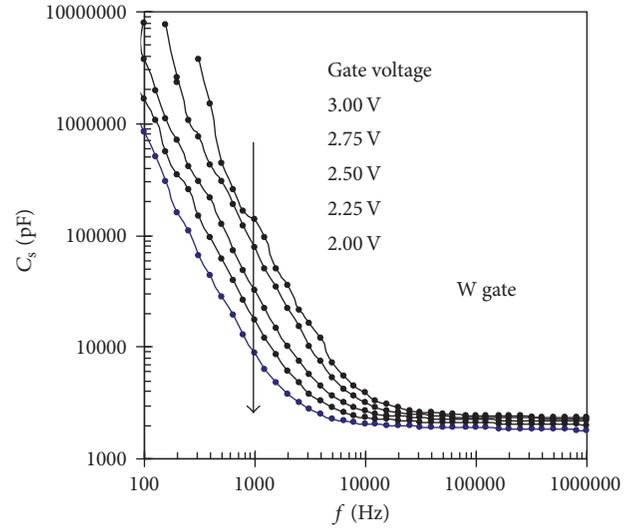
$$C_s(\omega) = \left(\frac{1/C_{tp}}{1 + 1/(\omega C_{tp} R_{tp})^2} + \frac{1/C_{so}}{1 + 1/(\omega C_{so} R_{so})^2} \right)^{-1}, \quad (1)$$

where $\omega = 2\pi f$ is the angular frequency of the measurement signal (f is the signal frequency).

In Figure 2 the experimental results for the case of an Al gate structure are shown. Substantial increase of three

TABLE 1: Parameters used in the theoretical calculations shown in Figure 4.

Gate	R_L (Ω)	R_{tp} ($k\Omega$)	R_{so} ($k\Omega$)	C_{tp} (nF)	C_{so} (nF)
Al	160	6	7.0	9.8	3.1
W	160	6	7.5	11.0	2.9
Au	200	60	70	7.9	2.3

FIGURE 3: C_s - f characteristics in the case of an Au gate.FIGURE 4: C_s - f characteristics in the case of a W gate.

orders of magnitude at 100 Hz is observed compared to high frequencies (50 kHz to 1 MHz range).

In Figure 3 the experimental results for the case of an Au gate structure are shown. Increase of two orders of magnitude at 100 Hz is observed compared to high frequencies. The increase is more important at higher gate voltages, attaining higher values at low frequencies and influencing the capacitance at higher frequencies.

In Figure 4 the experimental results for the case of a W gate structure are shown. Increase of three orders of magnitude at 100 Hz is observed compared to high frequencies (50 kHz to 1 MHz). In all three cases considered here, the increase of the capacitance is more important at higher gate voltages, attaining higher values at low frequencies and influencing the capacitance at higher frequencies.

In order to test the validity of the model, in Figure 5, we present the comparison of the experimental with theoretical results obtained using the five-element model. Only results for gate voltage -2.5 V are shown; other results being quite similar to the results presented here. Parameters used in the calculations are given in Table 1.

It is seen that in the case of Au gate leakage current is almost two orders of magnitude lower than these for other two metals. Since the differences between the capacitances of both the Ta_2O_5 and the SiO_2 layers are not substantial, it can be concluded that the main origin of the low leakage current for the Au gate is not related to differences in the thicknesses of the layers, but to lower density of defects, manifested in substantially higher resistances in the case of Au gate both of

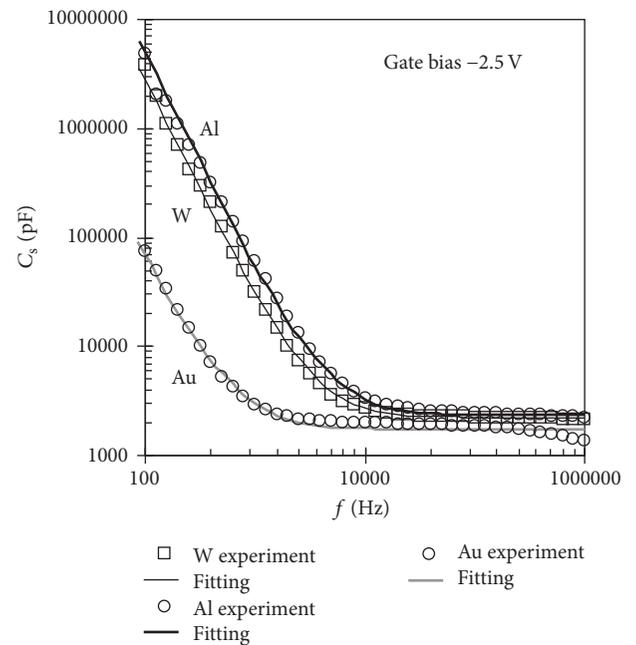


FIGURE 5: Comparison of experimental and theoretical results for effective series capacitances.

the Ta_2O_5 and the SiO_2 layers compared to the case of W and Al gates.

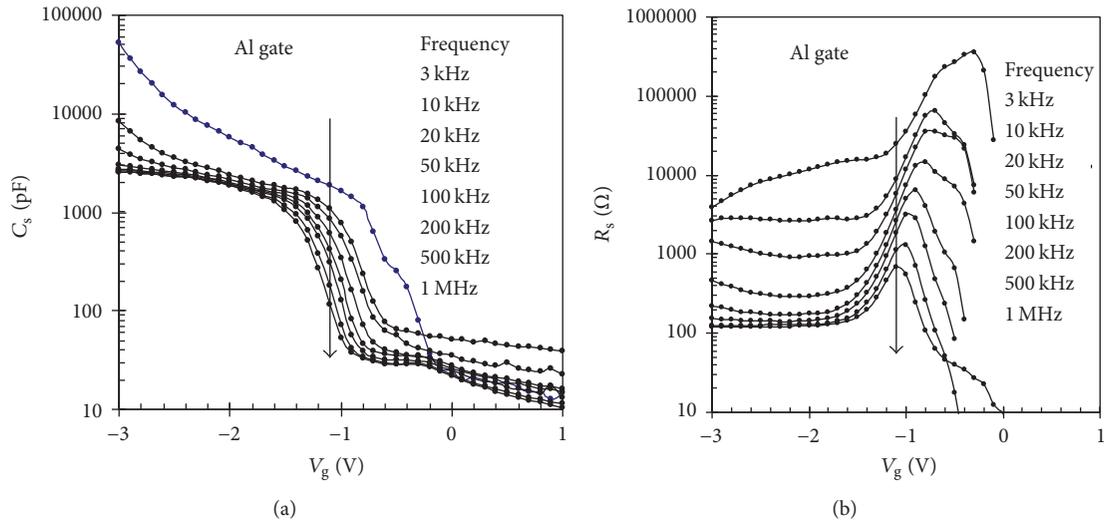


FIGURE 6: C_s - V and R_s - V characteristics for an Al gate.

4. Frequency Dependence of C - V Characteristics

The analysis done in previous section is applicable for C - f characteristics. For C - V characteristics it cannot be applied as is, since the parameters of model depend on the applied voltage. Therefore further development of characterization method is to be done. In this section we study the main aspects of the influence of leakage currents on measured C - V characteristics. The measurements of C - V characteristics are mainly done in the parallel mode. Above choice has been made assuming that the structure in accumulation can be described by a two-element model: metal-insulator-silicon capacitor (C_p) with a parallel resistance (R_p). Such an approach is justified for silicon dioxide insulating layers with low leakage. In the case of leaky and high- κ dielectrics, measurements in parallel mode have many disadvantages. A three-element model, including an additional serial resistance, was used to describe frequency dependence of the measured capacitance [20, 21]. In the case of high leakage thin dielectrics, it was observed that the C - V characteristics measured at higher frequencies are unrealistic; the measured capacitance decreases with the frequency and the gate voltage. In order to correct this deficiency, it was proposed to correct the C - V characteristics, by using the results of the measurements done at two different frequencies and the expressions obtained with the three-element model [22]. Using that method, more realistic results are obtained. The method was further improved by adding serial impedance [23]. Nevertheless, the method is based on the assumption that the difference between the C - V characteristics is due only to the leakage currents. Indeed, as we showed in [24], the flat band voltages are different for different frequencies (50 kHz, 100 kHz, and 1 MHz). The variations of the flat band voltage with frequency can be in great part accounted for by the effect of serial resistance (R_L). Before proceeding to

the method of correction of measured curves for the effect of serial resistance, appropriate choice of the measurement mode for high-frequency C - V characteristics is to be found. Therefore, as a crucial step in the procedure of MOS characterization, the best single frequency measurement method has to be adopted for obtaining correct high-frequency C - V characteristics. Further we shall show and discuss the results for C - V characteristics obtained at various frequencies both in serial and in parallel mode.

In Figure 6 the experimental results for the serial capacitance and serial resistance in the case of an Al gate structure are shown. It is seen that for high frequencies (50 kHz to 1 MHz), capacitance in accumulation at negative voltages higher than -2 V practically does not depend on the frequency. Therefore, the effect of the leakage does not influence the measured capacitances in the considered frequency range. A systematic shift to the left of the C - V curves with frequency is observed. It can not be explained as an artefact due to the leakage but appears to be connected with some real effects of oxide charge on the capacitance and the effect of serial resistance (R_L). In order to explain these effects, further investigations are required; they remain out of the scope of this study.

In inversion, at gate positively biased ($V_g > 0$), substantial decrease of the capacitance with increasing gate voltage is observed (Figure 6(a)). It can be explained by deep depletion resulting from exhausting of minority carriers (electrons) due to their tunnelling injection occurring at positive gate voltages [15]. In I - V characteristics this exhausting of minority carriers results in saturation of leakage currents [16].

A peak in the effective serial resistance is observed for all frequencies from 3 kHz to 1 MHz. Gradual shift to the left is observed as for the capacitances. Peak R_s values can be used for calculation of conductance and subsequently determination of interface state densities by the method using single G/ω - V curve measured at a given frequency ω [19].

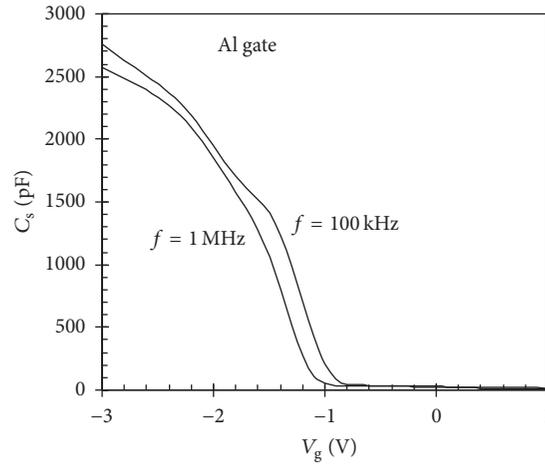


FIGURE 7: C - V characteristics at 100 kHz and 1 MHz, obtained in serial measurement mode for an Al gate.

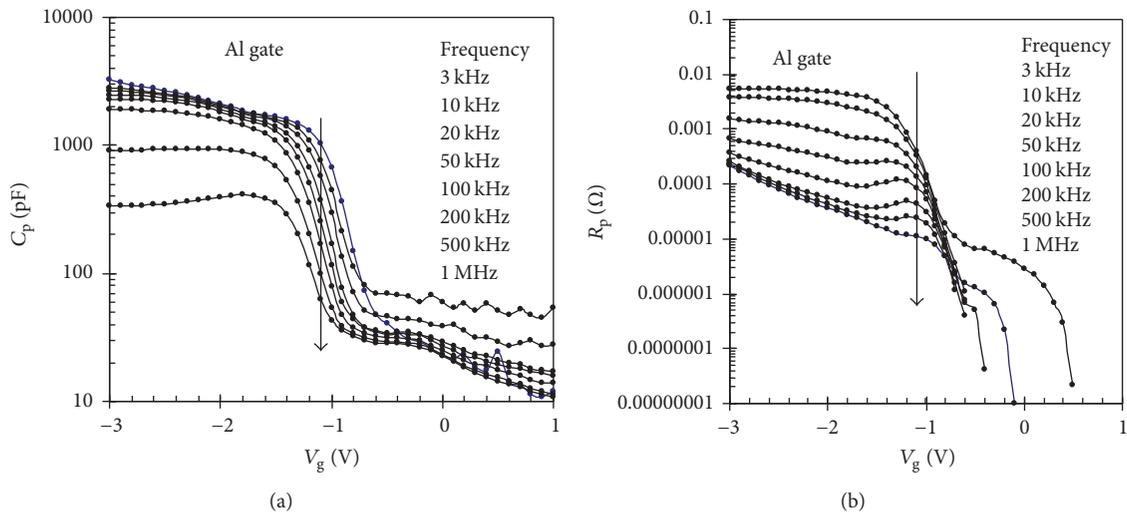


FIGURE 8: C_p - V and R_p - V characteristics for an Al gate.

In addition, the entire curves can be used for reliable determination of densities and energy positions of interface traps.

In Figure 7 the C - V characteristics obtained in serial measurement mode for two frequencies (100 kHz and 1 MHz, typically used for high-frequency C - V measurements) in a linear scale are shown. It is seen that the differences are smaller than 10%.

In Figure 8 the experimental results for the parallel capacitance and parallel resistance in the case of an Al gate structure are shown. It is seen that for high frequencies capacitance decreases for two orders of magnitude when the frequency increases from 50 kHz to 1 MHz. Therefore, the effect of the leakage influences critically the measured capacitances in the considered frequency range. A systematic shift to the left of the C - V curves with frequency is observed as in the case of serial measurement mode. Peaks in R - V curves are observed, being much less pronounced than for the serial mode.

Contrary to the case of a serial resistance, the parallel resistance decreases an order of magnitude when the frequency increases from 100 kHz to 1 MHz (Figure 8(a)). In Figure 9 the C - V characteristics for serial and parallel mode are compared for 100 kHz (Figure 9(a)) and 1 MHz. Even if the difference between the capacitance values in the case of frequency 100 kHz is not high, the shape substantially differ in accumulation region. At 1 MHz (Figure 9(b)) there are enormous differences between the curves.

Particular attention is to be paid to the shape of the curves C_p - V at highest frequencies. At 1 MHz (Figure 8(a)) it decreases from -1.5 V to -3 V instead of increasing. Therefore, the part in accumulation can not be used for further analysis, such as determination of interface states densities. At 100 kHz the curve looks much better, going to saturation at -3 V. However, this is a misleading fact. Namely, at -3 V one can not expect reaching saturation, since voltages of about -5 V are required for this. At such high voltages important wearout occurs, and hence it is not possible to

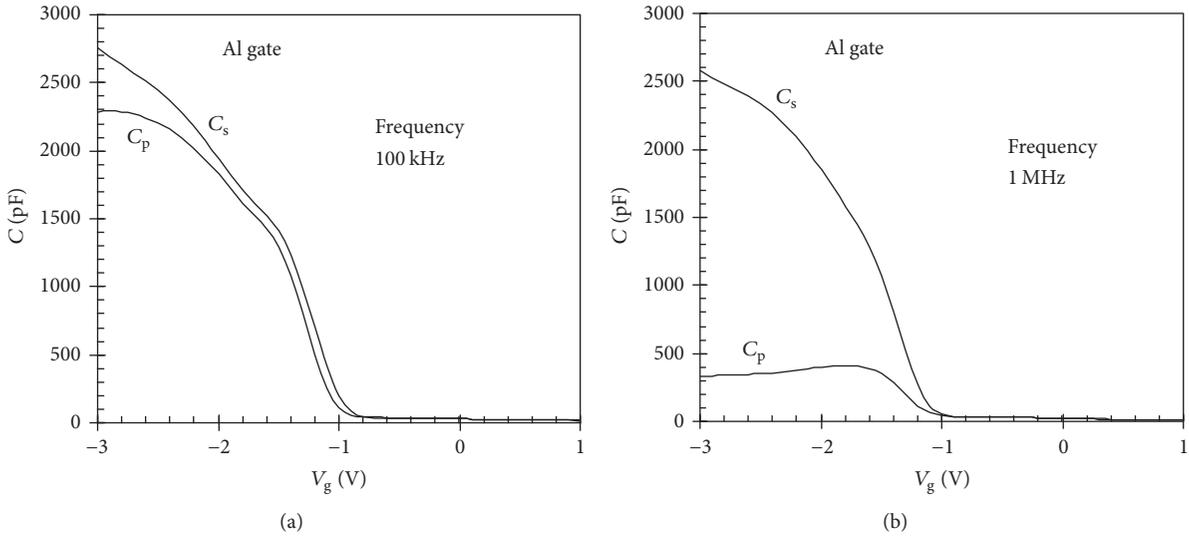


FIGURE 9: Comparison of C_s - V with C_p - V at two frequencies: 100 kHz (a) and 1 MHz (b) in the case of an Al gate.

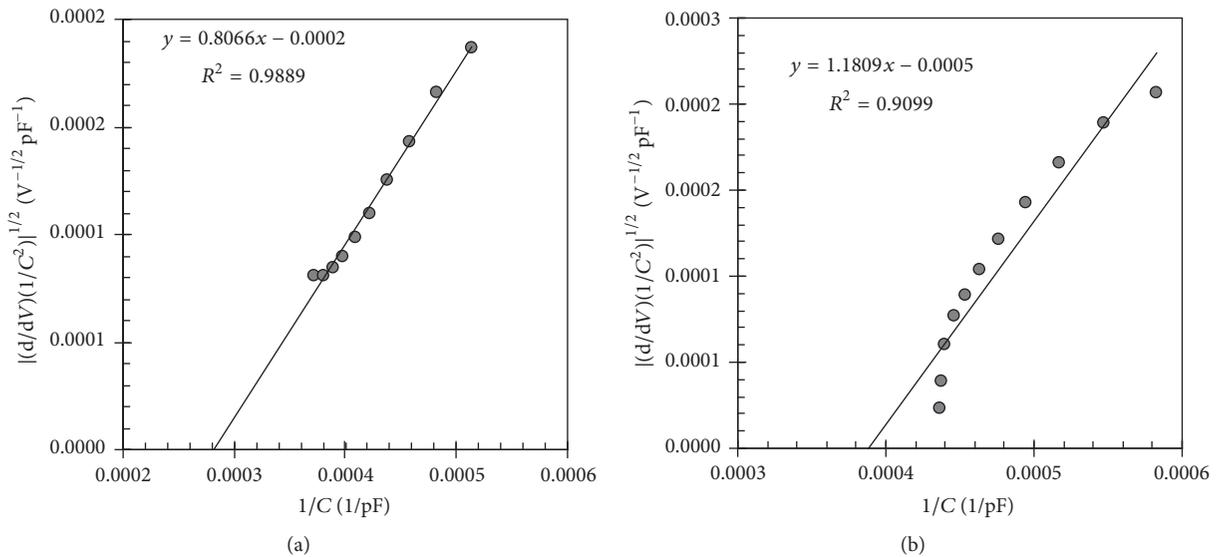


FIGURE 10: $d(1/C^2)/dV$ versus $1/C$ plot for 100 kHz for C_s (a) and C_p (b) in the case of an Al gate.

measure directly saturated capacitance. The observed flat part on the left is due to the compensation of the real increase of the capacitance with the decrease of the effective parallel capacitance due to the increase of the leakage (decrease of the parallel capacitances).

Above statement can be further supported by the analysis of the part of C - V curves in accumulation using the characterization method for extracting data on high- κ dielectrics proposed by Kar et al. [25]. If plotting $d(1/C^2)/dV$ versus $1/C$, straight line is to be obtained. As is seen from Figure 10, this is valid for C_s (a) but not for C_p (b). Therefore, measurements in serial mode can be used for further extraction of parameters, but not in parallel mode.

In Figure 11 the experimental results for serial capacitance and serial resistance in the case of an Au gate structure are shown. Similar results as in the case of Al gate are obtained.

In Figure 12 the experimental results for the parallel capacitance and parallel resistance in the case of an Au gate structure are shown. It is seen that for high frequencies capacitance decreases for an order of magnitude when the frequency increases from 50 kHz to 1 MHz. Therefore, the effect of the leakage influences less the measured capacitances in the considered frequency range than in the case of Al gates. A systematic shift to the left of the C - V curves with frequency is observed as in the case of serial measurement mode. Peaks in R - V curves are observed, being much more pronounced

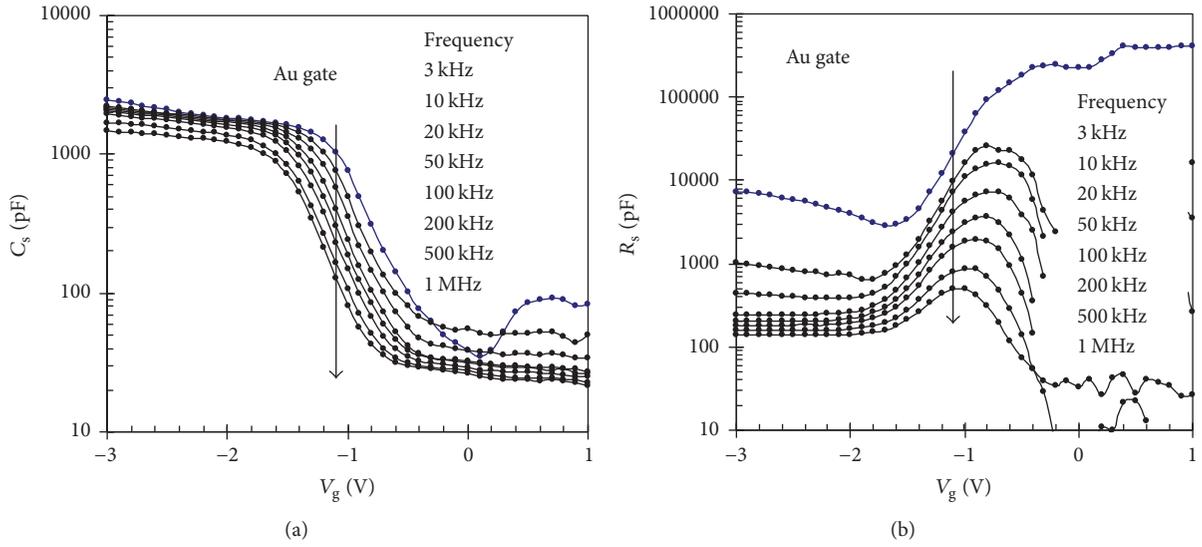


FIGURE 11: C_s - V and R_s - V characteristics for an Au gate.

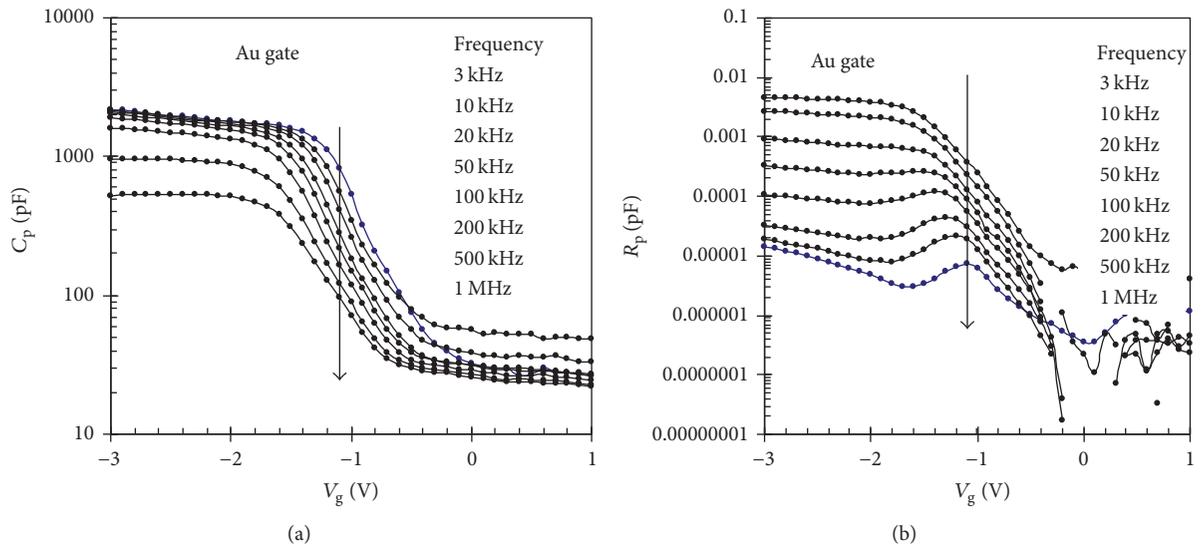


FIGURE 12: C_p - V and R_p - V characteristics for an Au gate.

than in the case of an Al gate. The differences between the results for Al and Au gates can be explained by lower leakage in the case of Au gates. This is in accordance with the values of the parallel resistances extracted from C_s - f measurements (Table 1).

In Figure 13 C_s - V curves are compared to C_p - V curves for $f = 500$ kHz. The frequency $f = 500$ kHz was so chosen because when making simple visual inspection, C_p - V curve looks like a curve for MOS capacitors containing low leakage dielectric, exhibiting clear saturation of the capacitance towards the strong accumulation. Even if the C_p - V curve seems to be rather good, in the $d(1/C^2)/dV$ versus $1/C$ plot only for C_s a good straight line is obtained (Figure 14(a)) and

not for C_p (Figure 14(b)). Nevertheless, the deviation from a straight line is smaller than in the case of an Al gate, due to lower leakage in the case of Au.

In Figure 15 the experimental results for serial capacitance and serial resistance in the case of a W gate structure are shown. Similar results as in the case of Al gate are obtained.

In Figure 16 the experimental results for the parallel capacitance and parallel resistance in the case of a W gate structure are shown. Results similar to those obtained for Al and Au gates are obtained for a W gate.

Above is also valid for the comparison of the C_s - V with C_p - V curves (Figure 17) and the $d(1/C^2)/dV$ versus $1/C$ plot (Figure 18). Therefore, the peculiarities of the C - V

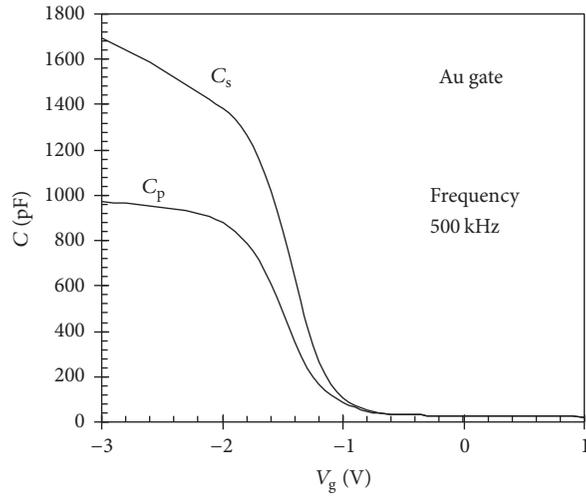


FIGURE 13: Comparison of C_s - V with C_p - V at 500 kHz in the case of an Au gate.

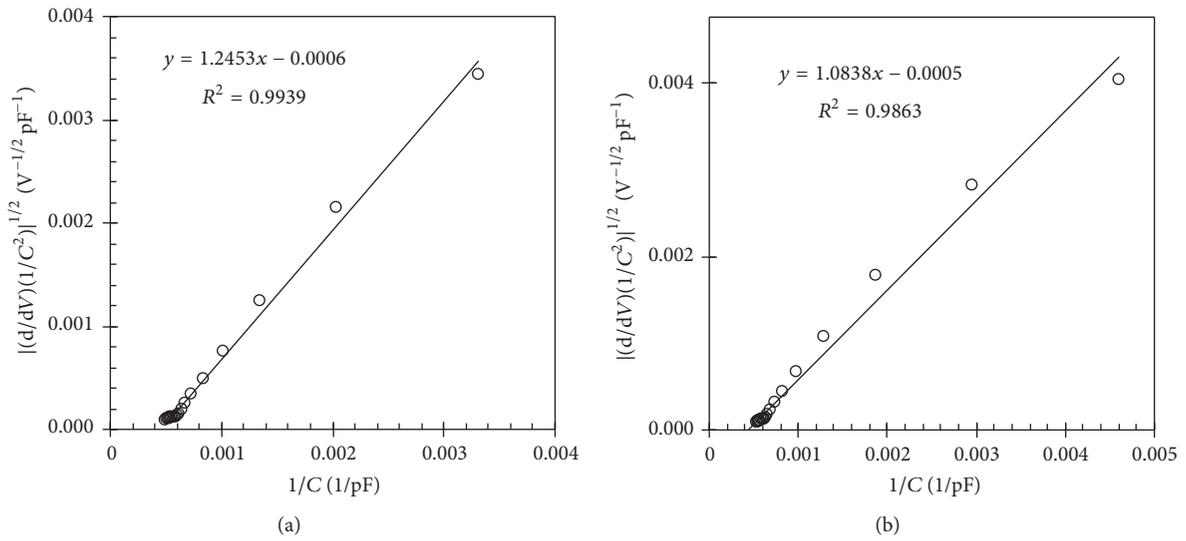


FIGURE 14: $d(1/C^2)/dV$ versus $1/C$ plot for 100 kHz for C_s (a) and C_p (b) in the case of an Au gate.

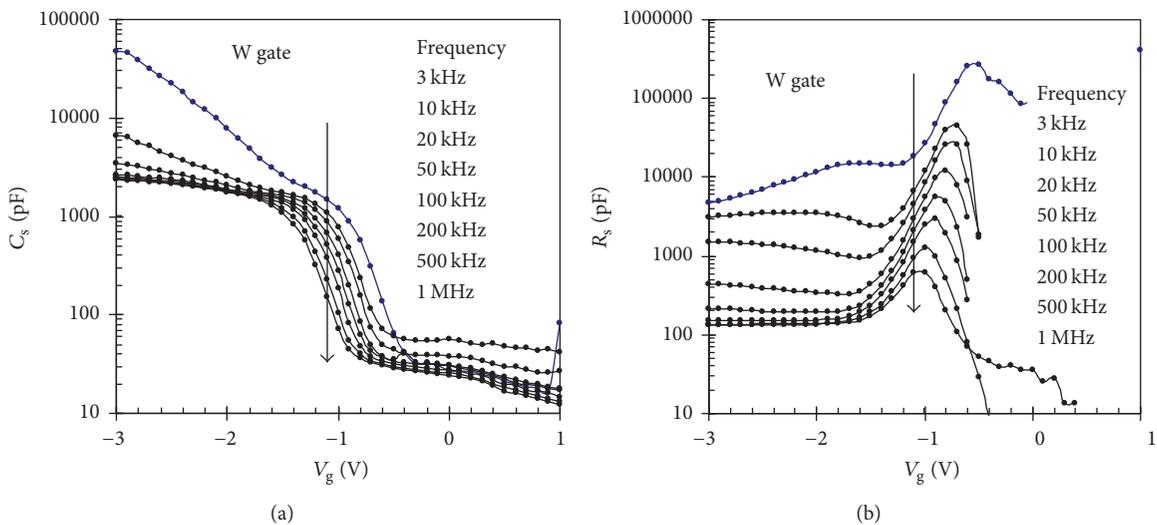


FIGURE 15: C_s - V and R_s - V characteristics for a W gate.

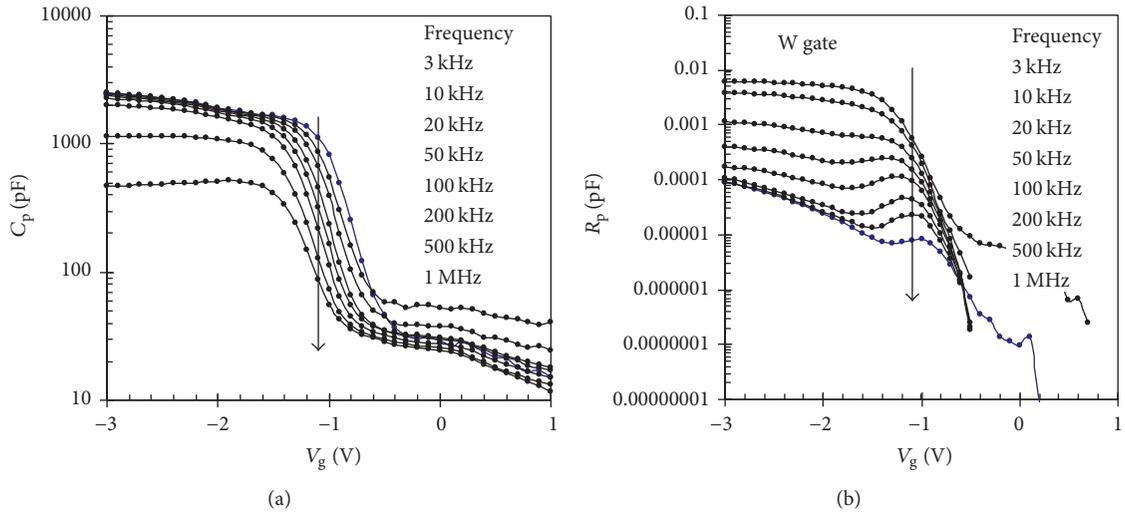


FIGURE 16: C_p - V and R_p - V characteristics for a W gate.

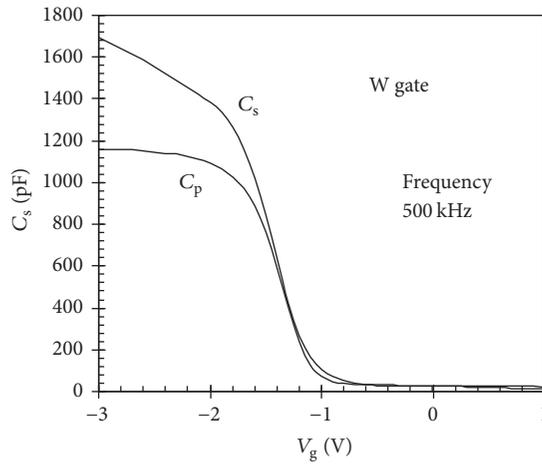


FIGURE 17: Comparison of C_s - V with C_p - V at 500 kHz in the case of a W gate.

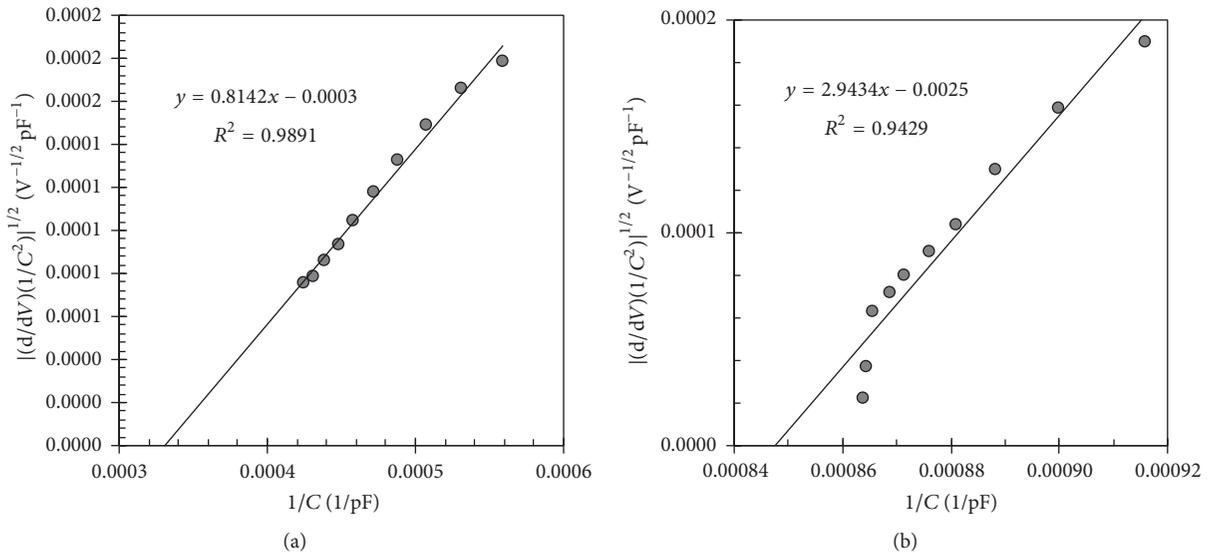


FIGURE 18: $d(1/C^2)/dV$ versus $1/C$ plot for 500 kHz for C_s (a) and C_p (b) in the case of a W gate.

TABLE 2: Equivalent oxide thickness (d_{eq}), flat band voltage (V_{fb}) obtained from C - V curves measured at 100 kHz, ideal flat band voltage ($V_{fb,id}$), and determined oxide charge (Q_{ox}).

Gate	d_{eq} (nm)	V_{fb} (V)	$V_{fb,id}$ (V)	Q_{ox} (10^{12} cm^{-2})
Al	2.27	-0.91	-0.59	2.8
W	2.71	-0.86	-0.29	4.6
Au	3.44	-0.78	0.18	6.0

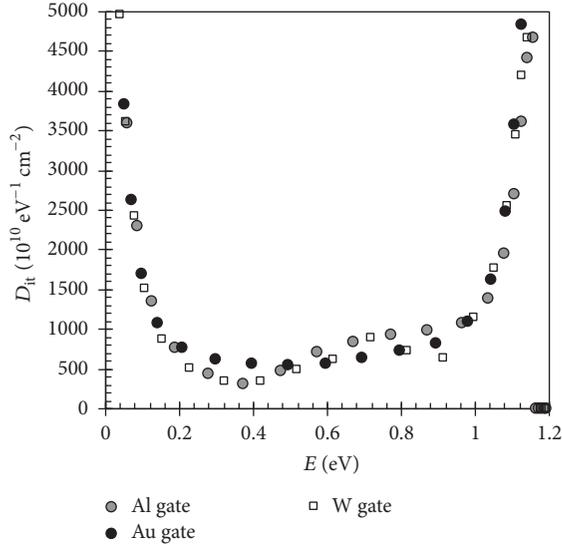


FIGURE 19: Interface state density versus energy over the entire Si bandgap.

measurements discussed above seem to be valid for different gate metals. Somehow different result is obtained in the case of lowest frequency in the considered range (3 kHz) for Al gate. This is a case where the gate is reactive with Ta_2O_5 [26] and the density of defects contributing to the leakage attains high values. Therefore, except for materials with high defect density, results obtained here are applicable in general. In addition, while limiting to frequencies in the range from 10 kHz to 1 MHz, even if using reactive gate metals, predictable results are obtained and the proposed method of characterization in this work is expected to provide highly reliable results.

For illustration, values of equivalent oxide thickness (d_{eq}), flat band voltage (V_{fb}), ideal flat band voltage ($V_{fb,id}$), and oxide charge (Q_{ox}), obtained from C - V curves measured at 100 kHz, using standard methods, are shown in Table 2. It is seen that oxide charges in all cases are comparable. Substantial difference in the equivalent oxide thickness is observed. The lowest value of 2.27 nm is obtained for Al gate and is attributed to the known reactivity of Al with Ta_2O_5 [26].

C - V characteristics obtained in serial mode can be used for effective determination of interface state densities (D_{it}). In Figure 19 the results obtained by standard single curve high-frequency method (Terman method) from characteristics

measured at 100 kHz are shown. No marked differences for different gates are obtained, indicating that the SiO_2 -Si interface properties strongly are not affected by the gate.

5. Conclusions

Capacitance of the metal-high- κ -semiconductor structures demonstrates complicated behaviour with voltage and frequency. Based on our studies on metal (Al, Au, W)- $\text{Ta}_2\text{O}_5/\text{SiO}_2$ -Si structures described as well as on the experience from various other metal-high- κ -semiconductor structures, we found that serial C - R measurement mode is more convenient for characterization of such structures than the dominantly used parallel one. Strong frequency dependence that is not due to real variations in the dielectric permittivity of the layers is observed. Very high apparent capacitance at low frequencies is described to be due to the leakage in Ta_2O_5 layer. We found that the above observation is mainly due to different leakage current mechanisms in the two different layers in the dielectric stack. The effect is highly dependent on the applied voltage, since the leakage currents rapidly grow with the applied electric fields in the layers. Additionally, at low frequencies, the measured value of the capacitance is influenced by transition currents of various origins.

From the capacitance measurements several parameters of the structures are extracted: capacitance in accumulation, effective dielectric constant, oxide charges, and interface state densities. Extracting parameters of the studied structures by standard methods without proper modification in the case of high- κ /interfacial layer stacks can lead to substantial errors that can make in many cases the results unusable or misleading. Here, described effects, as the one with the effects found by other authors for nanosized and ultra-thin dielectric layers, are to be used in the analysis. The applicability of all standard methods is to be reconsidered in view of these new effects. Some of the most important ceases are presented in this work.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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