Research Article

Research of p - i - n Junctions Based on $4H$ -SiC Fabricated by Low-Temperature Diffusion of Boron

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Novel method of boron diffusion at low temperatures between 1150 and 1300°C is used for the formation of both p - i SiC junction and i -region in one technological process. As the junction formation conditions in this method are essentially different from those in the conventional diffusion (low temperatures and process of diffusion are accompanied by formation of structure defects), it is of special interest to identify advantages and disadvantages of a new method of diffusion. Developed SiC p - i - n junction diodes have fast switching time, and the duration of the reverse recovery current is less than 10 ns with a breakdown voltage of 120–140 V. Fabricated diodes possess capability to operate at temperatures up to 300°C. As the temperature of diffusion process is lower than the melting temperature of silicon, this new technology allows fabrication of diodes on the base of SiC/Si epitaxial structures.

1. Introduction

Silicon carbide- (SiC-) based devices have number of advantages over traditional silicon and gallium arsenide analogues. One of such advantages is high operating temperature of SiC devices [1–3], which makes this material very promising for power and extreme electronics [2–7]. Another important feature of SiC is high saturation velocity of electrons [8], which enables SiC-based devices to operate at high frequencies (RF and microwave). An important characteristic of diodes for power and pulse application is the switching time. For SiC diode with an area of $100 \times 100 \mu\text{m}^2$, switching time (t_s) is ~ 20 ns [9] (silicon diodes have $t_s \sim 100$ ns [10]). Previously, it has been shown in [11] that the base region of SiC diodes doped by aluminum has a deep level with ionization energy $E_C - 1.45$ eV and a trapping level with ionization energy $E_C - 0.16$ eV, which is observed due to nitrogen impurity. Capture processes and thermal activation of electrons associated with these levels can greatly influence duration of current relaxation of SiC p - n junction. Currently, power diodes based on silicon carbide made by diffusion technology have maximal

breakdown voltage ~ 700 V for $4H$ polytype and ~ 1000 V for the $6H$ polytype of silicon carbide [12, 13].

Previously, it has been shown that to fabricate diodes with high breakdown voltage (more than 2000 V), highly resistive i -region of SiC p - i - n diodes needs to be created by epitaxial growth of thin SiC layer (free from micropipe defects) [14–16]. Afterwards (second technological step), p -region of SiC p - i - n diodes is formed by thermal diffusion at temperatures $> 2050^\circ\text{C}$ or ion implantation of SiC by aluminum [17, 18] and boron [17]. It is worth mentioning that heavily doped SiC crystal fabricated by ion implantation (with concentration of impurities up to 10^{19} cm^{-3}) should be annealed at a temperature of $\sim 1800^\circ\text{C}$ to remove the defects [3, 18]. Extremely high-temperature processing ($> 2050^\circ\text{C}$) needed during thermal diffusion [19–21] or after ion implantation [3, 18] may increase the production cost. Very high blocking voltage over 26.9 kV for such structures with epilayer (n^+ - n^- epilayer/ n^+ epilayer/ n^+ substrate) has been achieved in [21].

The most important process steps in SiC devices manufacturing are formation of p - n junction and low-resistance ohmic contact. The p -region of SiC diodes can

be conventionally formed by thermal diffusion of shallow impurity (at $T > 2000^\circ\text{C}$) or ion implantation of aluminum in SiC with concentrations up to 10^{19} cm^{-3} [9, 22]. For layers heavily doped by ion implantation, it is necessary to perform thermal treatment (at $T > 1600^\circ\text{C}$) to anneal radiation defects [3].

The materials used as impurity sources during diffusion are as follows: diborane B_2H_6 gas [23] (diffusion from gas phase) and wafer of boron nitride [24] or borosilicate glass (diffusion from solid state). Conventional diffusion processes are usually carried out in a vacuum or inert atmosphere. Extremely high temperatures (over 2000°C) are necessary during conventional diffusion process to form p - n SiC [19–21].

Low-temperature (900 – 950°C) diffusion of boron and phosphorus in single-crystal silicon carbide was studied in [25, 26]. Obtained high concentrations of up to 10^{21} cm^{-3} are explained by prevailing role of silicon vacancies in the process of diffusion of these impurities [27].

The mechanism of thermal diffusion in silicon carbide is quite complex as the crystal has two sublattices (silicon and carbon). Previously, Gao et al. and Lebedev [20, 28] studied boron diffusion on $6H$ -SiC in the temperature range between 2000 and 2200°C and have demonstrated that there are two types of boron solubility depending on the position of boron atoms in the carbon or silicon sublattice. According to Girka and Mokhov [29], the concentration of carbon vacancies at these temperatures in silicon carbide is very high (from 3×10^{17} to $5 \times 10^{17}\text{ cm}^{-3}$) and, according to Gao et al., carbon vacancies exert a strong influence on the diffusion of boron. In the silicon sublattice, the boron solubility ($\sim 6 \times 10^{19}$ to $9 \times 10^{19}\text{ cm}^{-3}$) is approximately 10 times higher than that in the carbon sublattice (from 1×10^{18} to $10 \times 10^{18}\text{ cm}^{-3}$) [30].

Several factors can influence thermal diffusion process such as surface conditions, chemical treatments, concentration of defects in carbon, and silicon sublattices. That is why conventional thermal diffusion is regarded as an old and unstable technology for fabricating p - n SiC junction.

This paper describes a novel method to diffuse boron at temperatures between 1150 and 1300°C that has been used for formation of p - i junction and i -region in one technological process. Characteristics of fabricated p - i - n $4H$ -SiC structures are presented. Diffusion temperature is lower than the melting temperature of silicon, and this new technology can be used to fabricate diodes based on the SiC/Si epitaxial structures. As the conditions of junction formation in this method are essentially different from those in the conventional diffusion (low temperatures and process of diffusion are accompanied by formation of structure defects), it is interesting to identify the advantages and disadvantages of a new method of diffusion.

2. Experimental

Single-crystal sample of silicon carbide has been grown at Cree, Inc., by physical vapor transport (PVT) method with a relatively low concentration of growth defects: N dislocations 10^4 cm^{-2} and N micropipes ~ 10 – 10^2 cm^{-2} for $4H$

polytype of n -SiC. Thickness of the sample ($4 \times 4\text{ mm}^2$) is ~ 300 – $600\text{ }\mu\text{m}$, and specific resistance is between 3.6 and $20\text{ }\Omega\cdot\text{cm}$.

The samples have been etching in KOH solution with UV light stimulation. Unlike to reactive ion etching, the UV light stimulated etching does not create defects and allows fabrication of a smooth soft surface [31].

Diffusion of boron in $4H$ -SiC has been performed at different temperatures between 1150 and 1300°C by the novel low-temperature diffusion method described in [31–39]. Borosilicate thin film on the surface of SiC has been used as a source for boron atoms.

The diffusion process has been carried out at inert atmosphere (to create a flow of vacancies of Si and C from the crystal surface into the bulk of the sample [38]). Increased concentration of Si and C vacancies allows increase of the diffusion constant and solubility of impurity up to 10^{20} cm^{-3} (depth of p -area reaches up to 2 – $3\text{ }\mu\text{m}$) [37, 38]. Low disintegration of SiC surface is expected, and the diffusion temperature in our method is between 1150 and 1300°C , which is lower compared to the conventional diffusion.

It should be noted that, in the works of Bagraev et al. [40, 41] for the formation of ultra-shallow p^+ - n junctions (with depth of 10 nanometers) at low diffusion temperatures of 900°C , the flux of silicon vacancies was created at the SiC-SiO₂ interface. In our case, the flux of V_C carbon and V_{Si} silicon vacancies was created by surface oxidation. Below, we describe briefly the mechanism of formation of V_C and V_{Si} vacancies.

In [42], it is described that, at temperatures 1100 – 1400°C , SiC exhibits two types of oxidation behavior, “active” and “passive,” depending upon the ambient oxygen potential. At high oxygen pressures, “passive” oxidation occurs, wherein a protective film of SiO₂(s) is formed on the surface by the reaction

At low oxygen potentials, severe “active” oxidation occurs due to the formation of gaseous products according to the following reactions:

Active oxidation of SiC occurs only at oxygen pressures lower than $\sim 3 \cdot 10^{-4}\text{ atm}$ at 1400°C . As seen from (2) and (3), surface oxidation of silicon carbide in these conditions leads to production flow of both carbon and silicon vacancies from the surface into the bulk of the crystal (may be mostly of carbon vacancies). Obviously, the vacancy concentration in this case can be much higher as compared with the introduction of vacancies by irradiation.

Our technological experiments show that, during diffusion process, the vacancies of Si and C penetrate into volume deeper than doping impurity. Deep penetration of vacancies leads to formation of i -region. So, in one technological process, both p - and i -regions are formed (Figure 1).

FIGURE 1: Schematic diode structures of p - i - n $4H$ -SiC diode.

Type of conductivity of doped layers and silicon carbide single crystals has been tested by hot probe (thermoprobe) method [43].

Distribution of electrically active impurities in SiC crystal has been measured by spreading resistance method after polishing the samples at an angle of 3° . The distribution of boron in very thin region near surface is obtained by using capacitance-voltage (C - V) measurements of Ni- p -SiC Schottky barriers. These methods allow obtaining of the distribution of electrically active impurities in the crystal, whereas the depth profiling by SIMS gives information on the total content of impurity including impurity atoms in nonactive interstitial sites and in inclusions of secondary phase in crystal.

Current-voltage (I - V) characteristics have been measured by a standard scheme using digital devices. The concentration of shallow impurities has been determined based on the capacitance-voltage (C - V) characteristics [44]. Impedance measurements have been carried out at different frequencies with the amplitude of the AC signal at 20 mV, while permanent bias has also been applied to the structure. Switching time for $4H$ -SiC diode structures has been measured on a special impulse stand [45].

3. Results and Discussions

It is well known that spreading resistance method allows measuring of the distribution of electrically active impurity only. Boron impurity distribution (up to $2\ \mu\text{m}$) for one of the $4H$ -SiC samples measured by spreading resistance method on the angle polished samples is shown in Figure 2. As the diffusion is stimulated by the flow of carbon and silicon vacancies generated on the surface of SiC crystal, the concentration of defects becomes very high near the surface. To study the distribution of boron in the region near the surface (on top of p -region), Ni- p -3C-SiC Schottky barriers have been fabricated and their C - V characteristics have been measured. As one can see in Figure 3, boron diffusion stimulated by the flow of Si and C vacancies shows high solubility of $\sim 10^{20}\ \text{cm}^{-3}$, although this value is practically unreachable by other doping technologies. Ion implantation technology also allows achieving high concentration of impurities such as aluminum. However, to anneal the defects, additional thermal treatment is necessary [3]. Another observed interesting feature is the quasiperiodic distribution

FIGURE 2: Distribution of N_B in $4H$ -SiC crystal after diffusion at 1300°C , measured by spreading resistance method on the angle polished sample [38].

FIGURE 3: Distribution of boron on the top of p -region of 3C-SiC (measured using Ni- p -SiC Schottky barriers) [37].

of boron in some samples. This might be due to the interaction of the diffusing impurities and point defects at high concentration, and it is probably related to some synergistic processes in diffusion.

Based on the experimental data (Figure 2), the following parameters have been defined: diffusion coefficient $D_B \sim 4 \times 10^{-11} - 6 \times 10^{-10}\ \text{cm}^2/\text{s}$, at 1150 – 1300°C and activation energy for diffusion of boron $\epsilon_a \sim 0.8$ – $1.3\ \text{eV}$ [37, 38]. Such a low value of activation energy is usually observed in interstitial diffusion mechanism in semiconductors [46].

Since diffusion takes place under conditions of surface oxidation in air at a fixed temperature, the concentration of vacancies on the surface is determined only by the temperature, and the reproducibility of the process is quite high (50–80%).

Figure 4 shows the current-voltage characteristics of p - i - n junction in $4H$ -SiC (p - n junction area is $6\ \text{mm}^2$).

For samples with a thickness of 300 – $400\ \mu\text{m}$, the breakdown voltage occurs to be within the range of

FIGURE 4: Current-voltage characteristics of p - i - n junction in $4H$ -SiC samples.

FIGURE 5: The dependence of capacitance (a) and the value $1/C^2$ (b) for one of the diodes for reverse voltages, measured at 1 MHz.

120–140 V. Thus, the variation of the breakdown voltage between the samples is no more than 20 V (about 15% of the maximal value). The nonlinearity coefficient (I_{for}/I_{rev}) at 25 V is about 100.

Such a low value of breakdown voltage is mainly due to the influence of dislocations ($N_d \sim 10^4 \text{ cm}^{-2}$) and micropipes ($N_m \sim 10^{-2} \text{ cm}^{-2}$) in the studied SiC crystals. It has been reported previously [47] that, with a screw dislocation concentration of $\sim 10^4 \text{ cm}^{-2}$, maximum breakdown voltage (V_b) between 350 and 400 V can be reached. This breakdown voltage can be improved in several ways, for example, by improving low-temperature diffusion technology, by formation of mesa-structure, and by surface passivation. But to get a significantly high breakdown voltage, it is necessary to use SiC crystal free from micropipes and lower concentration of dislocations.

The growth of forward current is observed at voltage values higher than 10 V. On the ohmic section of the I - V

characteristics, resistance of different junctions is between 15 and 20 Ohms, which indicates the presence of a high-resistance layer between p - and n -regions. This assumption is also confirmed by capacitance measurements: for reverse applied voltage, the capacitance is 9–12 pF (Figure 5). High-resistance layer leads to large losses, and this is a disadvantage of this technology which must be eliminated in the future.

Thickness W of i -layer has been evaluated by the known formula $C = \epsilon \epsilon_0 S / W$ (C is the capacitance of diode, $\epsilon = 9.7$ is the dielectric constant of silicon carbide, ϵ_0 is the electric constant, S is the layer area, and W is the thickness of layer), showing that, in SiC diode samples, $W \sim 39\text{--}40 \mu\text{m}$. According to the well-known expression $L \sim \sqrt{D \cdot t}$ (where L is the diffusion length, D is the diffusion constant, and $t = 30$ minutes is the diffusion time), the diffusion constant must be $D \sim 2 \times 10^{-9} \text{ cm}^2/\text{s}$.

Let us evaluate the diffusion constant of vacancy by using the following expression [48]:

$$D = D_0 \exp\left(-\frac{E_m}{kT}\right), \quad (4)$$

where D_0 is the preexponential factor, E_m is the migration energy, k is the Boltzmann constant, and T is the temperature. According to [48] devoted to atomistic study of intrinsic defect migration, the value D_0 for 3C-SiC is approximately $(1-3) \times 10^{-3} \text{ cm}^2/\text{s}$, and E_m for carbon and silicon vacancies are approximately 4.1 eV and 2.35 eV, respectively. In our nonequilibrium conditions, activation energy of vacancy diffusion has to be near activation energy of boron impurity (0.8–1.3 eV). Then, according to (4), the diffusion constant of vacancy ranges from 10^{-9} to $10^{-8} \text{ cm}^2/\text{s}$, which is in good agreement with the above experimental value $\sim 2 \times 10^{-9} \text{ cm}^2/\text{s}$.

High-resistance region, most likely formed by defects created during the diffusion, has inhomogeneous distribution of the carrier density. The distribution of impurity concentration can be evaluated by using the following expressions [44]:

$$\frac{d(1/C^2)}{dV} = \frac{2}{e\epsilon_s N(W)}, \quad (5)$$

$$W = \frac{\epsilon_s}{C(V)}, \quad (6)$$

where C is the capacitance of junction, ϵ_s is the dielectric constant of the silicon carbide, $N(W)$ is the concentration of impurity at W , and W is the depth of depletion region. As it can be seen from expression (5), the slope of $(1/C^2)$ function is decreased with increasing impurity concentration. According to data presented in Figure 6, the carrier concentration between i -layer and n -area of SiC increases from 10^{16} to $5 \times 10^{17} \text{ cm}^{-3}$ (impurity concentration in the substrate of silicon carbide).

The fabricated structure is layer stack of boron-doped p -region up to $2-3 \mu\text{m}$ with maximal concentration between $10^{19}-10^{21} \text{ cm}^{-3}$ and high resistive i -region which is created by defects related with deep penetration of Si and C vacancies into volume of crystal during diffusion. During the diffusion process, the Si and C vacancies penetrate into volume deeper than doping impurity. Deep penetration of vacancies leads to formation of i -region. Thus, in one technological process, both the p - and i -regions are formed.

Fabricated diode structures have been further studied by impedance measurements at relatively low frequencies 5,000, 10,000, 15,000, and 20,000 Hz (Figure 7). Assuming the parameters of the structures do not change in this frequency range, the data can be used for the development of equivalent circuits and evaluation of capacitance, series resistance, and other parameters of diode. Figure 8 shows the equivalent circuit of our structure (based on the equivalent circuit of the p - i - n diode) and a simplified circuit for the forward and reverse bias [49].

Equivalent circuit for this p - i - n junction consists of diffusion capacity C_{dif} parallel R_{pi} (p - i transition resistance),

FIGURE 6: Distribution of current carrier concentration on the boundary between i - and n -regions of diode defined by C - V measurements at 1 MHz.

series base, and ohmic contact resistance. For reverse voltage, the simplified diagram consists of C_{pi} , R_{pi} , C_{b} and R_{i} of p - i and i - n junctions, as well as high-resistance layer (Figure 8). It should be stated here that the sign i represents high resistance region but not the region with intrinsic conductivity.

For forward bias, the C_{dif} with parallel R_{pi} has conductivity S :

$$S = j\omega C_{\text{dif}} + \frac{1}{R_{\text{pi}}} = \frac{1 + j\omega C_{\text{dif}} R_{\text{pi}}}{R_{\text{pi}}}, \quad (7)$$

where $j\omega C_{\text{dif}}$ is the capacitance conductivity ($j = \sqrt{-1}$ means that capacitance changes the phase of AC). Impedance is

$$Z_1 = \frac{R_{\text{pi}}}{1 + j\omega C_{\text{dif}} R_{\text{pi}}}. \quad (8)$$

Total impedance for direct bias is

$$Z = \frac{R_{\text{pi}}}{1 + j\omega C_{\text{dif}} R_{\text{pi}}} + R_{\text{s}}. \quad (9)$$

Let us transform this expression into the canonical form:

$$Z = \frac{R_{\text{pi}}(1 - j\omega C_{\text{dif}} R_{\text{pi}})}{(1 + j\omega C_{\text{dif}} R_{\text{pi}})(1 - j\omega C_{\text{dif}} R_{\text{pi}})} + R_{\text{s}}, \quad (10)$$

$$Z = \frac{R_{\text{pi}}(1 - j\omega C_{\text{dif}} R_{\text{pi}})}{(1 + \omega^2 C_{\text{dif}}^2 R_{\text{pi}}^2)} + R_{\text{s}}. \quad (11)$$

Module of this impedance is

$$|Z_f| = \frac{\left((\omega C_{\text{dif}} R_{\text{pi}}^2)^2 + (R_{\text{pi}} + R_{\text{s}}(1 + \omega^2 C_{\text{dif}}^2 R_{\text{pi}}^2))^2\right)^{1/2}}{(1 + \omega^2 C_{\text{dif}}^2 R_{\text{pi}}^2)}. \quad (12)$$

For the reverse bias, the same method can be used to obtain an expression

FIGURE 7: Impedance of the diode structure at different frequencies in the direct (a) and reverse (b) voltage (●, 5 kHz; ▲, 10 kHz; ▼, 15 kHz; ■, 20 kHz).

FIGURE 8: Equivalent circuit diagram for a p - n junction with the intermediate layer of high resistance, constructed on the basis of an equivalent circuit pin diode (a) [49] and a simplified scheme for direct (forward bias) and inverse (reverse bias) connection (b).

$$|Z_r| \sim \frac{(R_{pi} + R_i)}{\left((1 - \omega^2 C_{pi} R_{pi} C_i R_i)^2 + (\omega C_{pi} R_{pi})^2 \right)^{3/2}}, \quad (13)$$

where ω is the frequency, C_{dif} is the effective diffusion capacity, R_{pi} is the junction resistance, R_s is the series resistance, and R_i is the resistance to high-resistance layer.

By computer fitting of expression (12) to impedance, the measured diffusion capacity data are evaluated for applied direct voltage 10 V, which occurs to be in the range from 80 pF to 1300 pF at a forward current from 100 μ A to 2.4 mA (Figure 9).

In this case, the value R_s includes both high-resistance layer and resistance of i - n junction which makes the value to vary from 4 to 100 Ohms.

The well-known expression for the diffusion capacity is as follows:

$$C_D = \frac{\tau_p J}{(kT/q)}, \quad (14)$$

where τ_p is the lifetime of minority carriers, J is the forward current through the diode, k is the Boltzmann constant, T is the temperature, and q is the electron charge. The lifetime of minority carriers estimated by using expression (14) is between 10 and 21 ns.

Even though expression (12) cannot be used for computer fitting as fitting parameter R_{pi} is not constant and slightly depends on frequency, the conducted fitting shows that the capacity of a high-resistance layer is between 3 and 12 pF (evaluated from fitting procedure) which is also confirmed by measuring the capacity (Figure 5). Resistance value R_i has varied considerably from 550 to 850 Ohms. The resistivity of the high-resistance layer occurs to be between 90 and 130 Ω -m and depends on the applied voltage and current through the structure.

This value is much lower than the value of intrinsic resistivity of silicon carbide. Here, it is necessary to mention that more experimental data points (not less than 20 data points) are required to fully prove this. Our measurements include only four frequencies which makes the values that

FIGURE 9: The results of computer fitting to experimental data on impedance at direct (a and b) and at reverse voltage (c and d) for some samples.

we have obtained to be an estimation rather than exact value.

The oscillogram of the current switching diode based on 4H-SiC is shown in Figure 10. Switching of diodes has been performed from forward current ($I = 0.25$ mA) to reverse voltage 60 V. As one can see from Figure 10, the diodes have very fast switching time and duration of the reverse recovery current (of the order of 10 ns) for junctions with an area of approximately 6 mm².

If we assume that the transition process is determined by the capacity of the junction (capacitive processes) [48] and this time is proportional to $t_r = RC$, where R is the series resistance and C is the capacity of the junction, then the relaxation time t_r should be less than 1 ns.

However, it has been shown earlier [11] that transition processes involving nonequilibrium carriers in silicon carbide are determined by the level of trapping (EK_2 with energy $E_C - 0.16$ eV) and by the duration of the reverse recovery current which is >20 ns. This level is ascribed to the donor impurity of nitrogen and the observed concentration profile of silicon carbide diode associated with the diffusion of nitrogen as background impurities. As the switching time

in our diodes is fast (~ 10 ns), it can be assumed that in our samples the concentration of these centres (with the trapping levels near the middle of the gap) is relatively low.

The measured switching time is sufficiently close to the lifetime of minority carriers (10–20 ns) which has been evaluated by using diffusion capacity of junction. The Maxwell relaxation can also influence the switching process. Estimate shows that, for specific resistance between 90 and 130 $\Omega \cdot m$, Maxwell relaxation time is between 5 and 7 ns ($\tau_\mu = \epsilon \epsilon_0 / \sigma$, where ϵ is the dielectric constant of the silicon carbide, ϵ_0 is the electric constant, and σ is the conductivity of a semiconductor).

Thus, the estimations of RC time relaxation, lifetime of minority carriers, and Maxwell relaxation time of the current do not contradict our experimental data.

It should be noted that the reverse branch of I - V characteristics of diodes does not have sharp breakdown region. That is why current of around 100 mA is believed to be the beginning of breakdown process. The dependence of reverse voltage at 100 mA U ($I_R = 100$ mA) versus temperature is shown in Figure 11. It can be seen from Figure 11 that the diodes have rectifying properties up to 300°C.

FIGURE 10: Oscilloscope trace of the current switching diode based on 4H-SiC, measured when switching diodes from forward current ($I = 25$ mA) to a reverse voltage of 60 V.

FIGURE 11: The temperature dependence of the reverse breakdown voltage of diodes based on 4H-SiC (measurements were carried out at a current of 100 mA).

A fundamental property of the p - i - n diode is its i -region ambipolar carrier lifetime τ , which represents the average time during which an electron-hole pair exists in the i -region of the diode [50].

A common method of measuring the pin diode: carrier lifetime is by forward biasing the device with a known current (I_F) and then extracting a known reverse current (I_R) during the turn-off phase. This method is named the reverse recovery method, and the carrier lifetime can be estimated by using the following expression in the framework of this method [51]:

$$\tau = t_{rr} \ln \left(1 + \frac{I_F}{I_R} \right), \quad (15)$$

where t_{rr} is the reverse recovery time. According to Figure 10, τ is close to Maxwell relaxation time.

Thus, diodes having small switching time and duration of the reverse recovery current <10 ns, breakdown voltage

from 120 to 140 V, and capable of operating at temperatures up to 300°C were developed.

A clear advantage of this new method is the fast switching time. We believe that it is caused by a decrease in the concentration of the traps. The disadvantage of our technology is a small breakdown voltage, which can be eliminated by using SiC samples without micropipe defects. A more serious challenge is the intermediate high-resistivity layer that increases losses. To prevent formation of this layer, further research is needed.

This fabricated SiC diodes can be potentially used in mobile phones, DSC, lighting, Notebook PCs, HDD, PPC, and power supplies for communication devices [52].

4. Conclusion

New method of boron diffusion at low temperatures between 1150 and 1300°C has been used for formation of both SiC p - i junction and i -region in one technological process. As the conditions of junction formation in this method is essentially different from the conventional diffusion (low temperatures and process of diffusion is accompanied by formation of structure defects), it is of special interest to identify advantages and disadvantages of new method of diffusion.

Developed SiC p - i - n diodes have fast switching time, and duration of the reverse recovery current is less than 10 ns with a breakdown voltage of 120–140 V. Fabricated diodes possess capability to operate at temperatures up to 300°C. As the temperature of diffusion process is lower than the melting temperature of silicon, this new technology allows fabrication of diodes based on the SiC/Si epitaxial structures.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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