

## *Retraction*

# **Retracted: Investigation on V<sub>2</sub>O<sub>5</sub> Thin Films for Field Effect Transistor Applications**

### **Advances in Materials Science and Engineering**

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This article has been retracted by Hindawi, as publisher, following an investigation undertaken by the publisher [1]. This investigation has uncovered evidence of systematic manipulation of the publication and peer-review process. We cannot, therefore, vouch for the reliability or integrity of this article.

Please note that this notice is intended solely to alert readers that the peer-review process of this article has been compromised.

Wiley and Hindawi regret that the usual quality checks did not identify these issues before publication and have since put additional measures in place to safeguard research integrity.

We wish to credit our Research Integrity and Research Publishing teams and anonymous and named external researchers and research integrity experts for contributing to this investigation.

The corresponding author, as the representative of all authors, has been given the opportunity to register their agreement or disagreement to this retraction. We have kept a record of any response received.

### **References**

- [1] S. K. Suresh Babu, D. Jackuline Moni, D. Gracia, and A. G. Adigo, "Investigation on V<sub>2</sub>O<sub>5</sub> Thin Films for Field Effect Transistor Applications," *Advances in Materials Science and Engineering*, vol. 2021, Article ID 2414589, 7 pages, 2021.

## Research Article

# Investigation on $V_2O_5$ Thin Films for Field Effect Transistor Applications

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$V_2O_5$  thin films are analyzed for the substitution of  $SiO_2$  to reduce the leakage current in devices when  $SiO_2$  becomes ultrathin in submicron technology. Vanadium pentoxide ( $V_2O_5$ ) has a high-k dielectric constant of 25 and can be replaced as a gate oxide in the field-effect transistor.  $V_2O_5$  is deposited using pulsed laser deposition (PLD) in the oxygen ( $O_2$ ) environment at room temperature and characterized. The films surface morphology has been examined by scanning electron microscopy. The capacitance, dielectric constant, and dielectric loss are analyzed for fabricated metal oxide semiconductor (MOS) structure using Solartron SI-1260 impedance analyzer. The transfer characteristic of the fabricated device is analyzed using National Instruments NI-PXI 4110. The  $I_{ON}/I_{OFF}$  ratio of  $10^6$  and threshold voltage ( $V_{TH}$ ) of 0.6 V is obtained.

## 1. Introduction

Thin film technology has a vital role in electronic industries. The active thin film transistor (TFT) is a part of thin film technology which is a composition of various thin layers to form the MOSFET. These layers can be formed by a device either over silicon or a glass substrate. The replacement of silicon dioxide ( $SiO_2$ ) with other materials is becoming a great challenge in the community. Many developments have occurred with  $SiO_2$ , but still the current leakage in a device has not been controlled in the transistor. This current leakage leads a battery to drain in minutes in the gadgets and also reduces the efficiency by producing an enormous amount of heat. So, in order to solve this problem, material with high dielectric constant ( $k$ ) of more than 3.9 has to be used [1]. Pulsed laser deposition techniques have been reported to fabricate  $V_2O_5$  thin films [2–7]. The paper deals with the preparation of  $V_2O_5$  using pulsed laser deposition,

and its performance as a gate dielectric in MOSFET.  $V_2O_5$  is reported as the best rare Earth materials in terms of good thermodynamic stability and high quality interface with silicon. Hence, these materials are studied for silicon FET.

## 2. Experimental

Many deposition techniques are available in the literature for coating the thin films. Pulsed laser deposition (PLD) technique is used for its uniform and stoichiometry deposition [8–12]. Nd-YAG laser at 355 nm is used to deposit a thin film onto the substrate, and the deposition is carried out in a chamber at oxygen ( $O_2$ ) atmosphere [13–20]. The base pressure maintained during deposition is about  $3.8 \times 10^{-6}$  torr. The  $V_2O_5$  (Sigma-Aldrich, 99.999%) target is placed in a sample holder which will rotate at a rate of 10 rotations per minute (rpm) during deposition.  $V_2O_5$  thin films are deposited on the glass and silicon substrate in room

temperature [21–25]. The confirmation of  $V_2O_5$  phase angle is done using XRD. The thin films' surface morphology is studied by scanning electron microscope (JEOL model JSM-6390), and amorphous nature of  $V_2O_5$  films is found using X-ray diffractometer (Shimadzu model XRD-6000). The optical properties of the thin films were studied using ultraviolet spectroscopy (Shimadzu UV-240) and photoluminescence spectroscopy. The electrical properties were studied using an impedance analyzer (Solartron SI-1260) by varying the frequency. The transfer I–V characteristics of fabricated MOSFET were carried out with National Instrument PXI 4110.

### 3. Results and Discussion

$V_2O_5$  film (at R.T.) is deposited using PLD for gate dielectric.

$V_2O_5$  thin films are deposited at room temperature and  $400^\circ\text{C}$  using PLD, as shown in Figure 1. These deposited films are analyzed for the selection of the best film for the gate dielectric of FET.

**3.1. Structural Analysis.** The structural characterization, done by interpreting the XRD peak data, gives an insight about the crystallinity and phase changing behavior of the film when annealed at different temperatures. From the XRD plot, as in Figure 2, it is clearly shown that, as the temperature increases, the amorphous nature of the film is revealed. Deposition of the film is carried out at  $400^\circ\text{C}$  and subjected to vacuum annealing and then annealed at  $400^\circ\text{C}$ , wherein an increase in its crystalline nature is observed. The peak is observed at  $17$  (2theta value) for  $400^\circ\text{C}$ , and its (hkl Miller indices) values correspond to (002), and the system observed is orthorhombic in structure. The small peak is observed at  $32.8$  (2theta value) for the silicon substrate and verified from the JCPDS (78–0250), and its values corresponds to (111).

Grain size can be determined, with the Scherrer formula as

$$D = \frac{\lambda * 0.94}{\beta \cos \theta}, \quad (1)$$

where  $\lambda$  is the wavelength,  $\theta$  is the Bragg angle, and  $\beta$  as the line broadening (Table 1).

The XRD pattern of  $V_2O_5$  at room temperature, shown in Figure 2, reveals that the amorphous nature and the same film is annealed at  $400^\circ\text{C}$  and obtained at  $2\theta$  at  $17^\circ$ . Also, the more amorphous nature of the thin film ensures a high-k dielectric value which marks its application in the fabrication of FET devices as gate dielectric.

The energy dispersive X-ray spectrum is shown in Figure 3. The observation of peaks further confirms the presence of vanadium dioxide in the deposited thin film.

**3.2. Surface Topography Analysis.** Figure 4 gives the SEM image of  $V_2O_5$  at room temperature and illustrates a granular nature. The porosity increases the diffusion barrier

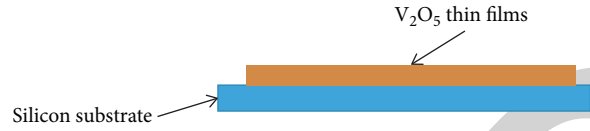


FIGURE 1:  $V_2O_5$  thin film deposition using PLD.

properties and will have a high-resistance effect on the layer, which can be more suitable for the gate dielectric layer.

**3.3. Film Morphology Analysis Using AFM.** AFM image (Figure 5) shows the small step layer deposition at maximum peak difference as  $833\text{ nm}$  over  $z$ -axis of the deposited film. It is observed for the  $20\ \mu\text{m} \times 20\ \mu\text{m}$  size of the placed sample. From the histogram graph, as shown in Figure 6, it is clearly observed that very few points are noted at higher peaks and all other points are almost uniformly deposited.

Observations carried out from the AFM characterization are given in Table 2. The root mean square roughness is about  $125\text{ nm}$  and maximum peak is observed at  $832\text{ nm}$  may be due to the ion implantation in the silicon substrate. The roughness average is noted as  $96\text{ nm}$  which shows the smooth deposition obtained using PLD and is more suitable for the thin film transistor. The average height is  $329\text{ nm}$  and proves the smooth deposition of the  $V_2O_5$  thin film.

**3.4. Capacitance, Dielectric Constant, and Dielectric Loss Analysis.** Solartron SI-1260 is used for the analysis of capacitance, dielectric constant, and dielectric loss of  $V_2O_5$  deposited at room temperature. Metal oxide semiconductor (MOS) structure is deposited over the N-Type silicon using the PLD technique, as shown in Figure 7. Gold is coated over the deposited film as terminals for electrodes. From equation (2), the capacitance of the MOS structure is calculated and plotted in Figure 8:

$$C = \frac{k \cdot \epsilon \cdot A}{d}. \quad (2)$$

From Figure 8, it is observed that the capacitance (in microfarad) of the MOS gradually decreases with the increase in the frequency; the amorphous state of the film has a good charging value till kilo Hz. This configured film can be more suitable for the low-frequency applications:

From equation (3) and (4), the obtain dielectric loss is

$$\tan \delta = \frac{\epsilon''}{\epsilon'}, \quad (5)$$

where  $t$  is thickness of the film,  $\omega$  is angular frequency,  $Z'$  is the real part of impedance,  $Z''$  is the imaginary part of impedance,  $\epsilon_0$  is permittivity of free space, and  $A$  is the area of the film.

The dielectric constant for the deposited film is observed high at low frequency and decreases with increase

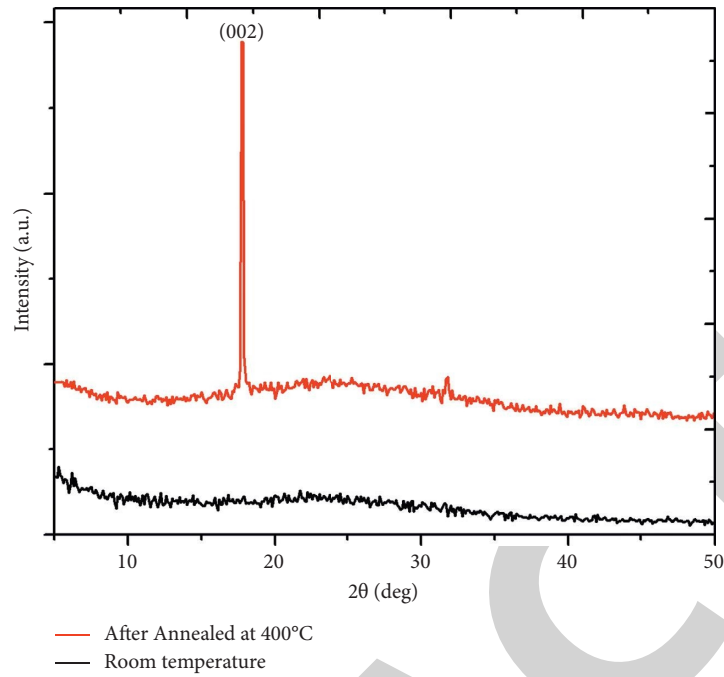


FIGURE 2: XRD plot of  $V_2O_5$  at room temperature.

TABLE 1: The grain size of the thin films.

Sample	D (nm)
As deposited	134
400°C	185

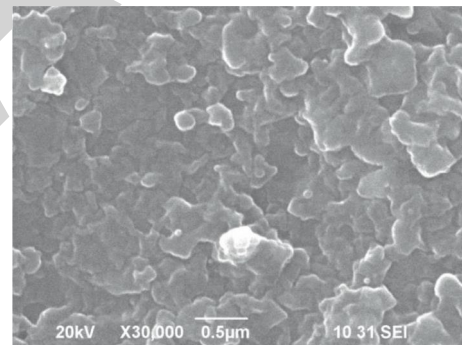


FIGURE 4:  $V_2O_5$  SEM image of at room temperature.

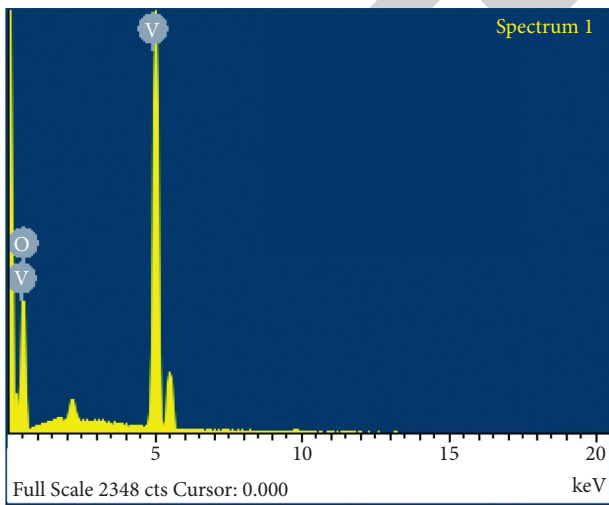


FIGURE 3:  $V_2O_5$  EDAX spectra.

in frequency, as shown in Figure 9. These changes happen because of larger grain boundaries of amorphous film at the applied electric filed [23].

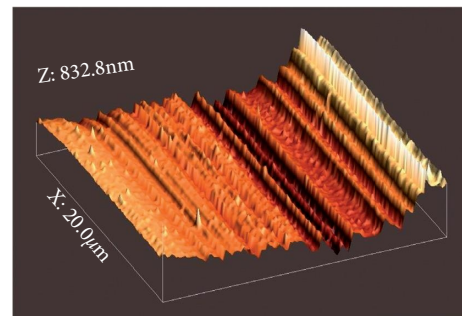
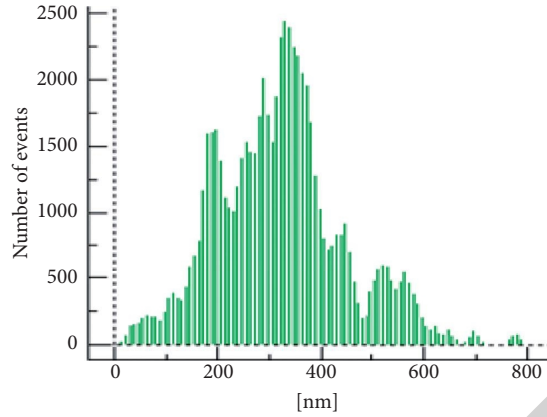
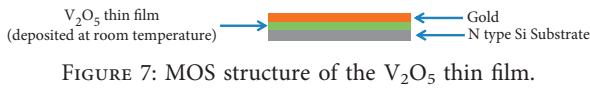
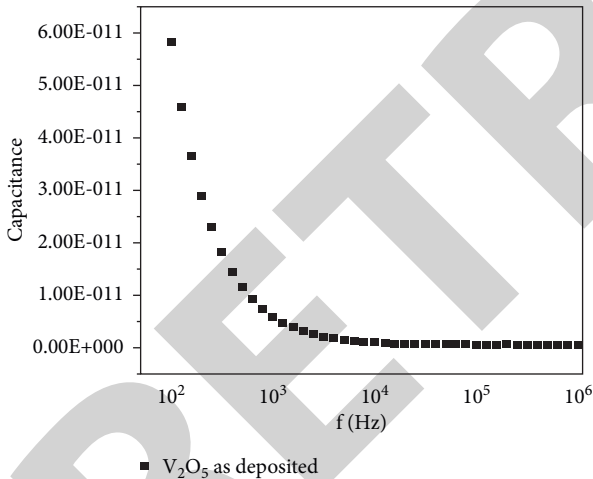


FIGURE 5:  $V_2O_5$  AFM image at room temperature.

FIGURE 6: Histogram graph of the AFM image of  $V_2O_5$ .TABLE 2:  $V_2O_5$  parameter analysis using AFM.

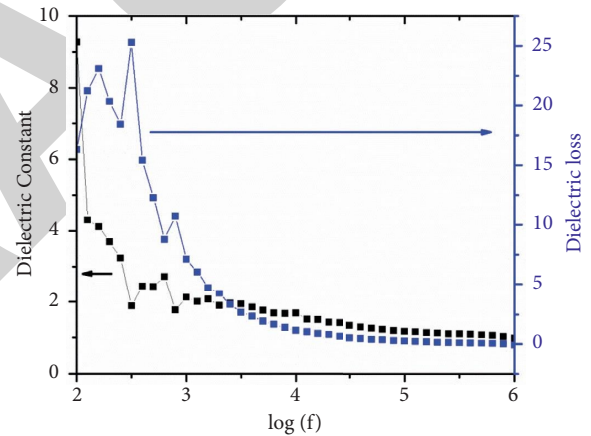
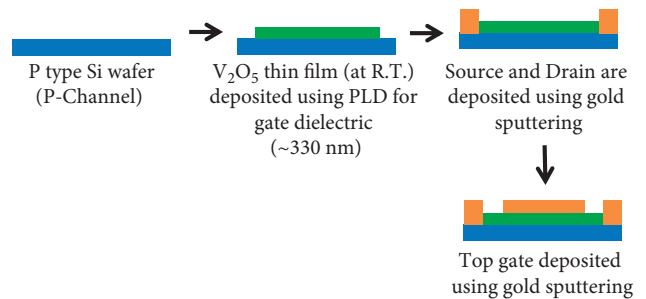
RMS roughness (nm)	Maximum value (nm)	Average roughness (nm)	Average height (nm)
125	832	96	329

FIGURE 7: MOS structure of the  $V_2O_5$  thin film.FIGURE 8: Capacitance vs. frequency analysis of the  $V_2O_5$  thin film prepared at room temperature.

$$\epsilon' = \frac{t}{\omega A \epsilon_0} \cdot \frac{Z''}{Z'^2 + Z''^2}, \quad (3)$$

$$\epsilon'' = \frac{t}{\omega A \epsilon_0} \cdot \frac{Z'}{Z'^2 + Z''^2}. \quad (4)$$

With these capacitance, dielectric constant, and dielectric loss results, the  $V_2O_5$  thin film deposited at room temperature is more stable at low frequency and can be a better gate dielectric layer in the replacement of conventional  $SiO_2$  in MOSFET.

FIGURE 9: Dielectric constant and dielectric loss vs. log frequency of the  $V_2O_5$  thin film prepared at room temperature.FIGURE 10: Fabrication steps involved in the  $V_2O_5$  film gate dielectric-based Si-MOSFET.

#### 4. MOSFET Fabrication

Figure 10 shows the fabrication steps of  $V_2O_5$  thin film gate dielectric-based Si-MOSFET. In this device, P-type silicon is used as the channel and also as a base layer for the proposed

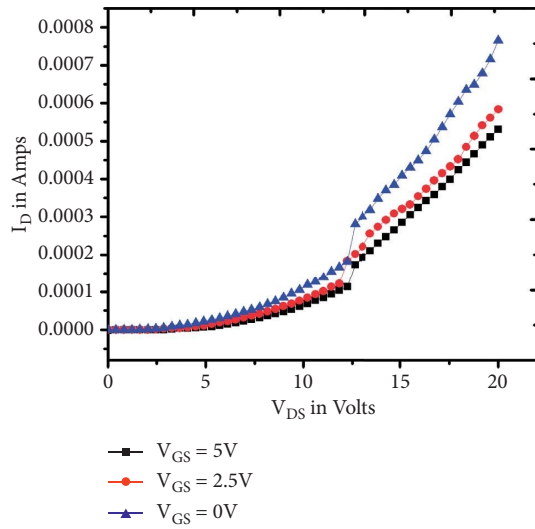


FIGURE 11: Output characteristics of  $V_2O_5$  thin film gate dielectric of Si-MOSFET.

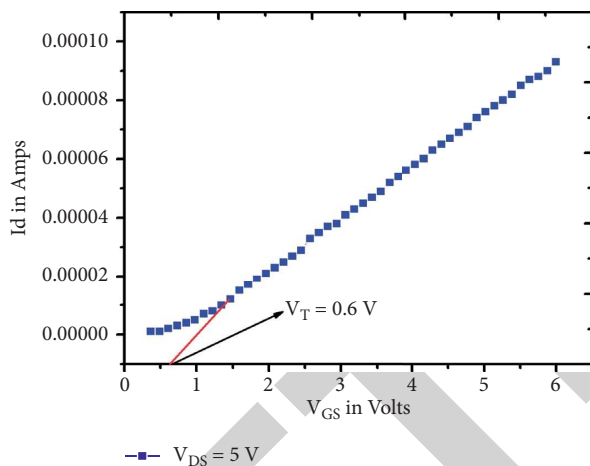


FIGURE 12: Transfer characteristics of  $V_2O_5$  thin film gate dielectric of Si-MOSFET (square root of drain current vs.  $V_{GS}$ ).

device. It is well cleaned and processed for the device fabrication. Inside the PLD chamber, the prepared  $V_2O_5$  pellet is fixed as the target. With prepared stainless steel (SS) mask, the  $V_2O_5$  thin film is deposited at 330 nm at room temperature as a gate dielectric layer. The thickness is measured using AFM. By using sputtering as the source, drain and gate are deposited with gold (Au) with the designed SS-mask.

The electrical characterization of fabricated MOSFET is carried out using National Instruments NI-4100. With the designed LabVIEW platform, the output and transfer characteristics are analyzed. Figure 11 shows the output characteristics of  $V_2O_5$  gate dielectric-based Si-MOSFET.

In output characteristics,  $V_{DS}$  is varied between 0 and 20 Volts with various constant gate voltage (0, 2.5 V, and 5 V), and the corresponding drain current  $I_D$  is noted. Kink in the I-V characteristics is because of the sudden rise in the applied voltage (randomly set by the program), which causes this effect.

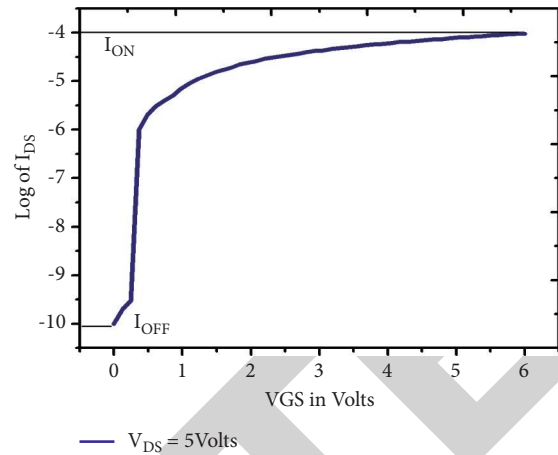


FIGURE 13: Transfer characteristics of  $V_2O_5$  thin film gate dielectric of Si-MOSFET (log. of drain current vs.  $V_{GS}$ ).

From Figure 12, the threshold voltage  $V_{TH}$  is found to be 0.6 V [26–29]. The  $I_{ON}/I_{OFF}$  ratio of fabricated MOSFET is calculated from the transfer characteristics results which are shown in Figure 13. The  $I_{ON}/I_{OFF}$  current ratio can be calculated by plotting the obtained drain current in the log scale; by measuring the maximum point in graph to minimum point of drain current gives the value of the  $I_{ON}/I_{OFF}$  current ratio as  $10^6$ .

The results show that the fabricated MOSFET has less leakage current from the observed  $I_{ON}/I_{OFF}$  current and  $V_2O_5$  thin film is more suitable for the gate dielectric of MOSFET.

## 5. Conclusion

The various characteristics of  $V_2O_5$  is analyzed and reported. The replacement of  $SiO_2$  dielectric in MOSFET is due to its large leakage current in submicron technology; the MOS structure of the  $V_2O_5$  thin film is studied, and its capacitance, dielectric constant, and dielectric loss at low frequency are analyzed. The results revealed that the  $V_2O_5$  thin film deposited at room temperature can be used as the gate dielectric of MOSFET. The Si-MOSFET is fabricated with  $V_2O_5$  thin film as the gate dielectric by using PLD. It is also observed that the good  $I_{ON}/I_{OFF}$  current ratio is  $10^6$  and threshold voltage ( $V_{TH}$ ) is 0.6 V. This  $I_{ON}/I_{OFF}$  ratio shows less leakage current with stable threshold voltage, and henceforth, the  $V_2O_5$  thin film can be a good replacement of  $SiO_2$  in MOSFET [30–36].

## Data Availability

The data used to support the findings of this study are included within the article.

## Disclosure

This study was performed as a part of the Employment of Addis Ababa Science and Technology University, Ethiopia.

## Conflicts of Interest

The authors declare that they have no conflicts of interest.

## References

- [1] H. Chakraborty and D. Durga Misra, "Characterization of high-k gate dielectrics using MOS capacitors," *International Journal of Scientific and Research Publications*, vol. 3, no. 12, 2013.
- [2] J. Scarminio, A. Talledo, A. A. Andersson, S. Passerini, and F. Decker, "Stress and electrochromism induced by Li insertion in crystalline and amorphous  $V_2O_5$  thin film electrodes," *Electrochimica Acta*, vol. 38, no. 12, pp. 1637–1642, 1993.
- [3] R. Enjalbert and J. Galy, "A refinement of the structure of  $V_2O_5$ ," *Acta Crystallographica Section C Crystal Structure Communications*, vol. 42, no. 11, pp. 1467–1469, 1986.
- [4] C. Sanchez, J. Livage, and G. Lucazeau, "Infrared and Raman study of amorphous  $V_2O_5$ ," *Journal of Raman Spectroscopy*, vol. 12, no. 1, pp. 68–72, 1982.
- [5] R. Baddour-Hadjean, J. P. Pereira-Ramos, C. Navone, and M. Smirnov, "Raman study of electrochemical lithium intercalation into sputtered crystalline  $V_2O_5$  thin films," *Chemistry of Materials*, vol. 20, no. 5, pp. 1916–1923, 2008.
- [6] S. Senapati and S. Panda, "Effect of aging of  $V_2O_5$  sol on properties of nanoscale films," *Thin Solid Films*, vol. 599, pp. 42–48, 2016.
- [7] D. O. Scanlon and A. Walsh, B. J. Morgan and G. W. Watson, "An ab initio study of reduction of  $V_2O_5$  through the formation of oxygen vacancies and Li intercalation," *Journal of Physical Chemistry C*, vol. 112, no. 26, pp. 9903–9911, 2008.
- [8] M. Benmoussa, A. Outzourhit, A. Bennouna, and E. L. Ameziane, "Electrochromism in sputtered  $V_2O_5$  thin films: structural and optical studies," *Thin Solid Films*, vol. 405, no. 1-2, pp. 11–16, 2002.
- [9] A. Kumar, P. Singh, N. Kulkarni, and D. Kaur, "Structural and optical studies of nanocrystalline  $V_2O_5$  thin films," *Thin Solid Films*, vol. 516, no. 6, pp. 912–918, 2008.
- [10] J. Huotari, R. Bjorklund, J. Lappalainen, and A. Lloyd Spetz, "Pulsed laser deposited nanostructured vanadium pentoxide thin films characterized as ammonia sensors," *Sensors and Actuators B*, vol. 217, pp. 22–29, 2015.
- [11] D. Q. Liu, W. W. Zheng, H. F. Cheng, and H. T. Liu, "Thermochromic  $VO_2$  thin film prepared by post annealing treatment of  $V_2O_5$  thin film," *Advanced Materials Research*, vol. 79–82, pp. 747–750, 2009.
- [12] A. Mauger and C. M. Julien, " $V_2O_5$  thin films for energy storage and conversion," *AIMS Materials Science*, vol. 5, no. 3, p. 349, 2018.
- [13] C. Julien, E. Haro-Poniatowski, M. A. Camacho-López, L. Escobar-Alarcón, and J. Jiménez-Jarquín, "Growth of  $V_2O_5$  thin films by pulsed laser deposition and their applications in lithium microbatteries," *Materials Science and Engineering: B*, vol. 65, no. 3, pp. 170–176, 1999.
- [14] L. Amarin, H. Cardozo, L. D. S. Martins, and A. Urbano, "Commitment between roughness and crystallite size in the vanadium oxide thin film opto-electrochemical properties," *Materials Research*, vol. 22, 2018.
- [15] Y. Zhang, J. Zheng, Y. Zhao, T. Hu, Z. Gao, and C. Meng, "Fabrication of  $V_2O_5$  with various morphologies for high-performance electrochemical capacitor," *Applied Surface Science*, vol. 377, pp. 385–393, 2016.
- [16] K. Shibuya and A. Sawa, "Optimization of conditions for growth of vanadium dioxide thin films on silicon by pulsed-laser deposition," *AIP Advances*, vol. 5, no. 10, Article ID 107118, 2015.
- [17] C. V. Ramana, O. M. Hussain, R. Pinto, and C. M. Julien, "Microstructural features of pulsed-laser deposited  $V_2O_5$  thin films," *Applied Surface Science*, vol. 207, no. 1–4, pp. 135–138, 2003.
- [18] S. Majid, D. K. Shukla, F. Rahman, K. Gautam, V. G. Sathe, and R. J. Phase, D. M. Phas, "Characterization of pulsed laser deposition grown  $V_2O_5$  converted  $VO_2$ ," *Journal of Physics: Conference Series*, vol. 755, Article ID 012027, 2016.
- [19] A. L. S. Hassen-Bey, T. Hakim, S. Lafane, and A. Z. Ait Djafer, "Substrate effect on electrical properties of vanadium pentoxide thin film for memristive device applications," in *Proceedings of the IEEE-Icse2016*, Kuala Lumpur, Malaysia, August 2016.
- [20] M. Jeanne, J.-G. Zhang, J. Turner, and D. Ginley, *Lithium Charging Capacities of Vanadium Pentoxide Thin Films Grown by Pulsed Laser Deposition for Rechargeable Li Battery Applications*, National Renewable Energy Laboratory, Golden, CO, USA, 1617.
- [21] G. A. Niklasson, S.-Y. Li, and C. G. Granqvist, "Thermochromic vanadium oxide thin films: electronic and optical properties," *Journal of Physics: Conference Series*, vol. 559, Article ID 012001, 2014.
- [22] N. B. Atan, I. B. Ahmad, and B. B. Yeop Majlis, "Effects of high-k dielectrics with metal gate for electrical characteristics of 18nm nmos device," in *Proceedings of the IEEE-ICSE 2014*, Kuala Lumpur, Malaysia, August 2014.
- [23] R. Fajgar, J. Kupcik, S. Jan, and N. Filip, "Characterization and properties of titanium-vanadium pentoxide thin films prepared by arf laser ablation," in *Proceedings of the NANOCON 2010. International Conference*, Olomouc, Czech Republic, October 2010.
- [24] X.-F. Zhang, K.-X. Wang, X. Wei, and J.-S. Chen, "Carbon-coated  $V_2O_5$  n as high performance cathode material for lithium ion batteries," *Chemistry of Materials*, vol. 23, no. 24, pp. 5290–5292, 2011.
- [25] N. M. Abd-Alghafour, N. M. Ahmed, Z. Hassan, and S. M. Mohammad, "Influence of solution deposition rate on properties of  $V_2O_5$  thin films deposited by spray pyrolysis technique," *AIP Conference Proceedings*, vol. 1756, no. 1, Article ID 090010, 2016.
- [26] K.-J. Baeg, G.-T. Bae, and Y.-Y. Noh, "Efficient charge injection in p-type polymer field-effect transistors with low-cost molybdenum electrodes through  $V_2O_5$  i," *ACS Applied Materials & Interfaces*, vol. 5, no. 12, pp. 5804–5810, 2013.
- [27] V. K. Kaushik, C. Mukherjee, T. Ganguli, and P. K. Sen, "Electrical and optical characteristics of aerosol assisted CVD grown ZnO based thin film diode and transistor," *Journal of Alloys and Compounds*, vol. 696, pp. 727–735, 2017.
- [28] S. Zhao, J. K. Sin, B. Xu, M. Zhao, Z. Peng, and H. Cai, "A high performance ethanol sensor based on field-effect transistor using a  $LaFeO_3$  nano-crystalline thin-film as a gate electrode," *Sensors and Actuators B: Chemical*, vol. 64, no. 1-3, pp. 83–87, 2000.
- [29] Y. Shimizu, K. Nagase, N. Miura, and N. Yamazoe, "New preparation process of  $V_2O_5$  Thin film based on spin-coating from organic vanadium solution," *Japanese Journal of Applied Physics*, vol. 29, no. 9, pp. L1708–L1711, 1990.
- [30] E. C. Elizabeth, "Optical properties of vanadium dioxide and vanadium pentoxide thin films," *Applied Optics*, vol. 30, no. 19, 1991.
- [31] R. André, F. Natálio, M. Humanes et al., " $V_2O_5$  nipla," *Advanced Functional Materials*, vol. 21, no. 3, pp. 501–509, 2011.
- [32] Y. Yue and H. Liang, "Micro- and nano-structured vanadium pentoxide ( $V_2O_5$ ) for electrodes of lithium-ion batteries," *Advanced Energy Materials*, vol. 7, no. 17, 17 pages, Article ID 1602545, 2017.
- [33] S. Deng, Z. Yuan, Z. Tie, C. Wang, L. Song, and Z. Niu, "Electrochemically induced metal-organic-derived amorphous  $V_2O_5$  for superior rate aqueous zinc-ion batteries,"

*Angewandte Chemie International Edition*, vol. 59, no. 49, pp. 22002–22006, 2020.

- [34] Y. Liu, Q. Chen, X. Du, X. Liu, and Li Peng, “Effects of substrate on the structure and properties of  $V_2O_5$  thin films prepared by the sol-gel method,” *AIP Advances*, vol. 9, no. 4, Article ID 045028, 2019.
- [35] S. Korkmaz, F. M. Tezel, and İ. A. Kariper, “Synthesis and characterization of GO/ $V_2O_5$  thin films,” *Synthetic Metals*, vol. 242, pp. 37–48, 2018.
- [36] A. A. Mane and A. V. Moholkar, “Effect of film thickness on  $NO_2$  gas sensing properties of sprayed orthorhombic nanocrystalline  $V_2O_5$  thin films,” *Applied Surface Science*, vol. 416, pp. 511–520, 2017.

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