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Research Article

Improved Switching Characteristics of Fast Power MOSFETs Applying Solder Bump Technology

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The impact of a reduced package stray inductance on the switching performance of fast power MOSFETs is discussed applying advanced 3D packaging technologies. Starting from an overview over new packaging approaches, a solder bump technology using a flexible PI substrate is exemplarily chosen for the evaluation. Measurement techniques to determine the stray inductance are discussed and compared with a numerical solution based on the PEEC method. Experimental results show the improvement of the voltage utilization while there is only a slight impact on total switching losses.

1. INTRODUCTION

Fast power MOSFETs in the voltage class up to 100 V realize very high current and power densities while at the same time switching transients achieve times below 50 nanoseconds. Due to the fast switching, parasitic inductances in the circuit have significant impact on converter power since overvoltages and oscillations reduce the voltage margin and hence, the maximum power rating. Optimizing the packaging of the devices is an important step to improve the utilization of the semiconductors and make use of their full current and voltage ratings.

Usually, state-of-the-art devices are assembled in discrete housing, or in power modules. The semiconductor dice are soldered to a leadframe or DBC, and thick wire bond technology is applied to contact the top source and gate pads of the dice as well as the external terminals. The wire bonds are a bottleneck with regard to stray inductance and the ohmic losses, that is, the current utilization of the chips. Further drawbacks include reliability issues and limitations with regard to 3D integration.

Several new packaging technologies have been proposed to overcome the structural limits of the wire bond technology and the related reliability problems (e.g., [1–8]) as well as the reliability and thermal constraints associated with the die solder contact [9]. Only a few ideas have made the transition to market yet, for example, the discrete International Rectifier "DirectFET" [10]. The ("low-temperature joining technique") LTJT, which is a promising alternative for the die solder bond, is close to realization for automotive applications [11].

Apart from the LTJT, most of the proposed packaging solutions concentrate on a substitution of the wire bonds including alternatives like ribbon bonding [12] or spring contacts as well as planar interconnect technologies in 3-dimensional stacked assemblies. The latter include solutions with a prestructured circuit board, for example, a copper frame, a flexible substrate, or a second DBC that is usually soldered to the top side of the dice by solder bumping. Examples are the "flip-chip-on-flex" technology [3, 4] and the "power ball grid array" technology applying two DBCs [5]. In derivatives of these solutions, copper posts or cylinders are soldered between the two substrates [6, 7], which might be necessary for high-voltage applications. Other feasible alternatives cover solutions where the electrical circuit layout is structured during a planar integration process with metallurgically-formed interconnects leading to a multilayer assembly. Typical examples are the planar integration with an "embedded power stage" [1] or the "Planar Power Polymer Packaging Technology" [2]. Table 1

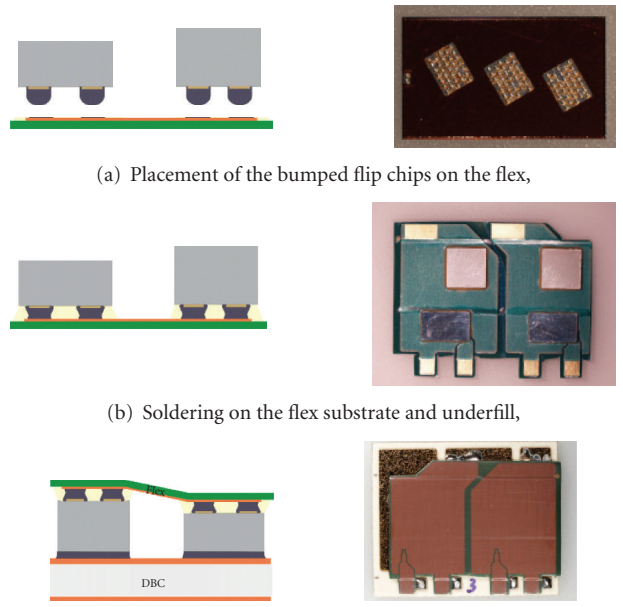
Table 1: Typical examples of alternative packaging technologies substituting wire bonding technology.

	Embedded power technology [1]	Planar power polymer packaging technology [2]	Flip-chip-on-flex technology [3, 4]	DBC sandwich technology [5]
Interconnect technology	Sputtering + electroplating	Sputtering + electroplating	Solder bump	Solder bump
Bottom substrate	DBC	DBC	DBC	DBC
Top substrate/chip carrier	Die embedded in a ceramic (Al_2O_3) + dielectric coating (125 μm).	Die mounted on a polymer film (50 μm) applying an adhesive.	Die soldered to a flexible polymer (50 μm).	Die soldered to a 2nd DBC.
Top Cu metallization thickness	125 μm–150 μm	75–125 μm	50 μm–150 μm	typical 300 μm Cu
Interconnects:				
- Diameter d	Vias with d = 1000 μm	Vias with d = 500–1000 μm	Solder bumps with d = 750–900 μm	Solder bumps with d = 200 μm
- Height	125 μm	$\approx$ 50–100 μm	$\approx$ 500–1200 μm	125 μm
- Pitch	not defined / [1]: 6 vias	not defined	1 bump per Al-pad	360 μm

summarizes the basic material and geometrical data of the described 3D approaches.

There are several advantages anticipated from 3D sandwich assemblies including higher power density due to a compact layout, reduced interconnect resistances, and higher current rating compared to wire bonds as well as less parasitic stray inductance giving improved switching behavior and reduced overvoltage. Furthermore, improved heat paths and the possibility to apply double-side cooling concepts due to a second planar surface are expected. The compact integration of control electronic components into the power assembly might be a further benefit. The reliability of 3D assemblies, on the other hand, has to be investigated thoroughly. Difficulties are to be expected, since several materials with different CTEs (coefficient of thermal expansion) are joined with large contact areas.

The focus of this paper is the evaluation of the switching behavior of fast MOSFETs applying sandwich-type packaging. Exemplarily, a solder bump technology is used with the top contacts of the dice soldered to a flexible PI substrate. The analysis is based on experimental results of a half-bridge topology in buck converter configuration. The prototypes are built with 100 V-MOSFETs (Infineon OptiMOS, chip area 26 mm^2) with high current rating and low on-state resistance in the range below 5 mΩ, and Schottky diodes (IXYS DWS 36-80 A). The wire bonds are limiting the chip utilization for this kind of MOSFET due to their current rating given by the maximum wire temperature.



(a) Placement of the bumped flip chips on the flex,

(b) Soldering on the flex substrate and underfill,

(c) Die bond on the DBC with flex deformation (thin Cu metallization) or die bond with preformed flex

Figure 1: Process flow of the flip chip technology. (Right figures: photographs showing the prototype during the assembly process: (a) bumped MOSFET, (b) chips soldered to the flex, (c) complete assembly).

2. PROTOTYPE DEVELOPMENT

2.1. *Flip chip-technology using a flexible PI substrate*

Figure 1 depicts the principle process flow of the flip chip technology. As a prototype, a complete half-bridge circuit is built applying two MOSFETs and two Schottky diodes.

The bumping layout for the chips is designed in order to maximize the number of solder joints within the design rules for flip chip assembly. 100 μm pad size at 200 μm pitch are chosen as this design still allows assembly using conventional equipment. As a basic design rule, the pad size should be between 30–50% of the chosen pitch. The bump array is chosen over a larger solder joint on the whole source pad area in order to reduce stress. Chip layouts optimized for wire bonding are limiting the area which can be used, since only a part of the chip is covered with Al-pads and the rest of the surface is coated with a passivation.

The wafers are bumped with electroless Ni/Au using a spin on resist and photolithography due to the unpassivated metallization (resist: 6 μm, Ni/Au bumps: 6 μm). The Ni

Figure 2: FC technology: Cross-section through MOSFET (left) and diode (right), showing the principle of height compensation by flex deformation.

Table 2: Summary of interconnect data

	FC–Flex
Diameter d	100 μm pad /$d \approx$ 125 μm (ball)
Height h	60 μm
Pitch p	200 μm
Ratio $r_A = A_s/A_{\text{chip}}(\varepsilon = 80\%)$	max. 20%
Material	Soft solder
- thermal conductivity	35–50 W/mK
- electrical conductivity	7–10 $10^6/\Omega$m
Average thermal conductivity λ_{av}	max. 7–10 W/mK
Average electrical conductivity σ_{av}	max 1.5–2 $10^6/\Omega$m
Metallization layer	50–150 μm Cu

bumps grow in the resist openings. Then SAC solder paste is printed on the Ni/Au UBM and reflowed to form solder bumps of 60 μm height. The chips are placed on the flexible substrate (50 μm polyimide with Cu/Ni/Au metallization of 50, 100, or 150 μm Cu-thickness depending on the rated current) and soldered in a conventional reflow step with a maximum temperature of 250°C.

In order to compensate the height difference of the chips and contact the interconnects to external leads, it is aimed for deformation of the flexible substrate during the assembly on the DBC (Figure 2). It turns out that for the thicker metallization layers plastic deformation is not achieved during the bonding process at 200°C with 5 kg pressure. But for these substrates, a forming step before the assembly is possible comparable to the forming of leadframes without altering the rest of the process flow.

2.2. Geometric and electric characteristics

Table 2 summarizes the basic geometric data for the solder bump technology. Different from the comparable solutions [3, 4] given in Table 1, bump diameter and pitch are chosen relatively small in the 100–200 μm range. For the FC technology, the small diameters are advantageous with regard to stress in the solder joints. On the other hand, the height of the interconnects is limited according to the approximation of the solder bumps as balls, giving restrictions to insulation clearances.

The cross section of the solder bumps and the total contact area on the chip should be as large as possible to reduce current densities and losses. The available contact area is restricted by the pad layout of the chip. From existing data for active chips, a maximum of $\varepsilon \approx 80\%$ of the total chip area A_{chip} can be estimated for the pads (for the chip in Figure 1, ε is only 18%.) Assuming an average diameter

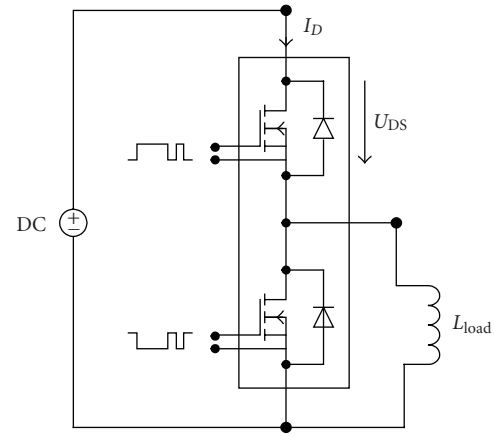


Figure 3: Test circuit.

d_{av} for a single contact, the total contact area A_s related to A_{chip} is

$$r_A = \frac{A_{s,\text{total}}}{A_{\text{chip}}} = \frac{\pi}{4}\frac{d_{\text{av}}^2}{p^2}\cdot\varepsilon. \quad (1)$$

The ratio r_A is introduced for comparability reasons. It defines an average electrical conductivity σ_{av} and an average thermal conductivity λ_{av} of the top chip contact, see Table 2. Since the solder bumps are very short, their contribution to the power losses is negligible if the maximum r_A is used .

Considering the top metallization, with a maximum Cu-thickness of 100–150 μm, the FC technology is comparable to solutions [1–4]. The current rating of the metallization is basically defined by the ohmic losses and the heat paths in the package. This aspect is further discussed in [13].

With regard to parasitics and switching characteristics, the chosen FC demonstrator is exemplary for a variety of 3D packages.

3. MEASUREMENT OF THE STRAY INDUCTANCE

The switching characteristics of the power MOSFETs show the interaction of the semiconductor device properties with the stray inductance L_σ of the assembly. Parasitic capacitances further contribute to the switching behavior, but since the internal MOSFET capacitances are dominant, the impact of the package can be neglected. In order to determine the stray inductance of a commutation circuit, apart from double-pulse measurements in buck converter configuration (see Figure 3), further techniques exist including voltage measurements based on an externally switched current and measurements applying an impedance analyzer.

3.1. Double-pulse measurements

A test system has been built which consists of a DC-link capacitor bank with up to 15 mF and a tapped air-core load coil with up to 150 μH supplemented by a gate drive and a liquid cooling system to mount the flip chip assembly. The test setup has a maximum voltage rating

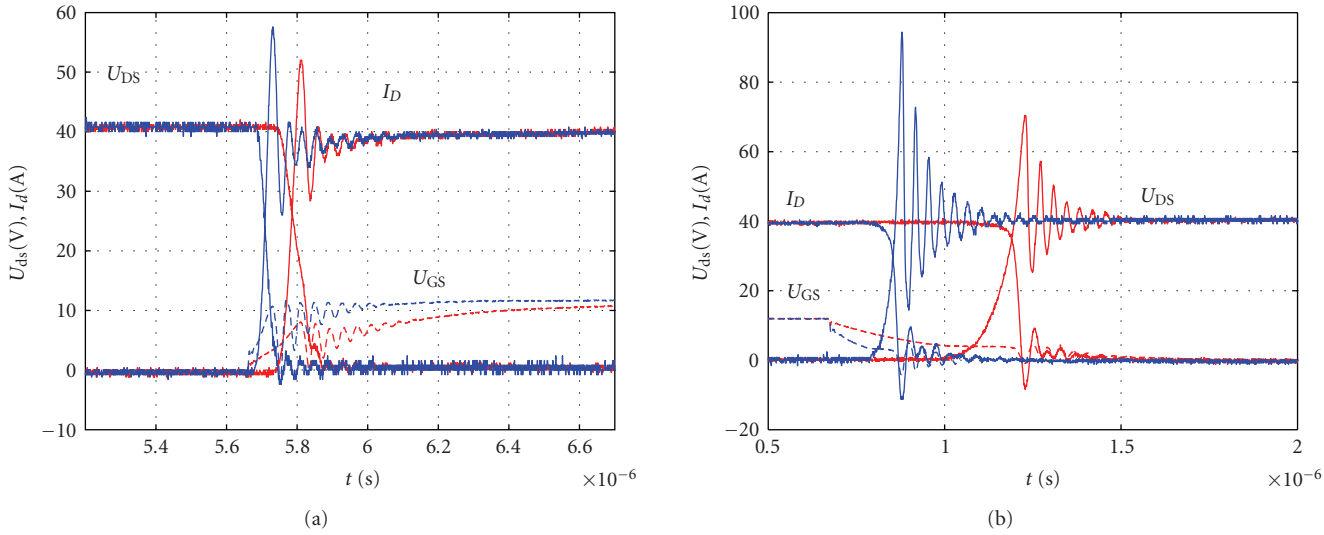


Figure 4: Switching characteristics of the 100 V MOSFET assembly with different gate resistances; blue: RG = 5.6 Ω red: RG = 22 Ω (a) turn-on, (b) turnoff.

of 200 V and is capable of continuous load currents up to 250 A. The gate drive is capable of 9 A peak currents with 20 nanoseconds rise/fall time into 10 nF capacitive loads. As some components like the dc-link capacitor bank and the load inductance are easily changed, the voltage and current rating is adaptable over a wide range. Figure 3 depicts the basic double-pulse test circuit and switching principle. The current is measured with a high performance Rogowski current transducer of high bandwidth allowing to correctly acquiring steep current transients. The delay of 40 nanoseconds is corrected in the figures. The voltage is captured with the full bandwidth of 500 MHz. Basically, from the double-pulse measurements, switching times, switching energies, and the voltage and current overshoots may be derived, all of which depend on the chosen semiconductors, on the design of the test circuit, and on the gate driver.

Double-pulse measurements varying the load current and the gate resistance have been performed. Figure 4 exemplarily depicts the turn-on and turnoff characteristics of the flip chip demonstrator switching 40 A at 40 V using a gate resistance of either 5.6 Ω or 22 Ω. Typically, since the turn-on is governed by the Schottky diode, the impact of the gate resistance is more evident in the turnoff. For the chosen MOSFET type, switching times below 100 nanoseconds are typical.

Measuring the oscillation frequency in conjunction with the output capacitance of the MOSFET gives the total stray inductance of the circuit including dc link and external leads. Due to the oscillations, deducing the stray inductance only from the voltage overshot at turnoff is not feasible. With a measured oscillation frequency of 27 MHz and a specified typical MOSFET capacitance C_{oss} = 1.37 nF (maximum 1.82 nF), the stray inductance of the commutation circuit is calculated to L_σ = 19–25.3 nH.

A more accurate result is achieved by introducing a defined additional inductance ΔL into the circuit and analyzing the change in the oscillation frequency. Neglecting changes in the mutual inductances, the original inductance is then achieved according to

$$L_\sigma = \frac{\Delta L}{(f_1/f_2)^2 - 1}. \tag{2}$$

From the results in the following section, for ΔL = 10 nH the frequency changes to f_2 = 23 MHz and hence, the stray inductance of the commutation circuit is calculated to 26.5 nH.

Since these results include the dc link (interconnects and capacitors) and external leads, other measurement techniques are required to determine the contribution of the sandwich package to the overall stray inductance.

3.2. Externally switched current

Eliminating the impact of the device's switching characteristics is achieved, if the load current is switched externally while the devices of the DUT are continuously in the on-state. With an appropriate voltage measurement, the stray inductance of the package itself can be measured. Figure 5 depicts the operation principle of this technique. The test circuit is designed to produce a current rise of 200 A/μs at 42 V and 0.2 μH. Since currents up to 50 A arise, the on-state voltage drop of the semiconductors needs to be considered.

Hence, the total stray inductance of the package is derived according to

$$L_\sigma = (\Delta U - 2 \cdot R_{DS,on} \cdot I_D) \Big/ \left.\frac{dI}{dt}\right|_{I_D}. \tag{3}$$

Table 3 summarizes the results for the flip chip on flex demonstrator. Since the MOSFET on-state losses may be calculated more exactly than the on-state losses of the body diode in parallel to the external Schottky diode, the results

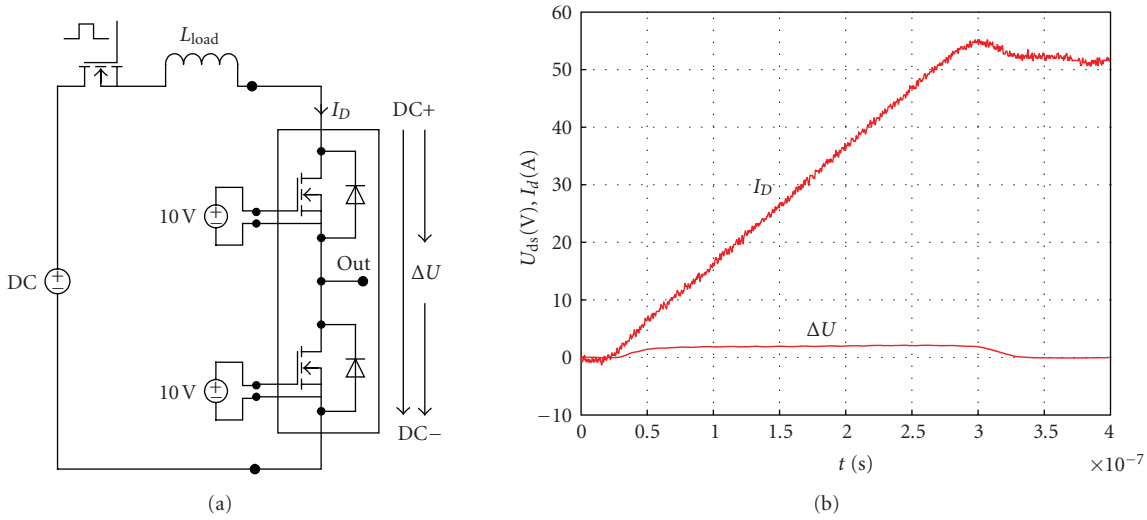


Figure 5: Measurement of the voltage drop across the package with an externally switched current.

Table 3: Stray inductance measurement at 200 A/μs.

	Flip chip assembly	TO 220 assembly
DC+-DC−	8.44 nH	26.5 nH
DC+-Out	5.4 nH	14.0 nH
Out-DC−	3.86 nH	13.5 nH

are given for the forward direction. From dc measurements, the on-state resistance is determined to 3.7 mΩ at 25°C chip temperature with 20 A test current. Although only 100 solder bumps could be placed due to the limited source pad area of the chip, the Rdson is reduced compared to the TO220 device. The corresponding datasheet (Infineon IPP05CN10N) specifies 4.1–5.6 mΩ for the TO220 and 3.8–5.1 mΩ for the TO263 housing.

For comparison, the same setup is used characterizing a standard assembly with two MOSFETs each in TO 220 housing. In this case, the MOSEFTs are soldered onto a dummy substrate with a geometry comparable to the flip chip assembly. The voltage is measured across equivalent connection points on the dummy package. With the $R_{DS,on}$ determined to be 7 mΩ, the resulting stray inductance of this assembly is calculated to 26.5 nH and hence, considerably higher than the flip chip inductance.

In Table 3, the sum of the two partial inductances is slightly higher than the total inductance due the mutual inductance between the two circuit paths.

3.3. Impedance analyzer

A different alternative is the use of an impedance analyzer, for example, HP4294A. In this case, precautions including correctly biased devices and a preceding calibration need to be taken: The measurement requires the switches to be in the off-state and derives the circuit inductance and capacitance from an LRC resonant circuit. Therefore, the gate-source

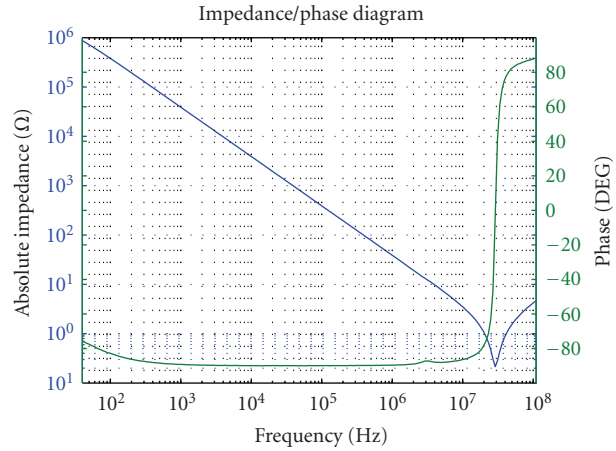


Figure 6: Impedance measurement plot DC+ to DC−.

Table 4: Inductance measurement using impedance analyzer HP4294A.

	DC +-DC−	DC+-Out	Out-DC−
L	6.69 nH	2.52 nH	2.24 nH
f_{res}	29.16 MHz	38.05 MHz	40.34 MHz

contacts of the MOSFETs are shorted and the antiparallel diodes are biased with a negative voltage; see Figures 6 and 7.

Table 4 contains the results for the flip chip demonstrator. Compared to the technique described in Section 3.2, the error introduced is higher since the capacitances of the chips and the stray inductance are spatially distributed. The measured capacitance includes the MOSFET and diode capacitances as well as the package capacitance. All concurrent paths are measured, resulting in a lower measured inductance that is composed of the parallel inductances of the diode and MOSFET current paths. Therefore, this technique is not suitable for multichip modules, as it does

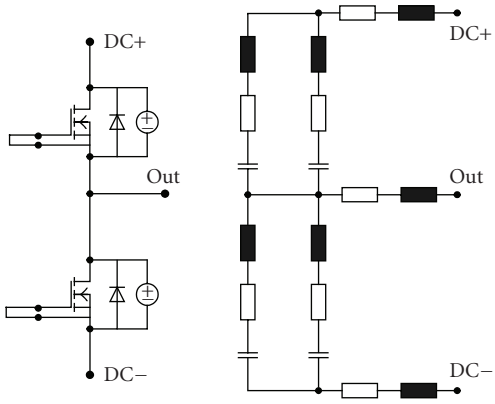


Figure 7: Test circuit and equivalent circuit of the assembly.

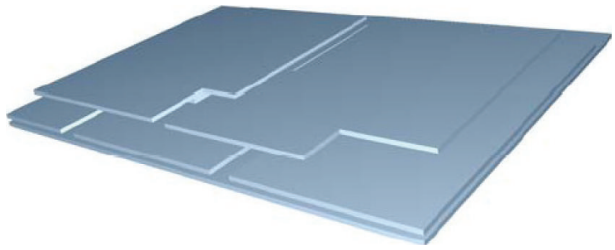


Figure 8: PEEC model of the FC half-bridge assembly.

not reflect the relevant current path. Figure 7 shows a model for the distribution of parasitic passive components.

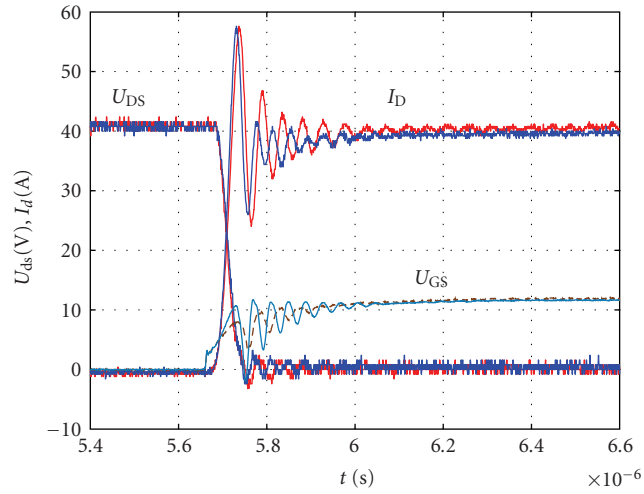
4. NUMERICAL CALCULATION OF THE STRAY INDUCTANCE

Commonly, "partial element equivalent circuit" (PEEC) as well as combined PEEC- and FEM-methods (Maxwell Q3D Extractor) are applied for the calculation of partial self and mutual inductances of electrical geometries, for example [14]. Here, the FC demonstrator is modeled with the software "FastHenry" [15]; see Figure 8. Planar conducting structures are used to account for the 2-dimensional current flow. The total package inductance DC+ to DC− is calculated to 8.64 nH at low frequencies and shows good agreement with the measured results. Skin and proximity effects are not considered in the result for comparability with the measurements but can be taken into account for a more detailed circuit simulation.

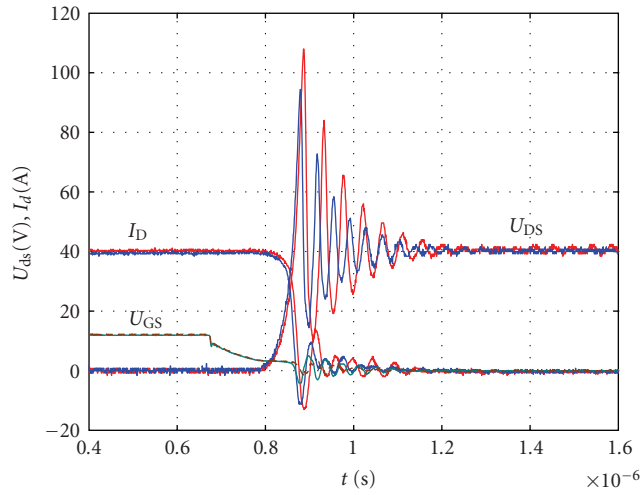
From the simulation, the DC resistance is calculated to 3.8 mΩ, which is also in good agreement with the measurements.

5. IMPACT OF THE STRAY INDUCTANCE ON THE SWITCHING CHARACTERISTICS

In order to analyze the impact of the stray inductance, the switching characteristics of the flip chip demonstrator is first measured in the optimized low-inductive test circuit. Even in this case, the inductance of the flip chip assembly (8-9 nH) is quite low compared to the inductance of the total circuit



(a)



(b)

Figure 9: Impact of the stray inductance on the measurements, $R_G = 5.6\,\Omega$; blue: FC assembly, red: Add. stray inductance; (a) turn-on (b) turnoff.

(26 nH). In a second step, an additional inductance of 10 nH is introduced into the circuit to simulate a chip and wire assembly. Exemplarily Figure 9 depicts two measurements switching 40 V and 40 A with a gate resistance of $R_G = 5.6\,\Omega$ in the buck converter test circuit given in Figure 3.

In the following, the impact of the increased stray inductance on the voltage overshot and on the switching losses will be discussed.

5.1. *Voltage overshoot during switching*

Figure 10 shows the voltage overshoot as a function of the load current with the gate resistance as parameter. The dashed lines represent the measurements with the increased stray inductance. The voltage limit is set to the rated voltage of 100 V, avalanche operation is not tested here. The increase in voltage overshoot is basically in the range of

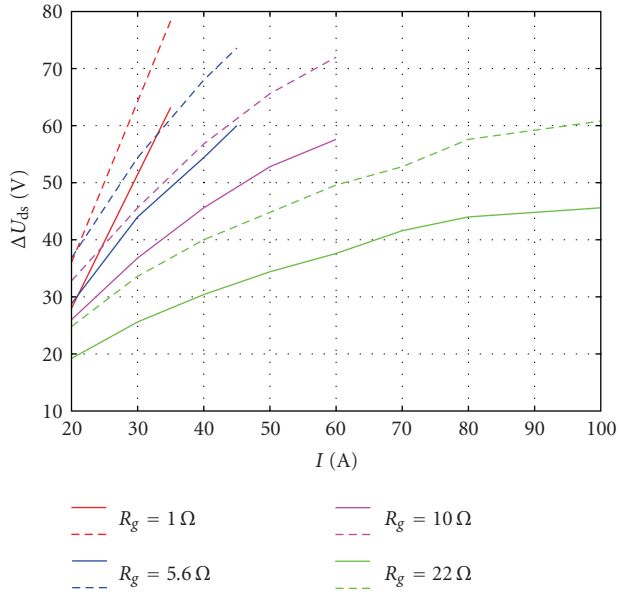


FIGURE 10: Voltage overshoot as a function of the stray inductance. Dashed lines: additional stray inductance of 10 nH in the circuit.

25–30% for the increase of the total stray inductance of approximately 40%. This clearly shows the benefit of higher chip utilization due to a better voltage rating achievable with a planar package with reduced stray inductance. As the voltage overshoot is superimposed by a damped oscillation and switching speed varies with load current, there is no linear relationship between current or stray inductance and overvoltage.

5.2. Switching energies

Apart from the on-state resistance, for high-frequency applications also switching losses of MOSFETs are relevant for the power losses. In the datasheets, basically turn-on and turnoff switching times for resistive loads are given. Usually, from these datasheet values, the switching energies are derived according to $E_{sw} = 0.5 \cdot U_d I_d (t_{rise} + t_{fall})$.

Alternatively, the switching energies can be extracted more exactly from the double-pulse measurements allowing to analyze the impact of the stray inductance on the switching losses. The switching losses are determined varying gate resistance and load current. The load current is increased until a voltage limit of approximately 100 V is reached. Figure 11 shows the typical increase of switching losses with increasing gate resistance as switching speed is lowered. Turnoff losses are approximately 15% higher with higher stray inductance due to the voltage overshoot. Turn-on losses are lowered up to 25% as current rise time is limited by the stray inductance. In summary the switching losses are slightly affected by the stray inductance leading to around 5% lower losses with lower stray inductance, since turnoff losses are dominant. As switching speed decreases with higher current due to the miller effect, there is also a nonlinear increase

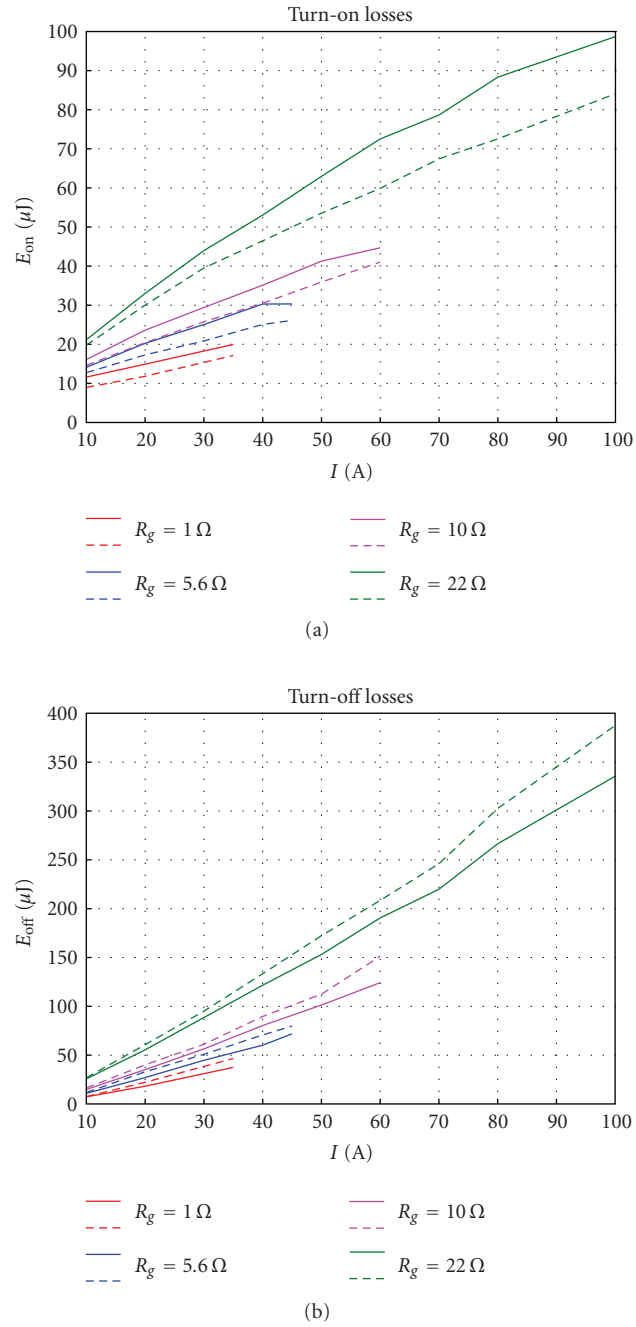


FIGURE 11: Switching losses for different gate resistances at (a) turn-on and (b) turnoff. Dashed lines: additional stray inductance of 10 nH in the circuit.

in switching losses at higher current levels, especially with higher gate resistances.

Figure 12 depicts a comparison of switching and on-state losses in a DC/DC converter with 50% duty cycle at different switching frequencies. The calculation is based on the switching losses measured with a gate resistance of 5.6 Ω. A linear extrapolation is done for the switching losses at higher current levels. This leads to underestimated switching losses at high current levels, as discussed before.

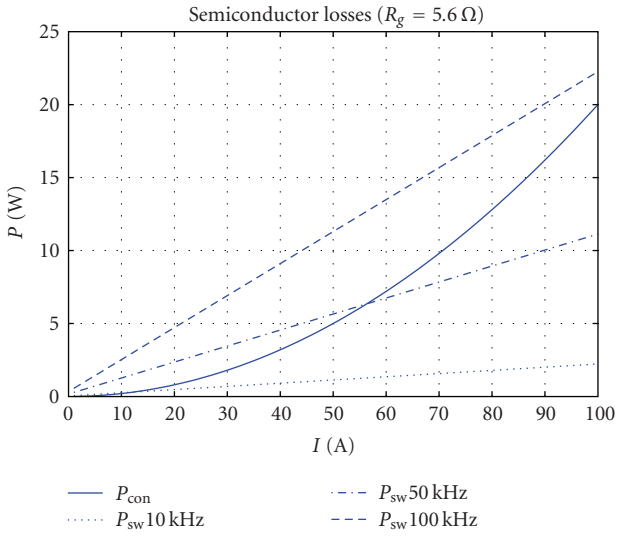


Figure 12: Conduction losses and switching losses at 50% duty-cycle, $R_G = 5.6\,\Omega$.

At lower frequencies in the 10 kHz range, the losses are dominated by the on-state losses due to the MOSFETs and package $R_{DS,on}$. With higher switching frequencies up to 100 kHz, the switching losses increase and dominate the power losses of the system. For the given devices, the impact of the stray inductance is not relevant for the loss calculation.

6. SUMMARY

In this paper, the impact of a reduced package stray inductance on the switching performance of fast power MOSFETs is discussed applying advanced 3D packaging technologies. Starting from an overview over new packaging technologies, a solder bump technology using a flexible PI substrate is exemplarily chosen for the evaluation.

Measurement techniques to determine the stray inductance of the package are discussed, showing that accurate results may be achieved applying an externally switched current approach while double-pulse measurements and the use of an impedance analyzer are not feasible for the package characterization. Good agreement with a numerical solution based on the PEEC method is found.

The relevance of a low stray inductance for fast switching MOSFETs is obvious from the measurement of the voltage overshoot allowing operating the new device at significantly higher DC voltages—up to 25%—than standard packages. The impact on the switching losses, however, was found to be less pronounced due to the reduced losses at turn-on.

As an additional benefit, also the package resistance is reduced compared to standard housing while at the same time larger copper areas substituting the wire bonds are able to carry higher amounts of current. This thermal aspect is discussed further in [13].

ACKNOWLEDGMENT

Part of the work has originally been presented at the IEEE PESC Conference 2007 [13] and the EPE Conference 2007 [16]. This article gives a comprehensive summary of the results.

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