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HYBRID-INTEGRATED SERIES-TO-PARALLEL CONVERTERS FOR GIGABIT RATES

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The generation and processing of data signal sequences in the gigabit range make high demands on circuitry and technology. For this high-speed thick-film switching circuits have proved successful. With a suitable circuitry, which is tailored to both the requirements of the subnanosecond range and the conditions of the thick-film technique, it is possible to solve many problems connected with the generation and processing of data signals in the gigabit range.

The conventional method of series-to-parallel conversion with shift registers can, however, not be applied at justifiable costs with the present-day components. Therefore signal processing at the receiving end by bit error rate measuring equipment at bit rates from 640 Mbit/s up to 1,28 Gbit/s is used to demonstrate hybrid-integrated thick-film circuits which, in connection with coaxial and strip lines, allow the series-to-parallel conversion of high bit rates.

The principle applied here uses lines as storing elements and high speed gates as switches. By supplying the data signal as well as the shift and sampling clocks in a serial mode, it is possible to obtain a geometrically linear arrangement of the thick-film circuits so that problems of clock supply and differing signal delays can be excluded. The combination of a few extremely high-speed thick-film circuits with commercial monolithic circuits allows series-to-parallel conversions to be performed in a simple, reliable and flexible way and in any conversion ratio.

1. INTRODUCTION

The generation and processing of data signal sequences in the gigabit range is at present still mostly confined to research projects having broadband communication systems as a goal.[1–3] Basic problems have to be solved by appropriate technologies and circuitries. The monolithic integrated circuitry must still be ruled out because of too long signal delay times, a classical design with discrete components fails as a result of stray inductances and capacitances. On the other hand, the high-speed thickfilm switching circuits, where all passive components are integrated and the active components are inserted into the completed circuit, have proved successful. With a suitable circuitry, which is tailored to both the requirements of the subnanosecond range and the conditions of the thickfilm technique, it is possible to solve many problems connected with the generation and processing of data signals in the gigabit range.[4–5]

In the Research Institute of the Deutsche Bundespost a number of broadband bit error measuring sets were constructed, which cover the range between 160 Mb/s and 1.28 Gb/s.[6] These high bit rates are obtained on the transmit side by multiplexing for instance 4 bit streams of a relatively low bit rate (e.g. 320 Mb/s) into 2 bit streams with double the bit rate (640 Mb/s) and these then into the final bit rate of 1.28 Gb/s. On the receive side this signal is demultiplexed and further processed. The first stage of the receiving equipment must therefore be a demultiplexer which is capable of series-to-parallel converting, for instance, a 1.28 Gb/s data signal into 4 signals of 320 Mb/s each.

2. PRINCIPLES OF SERIES-TO-PARALLEL CONVERSION

In general a series-to-parallel converter consists of a linear shift register, in which the data signal is written in serially and read out in a number of parallel sub-signals corresponding to the number of shift register stages. These sub-signals are then read into a latch. This method requires fast shift register and memory stages which at the present time can be operated safely only up to 600 MHz with monlithic Si-circuitry. A hybrid design would involve too much technical expense because of the great number of components required, especially for the shift register stages. The shift and sample clocking could not be solved satisfactorily without considerable expense because these clocks have to be applied to all stages simultaneously and with the same amplitude.

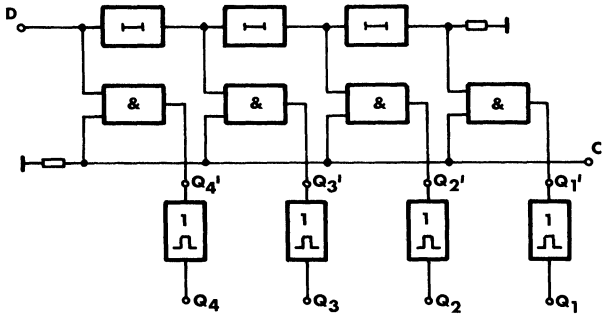

FIGURE 1 Series-to-parallel converter for 640 Mb/s with parallel clock. Length of delay lines is 1.56 ns.

For the series-to-parallel conversion of extremely high bit rates the active memory cells were therefore replaced by passive components in connection with hybrid logic gates. The gates have a simple design, need only few components, can thus also be constructed sufficiently small in hybrid circuitry and reach, with the same components, considerably higher switching speeds than memory cells. Since the mentioned bit error measuring equipment works at certain fixed frequencies, it is also possible to use coaxial or printed strip lines as passive stores.

Figure 1 shows a series-to-parallel converter demultiplexing a data signal at a bit rate of 640 Mb/s into 4 signals at 160 Mb/s each. The serial input signal runs from input D via 3 delay lines to a termination.

The delay lines have a delay time of

$$\tau = 1/f_b = 1.56\ ns$$

(f_b = 640 MHz = bit following frequency). Via AND-gates in the rhythm of the sample clock (160 MHz, duty factor 1:4), the information is taken from the passive store and passed on to the output terminals Q_1 to Q_4 after having run through oneshots. The oneshots bring the short input pulses (about 780 ps half width) to a sufficient width for further processing at 160 Mb/s (6.25 ns). By choosing the delay time τ, 4 successive bits of the data signal are passed on per sample clock so that at output Q_1 for instance bit 1, 5, 9 . . . , at Q_2 bit 2, 6, 10 . . . , at Q_3 bit 3, 7, 11 . . . and at Q_4 bit 4, 8, 12 . . . appear. The mode of operation of the circuit thus corresponds to that of a normal shift register.

The implemented circuit is shown in Figure 2. The delay lines are printed 50-ohm strip lines which are accommodated together with the 4 AND-gates on a 2 in. by 2 in. substrate. For the pulse lengthening the signal delay times of monolithic MECL-III gates are utilized.

The higher the bit rate of the data signal, the more difficult becomes the implementation of the converter circuit according to Figure 1. This is for two reasons: Firstly the data signal is attenuated and delay-distorted when passing through the 3 delay lines and secondly it involves more and more expense to

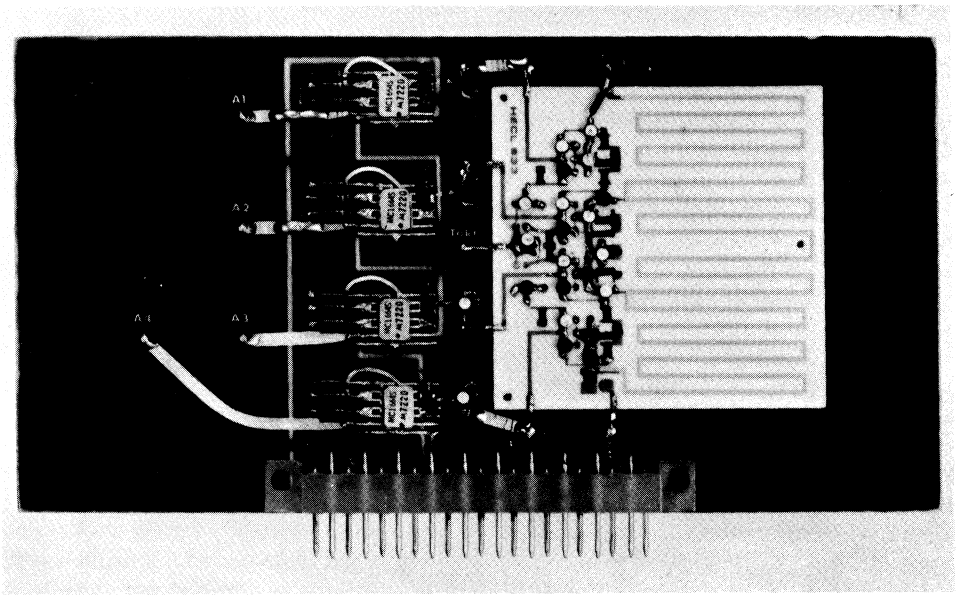

FIGURE 2 Series-to-parallel converter for 640 Mb/s. Size of the thickfilm circuit is 2 in. by 2 in., delay lines are printed strip lines. RF-connectors are mounted on the rear side.

supply the sample clock to all AND-gates with sufficient amplitude and without delay differences. These difficulties can be reduced with a circuit according to Figure 3 by connecting the clock serially in opposite direction to the data signal. This reduces the total delay of the data signal to one half and the clock supply becomes uncritical. The total circuit can be geometrically linearly expanded, the maximum distance between two adjacent AND-gates being only limited by the length of the delay lines.

Each delay line DL_1 to DL_6 has the delay time

$$\tau = 1/2f_b$$

For f_b = 960 MHz, τ = 520 ps, the sampling is done at 960:4 MHz = 240 MHz at a duty factor of 1:4.

The circuit operates as follows: The first 4 bits of the data signal arrive at point D in the sequence 1,2,3,4. We assume that at the time t_0, bit 1 has reached the output of delay line DL_3 and that simultaneously a clock pulse appears at input C. Bit 1 and the clock are combined in AND 1, output Q_1' assumes the logic value of bit 1. At the time $t_0 + \tau$, bit 2 and clock are at AND 2, Q_2' assumes the value of bit 2. At $t_0 + 2\tau$, bit 3 and clock meet at AND 3 and at $t_0 + 3\tau$, bit 4 and clock meet at AND 4. During the time between $t_0 + 4\tau$ and $t_0 + 7\tau$ no logic operation is possible because the next clock pulse does not appear at input C before the time $t_0 + 8\tau$, but at the same time bit 5 appears at the output DL_3, the first of the next group of 4 bits to be processed.

The output signals Q_1' to Q_4' of the series-to-parallel converter have a half-width of about 520 ps and are in oneshots brought to a width of about 2 ns for further processing at 240 Mb/s. The 4 output signals do, however, have a mutual delay of τ. If this causes timing problems in the further processing, an equalization must be made via subsequent delay lines DL_7 to DL_9, i.e. bit 1 must be delayed by 3 τ, bit 2 by 2 τ and bit 3 by τ. This delay is most easily achieved by connecting the series-to-parallel converter with the following circuit via lines of different lengths.

The oscillograms of a circuit according to Figure 3, which was, however, operated at 1.28 Gb/s, are represented in Figure 4 for one of the 4 outputs, where for practical reasons the logic "1" is assigned to a negative voltage. The first line from the top is the 1.28 Gb/s data signal at input D (a pseudo-random pulse pattern), the second line is the sample clock C. The resulting output signal Q' consists of each 4th bit of the input signal and is shown in the third line. The lengthened output signal Q with the bit rate 320 Mb/s is line 4.

Figure 5 shows the implemented circuit. One AND-gate and one oneshot each are integrated on a substrate of 1 in. by 0.75 in. The delay lines are constructed as 50-ohm coaxial lines and connected to the circuit from the rear side of the board.

Although it is also possible to operate the circuit according to Figure 3 at bit rates above 1 Gb/s, the advanced monolithic circuitry has allowed a better solution by which the number of passive elements can be reduced to one third and that of the active hybrid circuits to one half (Figure 6). The matching problems between delay line (delay time 390 ps at 1.28 Gb/s) and logic gates are thus diminished and a further increase of the controllable bit rate is possible.

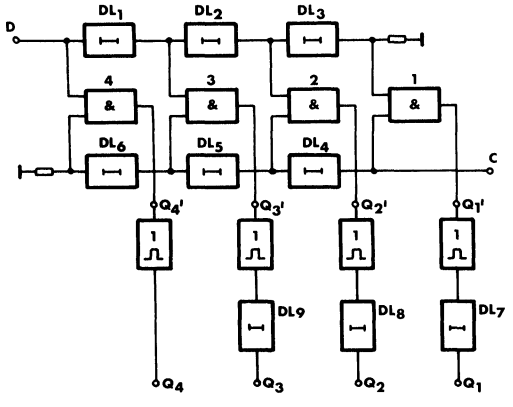

FIGURE 3 Series-to-parallel converter for 960 Mb/s. Clock runs serially in opposite direction to the data signal. Length of delay lines 1 to 6 is 520 ps, of DL_7 is 1.56 ns, of DL_8 is 1.04 ns and of DL_9 is 520 ps. This circuit can also be operated at bit rates of up to 1.28 Gb/s.

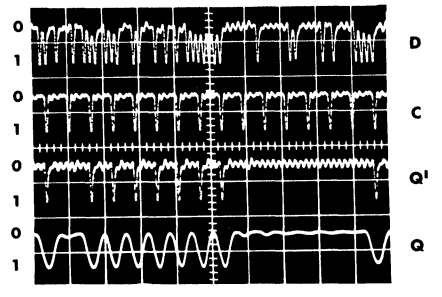

FIGURE 4 Oscillograms of Figure 3 circuit. Data signal D is sampled by clock C. Output Q' is broadened to Q. Horiz.: 5 ns/unit, vert.: 1 V/unit.

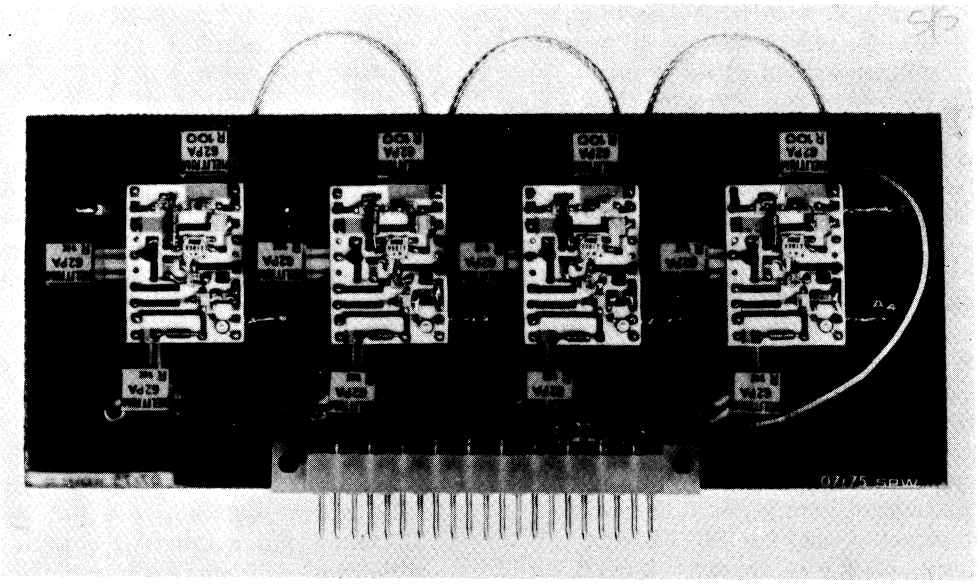

FIGURE 5 Series-to-parallel converter for 960 Mb/s. Size of the thickfilm circuits is 1 in. by 0.75 in., delay lines are coaxial cables, soldered directly on the rear side.

This series-to-parallel converter in Figure 6 demultiplexes in two steps; the input signal at D (e.g. 1.28 Gb/s) first is demultiplexed according to the previously described method with the aid of sampling clock C_1 (640 MHz, duty factor 1:2) into 2 parallel bit streams of 640 Mb/s each, which appear at outputs $Q'_{1/3}$ and $Q'_{2/4}$. After pulse lengthening and equalization of the different delays the signals at $Q_{1/3}$ and $Q_{2/4}$ are transferred to 2 D-flipflops connected in parallel, which are operated with anti-phase rectangular clocks C_2 (320 MHz). In this way 2 signals at 320 Mb/s are obtained from one 640 Mb/s signal. The oscillograms in Figure 7 illustrate this operation. The 1.28 Gb/s signal at input D of the first line yields, in connection with sampling clock C_1 of the second line, the broadened 640 Mb/s signal $Q_{1/3}$ of the third line (in the Figure this signal appears inverted). $Q_{1/3}$ consists of the bits 1,3,5,7... of the input signal. At output Q_1, there appears only each second bit of signal $Q_{1/3}$, that means for instance bits 1,5,9... of signal D. Because of the operating mode of a D-flipflop, Q_1 has the NRZ-form.

Figure 8 shows the implemented circuit. On the

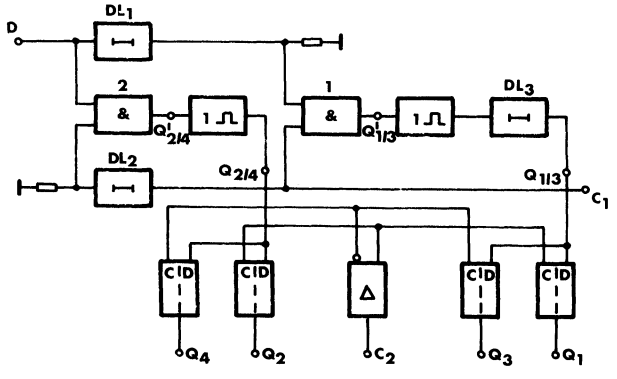

FIGURE 6 Series-to-parallel converter for 1.28 Gb/s. Demultiplexing is done in two steps. Length of delay lines is 390 ps.

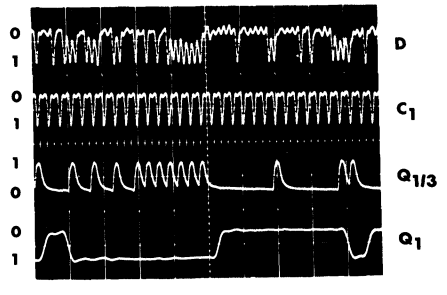

FIGURE 7 Oscillograms of Figure 6 circuit. Data signal D and clock C_1 produce output $Q_{1/3}$. The second demultiplexing yields Q_1. Horiz.: 5 ns/unit, vert.: 1 V/unit.

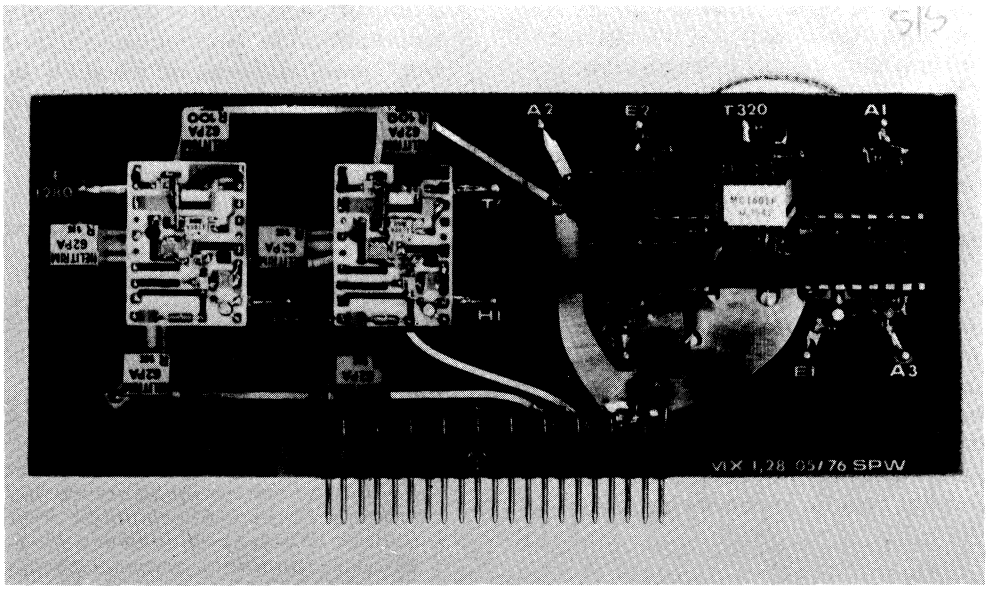

FIGURE 8 Series-to-parallel converter for 1.28 Gb/s which demultiplexes in two steps. The second step from 640 Mb/s to 320 Mb/s is done by monolithic flipflops.

left, one recognizes the two hybrid AND and pulse lengthening circuits and, on the right, the 4 monolithic *D*-flipflops and the clockdriver. The delay lines DL_1 to DL_3 are attached to the rear side of the board and consist of a teflon-insulated 50-ohm coaxial cable.

3. CIRCUIT CONSTRUCTION

Figures 2, 5 and 8 show the method chosen for the circuit construction. The thickfilm circuits are not encapsulated, but directly mounted to etched circuit boards on which also all other components, such as monolithic circuits, coaxial lines and RF-plugs are accommodated. This has the advantage of a compact construction and leads to short line lengths. In principle, all signal-carrying lines have 50-ohm terminations. On thickfilm circuits and etched boards use is made of strip lines and between different etched boards of coaxial lines. The connectors visible in the Figures serve only for power supply, all other connections are established by means of RF-plugs (SMA or SMC) being on the rear side of the etched boards.

For the thickfilm circuits use is made of Al_2O_3 substrates which are printed on both sides. All passive components, resistors, wiring, crossovers, capacitors and strip lines are printed, the semiconductors are soldered to the finished circuits. According to the complexity of a circuit, up to 7 layers (strip lines in gold, wiring in palladium-silver, 1 to 3 different resistance layers, 1 to 2 different dielectrics for crossovers and capacitors) are printed on the top side and 3 layers (ground layer, dielectric, power supply surface) on the bottom. Figure 9 shows as an example the masks for the individual fabrication steps of the thickfilm circuits in Figures 3 and 6. The ceramic substrate is drilled with ultra-sound (1), when

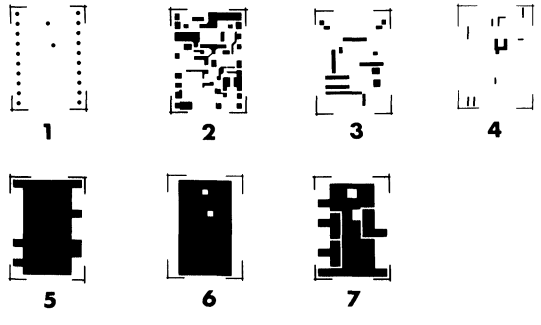

FIGURE 9 Thickfilm masks for the circuits of Figures 5 and 8. Masks 1 to 4 are for the front side, masks 5 to 7 for the rear side.

printing the wiring, the holes are plated through and they represent a very low-resistance and low-inductance connection of only 0.6 mm in length between the top and bottom sides. The wiring (2) is printed with a solderable palladium-silver paste. Afterwards the resistance print (3) and a glaze print (4) are made. The latter serves as a tin barrier when soldering the semiconductors.

The first print on the rear side (5) is the ground layer, it is the opposite electrode for possible strip lines on the front side and forms, in connection with the second rear side layer (6), which is a dielectric, and the third rear side layer (7), the metallic power supply surface, by-pass capacitors for the supply voltages. The strict separation of signal-carrying lines on the front side from large-surface, capacitively grounded power supply lines on the rear side ensures smooth decoupling even for extremely high bit rates.

4. SUMMARY

Series-to-parallel converters for gigabit rates can be constructed of passive stores in the form of lines and active circuits in the form of hybrid-integrated thick-film circuits. The combination of a few very high-speed, but simply designed thickfilm circuits and medium-speed monolithic flipflops represents the least expensive and most uncritical solution.

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