Electrocomponent Science and Technology
1977, Vol. 4, pp. 213–217

THE RELIABILITY, TESTING AND EVALUATION OF HYBRID MICROCIRCUITS

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(Received May 25, 1977; in final form June 22, 1977)

Reliability aspects of Hybrid Microcircuits are considered, including a prediction model illustrating the detail knowledge of the technology and application necessary. Circuit, part and element data is presented for two different test circuits. Use is made of predicted circuit failure rates to establish an electrical endurance test programme together with the thermal stress levels likely to generate some failures in an acceptable time. Results of testing the circuits at more than one temperature are presented, evaluated and compared with prediction. Failure analysis enables the performance of add-on parts, circuit elements and bonds to be assessed. A second series of test circuits confirms an improved bonding system. The usefulness of reliability modelling prior to endurance testing is justified together with some degree of thermal overstress.

1. INTRODUCTION

Hybrid microcircuits are usually custom-built and non-standard. Reliability considerations require knowledge of their technologies, complexity and quality of manufacture as well as their operating environment. Methods exist which use such detailed knowledge to predict their reliability.

A case history of a reliability test programme carried out on active thick film hybrid microcircuits is given. Use is made of reliability prediction in establishing the programme and evaluating the results of pre-production B.A.C. manufactured circuits.

2. RELIABILITY CONSIDERATIONS

Active hybrid microcircuits can be significantly more reliable than the equivalent assembly of discrete components for the following main reasons:–

1) The reduction in the number of electrical joints.
2) Use of a more stable substrate material.
3) Greater resistance to mechanical stresses.
4) The replacement of a number of packages by one capable of providing a dry gas environment for all circuit elements.

They can provide a wide range of electronic functions or sub-systems on a single substrate utilizing the inherent reliability of semiconductor devices. Thus there is a wide range of complexity and reliability.

A major reliability problem for a manufacturer of such circuits is the difficulty of controlling the quality of bought outside add-on chip components. He must also assure himself of the reliability of his wire bonding over the full temperature range quoted. Thermal considerations of the overall circuit packaging is important so that hot spots are minimised.

3. INITIAL TEST CONSIDERATIONS

Assuming that representative packaged circuits have passed appropriate climatic and mechanical tests, there remains a need for electrical endurance testing to demonstrate their reliability.

Some early considerations concern the number of circuits required for testing and the test time duration. Obviously, it is useful to be able to predict the rate of failure of the circuits with reference to their manufacturing standard and the test environment. A detailed prediction will be useful in assessing the results and some degree of confidence obtained in the prediction method – besides seeing that adequate test durations are established. Unfortunately, it is usually difficult to achieve as many component test hours as one would wish within the usual time, cost and availability constraints.

As a minimum, more than one failure should be predicted or experienced.

4. RELIABILITY PREDICTION MODEL

The following outlines the American Military Handbook 217B, "Reliability Prediction of Electronic Equipment"[1] method for predicting the failure rate of hybrid microcircuits. This defines the circuit failure rate λ_t in failures/10^6 hrs. as:–

$$\lambda_t = \lambda_b (\pi_T \pi_E \pi_Q \pi_F) \quad (1)$$

where λ_b = Base failure rate
π_T = Thermal stress factor, an exponential function of ambient temperature
π_E = Environmental factor
π_Q = Quality factor – obtained by considering MIL–STD–883 Quality Levels
π_F = Circuit function factor

Numerical values can be obtained for the above π factors. In the present work the environment factor was taken as that for a ground benign environment (0.2), the quality factor was interpolated to be between 883 Level B and C and taken as 5, and the circuit function factor given for Analogue Circuits is 1.0, for Digital circuits 0.8 and for a mixed A/D circuit 1.1.

The base failure rate itself depends on the number of circuit elements, added-on components and the technologies employed. It is given by:

$$\lambda_b = \lambda_{sub} + \lambda_{ac} + \lambda_p \quad (2)$$

where λ_{sub} = substrate contribution from bonds, printed elements, their density on the substrate and the substrate itself.
λ_{ac} = contribution from attached components
λ_p = small contribution depending on package type

The necessary data is available to enable the above to be quantified.

5. TEST CIRCUITS

Two typical circuit types were selected. One performed an analogue function and the other a combination function, predominantly digital.

The first circuit contained the following:–

1 Substrate 19 mm square, 96% alumina.
19 Thick film resistors (Du Pont 1000 series material).
3 Analogue i.c. chips.
5 Transistor and 11 diode chips.
3 Capacitor chips.
126 Ultrasonic bonds of 0.025 mm diameter aluminium wire.

In the first series of test samples, conductors were produced from gold ink of a fritted nature. For the second series a fritless gold ink was used. Its electronic complexity can be assessed from the fact that it includes some 57 transistor elements.

The second circuit contained the following:–

1 Substrate 19 mm square, 96% alumina.
11 Thick film resistors (Du Pont 1000 series material).
8 Digital i.c. chips.
2 Transistor and 1 diode chip.
272 Ultrasonic bonds of 0.025 mm diameter aluminium wire.

It has an electronic complexity of 50 gates or some 200 transistor elements. In both cases the substrate was soldered into a glass walled package resulting in a low thermal resistance from substrate to base. Thus there was very little temperature gradient between the package base and the substrate. The package was hermetically sealed with a dry nitrogen gas content.

6. TEST PROGRAMME AND METHODS

Reliability Predictions were made for the two circuit types using Handbook 217B,[1] for the maximum operating temperature classification of 125°C. The π values have already been discussed (section 4) and the λ values used in Eq. (2) were as below:–

λ	Analogue Function	Combination Function (digital/analogue)
λ_{sub}	0.03	0.04
λ_{ac}	0.35	0.15
λ_p	0.03	0.03
λ_b	0.41	0.22

All values quoted are at 25°C. An acceleration factor

must be applied to calculate the values at other temperatures. (Acceleration factor = 10 for 100°C; 18 for 125°C; 34 for 150°C; 61 for 163°C).

Predicted values obtained for failures per 10^6 hours are shown for various temperatures in Tables I and II.

The predicted figures suggested that the Mean Time Between Failures (M.T.B.F.) of the analogue circuit could be over 100,000 hours and that of the mostly digital circuit about 200,000 hours. Test durations should be such that the product of the test duration and the number of test samples should exceed 2 x M.T.B.F. for the appropriate temperature. Should the circuits prove much less reliable, then the tests could be terminated earlier. Consideration was given to a degree of thermal overstress testing by extrapolating the temperature/failure rate curve in the prediction model and also to testing at a lower temperature. As earlier bond evaluation had suggested there might be a wear out mechanism present above some 100°C, it was decided that a first series of tests would be carried out at three temperatures for each circuit.

To reduce the thermal resistance between substrate and ambient conditions ($R_{\theta.S-A}$), circuits were immersed in oil baths containing Dow Corning 200 silicone oil. This reduced ($R_{\theta.S-A}$) from 50°C per watt in air to 18°C per watt in oil, resulting in better control of the substrate temperature with the known possible variation in power dissipation from one circuit to another of the same type.

A thermal plot carried out on two analogue circuit substrates resulted in a maximum measured variation of 10°C across either substrate. This work was carried out by the U.K. Electrical Research Association as were investigations into failure mechanisms.

For endurance test purposes each circuit was connected to its individual printed wiring board. Forty boards could be accommodated in a rack positioned in an oil bath. Circuits were considered to have failed when not meeting their full specification whilst operating at 125°C. Full testing was carried out at regular intervals. When a failure was indicated whilst operating at temperatures above 125°C, the suspect circuit was retested at 125°C before being classed as a failure.

7. SCREENING OF TEST SAMPLES

Following normal production testing, all test samples were given a Sealing Test such that their leak rate was better than 5 x 10^{-7} atmospheres, cc. per second. The units were then subjected to a 48 hour operating burn-in test at 125°C. Final electrical testing enabled some marginal performance circuits or early failures to be removed before the start of the electrical endurance tests. (Some 6% were screened out for the Series 1 circuit; 0% for the Series 2).

8. CIRCUIT TEST RESULTS

Summaries of the results of the first test series are given in Table I.

Assessed failure rates are calculated as statistical best estimates for comparison with predicted values which must be considered as representing mean values.

Clearly the results show a bonding problem at temperatures above 100°C. Nearly all the bond failures concerned bonds to the fritted gold conductors and were very temperature sensitive.

Weibull plotting of bond life times demonstrated that for temperatures of 125°C and above three distributions of life times resulted.

1) An early failure period considered to be the result of the use of too low a bonding energy.

2) An interim period of reduced failure rate.

3) A wear out period of increasing failure rate for temperatures of 125°C and above.

TABLE I
Series 1 circuit test results and predictions

Circuit type	Sub. T°C	Number tested	Test (hrs) duration	Circuit hrs.	Failures		Failures per 10^6 hrs	
					Bonds	Total	Assessed	Predicted
Analog	100	31	12,000	362,000	0	1	4.4	4.1
Analog	125	31	11,250	252,000	8	10	41	7.4
Analog	163	20	2,000	28,100	12	14	510	25
Dig. Anal.	100	35	10,000	343,000	0	1	4.7	2.2
Dig. Anal.	125	40	10,000	334,000	6	9	28	4.0
Dig. Anal.	150	17	3,750	32,300	11	12	390	7.5

It was thus decided to carry out a second series of tests using conductors produced from fritless gold inks and with a tighter control of bonding energy. The same circuit types were used with circuits subjected to the highest test temperatures previously employed for each basic type. Summaries of the results of this second test series are given in Table II and III.

It will be seen that there was a dramatic reduction in bond failures especially when the increased number of circuit hours at the two highest temperatures are considered. The single bond failure occured early in the test period at about 888 hours. (Table II).

9. DETAIL COMPARISON WITH PREDICTION

Table IV and Table V give the detailed results of

TABLE II
Series 2 circuit test results and predictions

Circuit type	Sub. T°C	Number tested	Test (hrs) duration	Circuit hrs.	Failures		Failures per 10^6 hrs	
					Bonds	Total	Assessed	Predicted
Analog	163	40	5,300	203,000	0	2	13	25
Dig. Anal.	150	40	5,250	206,000	1	1	8.0	7.5

TABLE III
Extended Series 2 circuit test results

Circuit type	Sub. T°C	Number tested	Test (hrs) duration	Circuit hrs.	Failures		Failures per 10^6 hrs
					Bond	Total	
Analog	163	40	8,350	316,600	4	6	20
Dig. Anal.	150	40	7,650	298,000	3	3	12

(Cumulative data including that of Table II).

TABLE IV
100°C rationalised part test results and predictions

Part type	Part hrs. x 10^6	Number failed	Failures per 10^6 hrs (100°C)	
			Assessed from test	Predicted
Linear I.C. 723	4.4	6	1.5	0.50
Linear I.C. 741	2.2	1	0.75	0.54
Digital I.C.				
5400, 5402, 5410	5.3	1	0.31	0.13
5420	3.5	1	0.49	0.21
54121	1.8	1	0.91	0.15
5474	3.5	1	0.49	0.31
Transistors N.P.N.	10.1	0	0.068	0.11
Transistors P.N.P.	4.5	0	0.15	0.17
Switching diode	17.3	0	0.04	0.048
Ref. diode	8.9	0	0.08	0.22
Capacitor	6.7	0	0.10	0.004
Thick film resistors	61.5	0	0.011	0.005
Series 1 bonds	430	38	0.09	0.0005
Series 2 bonds	350	1	0.0046	0.0005

TABLE V
100°C rationalised part extended test results

Part type	Part hrs. x 10^6	Number failed	Failures per 10^6 hrs 100°C	
			Assessed from test	Predicted
I.C. 723	6.95	6	0.96	0.50
I.C. 741	3.48	1	0.48	0.54
Digital I.C.				
5400, 5402, 5410	7.72	1	0.21	0.13
5420	5.10	1	0.33	0.21
54121	2.62	1	0.61	0.15
5474	5.10	1	0.33	0.31
Transistors N.P.N.	15.4	0	0.045	0.11
Transistors P.N.P.	7.11	0	0.095	0.17
Switching diode	27.2	0	0.025	0.048
Reference diode	14.1	0	0.048	0.22
Capacitor	10.6	0	0.062	0.004
Thick film resistors	94	0	0.0072	0.005
Series 2 bonds	525	7	0.014	0.0005

(Cumulative data including that of Table IV). (The beginning of bond wearout at $T \geqslant 150°C$ is suggested after about 7000 hrs.)

testing, statistical estimation of failure rates and comparison with prediction. Part Type hours are rationalised to 100°C substrate temperature by using the relative predicted acceleration factors for temperatures above 100°C. The number of failures are those experienced.

These summary tables show that all failures were either bonds or integrated circuit chips. Results suggest that bonds are improved by more than 1 order at 100°C with a greater improvement at higher temperatures for durations up to at least 5,000 hours. (Table IV).

10. CONCLUSIONS

The desirability of high temperature operational testing of pre-production hybrid microcircuits has been confirmed together with the usefulness of prediction methods such as those found in MIL-HDBK-217B Section 2.1.7., currently under review.

Some reservations of the 217B method concern the Thermal Stress factor and its equal application to all circuit elements, and the difficulties in estimating the very sensitive quality factor unless standard American Screening and Quality Conformance procedures are employed.

Predictably, attached integrated circuits should represent the major failure contributions, especially if active hybrid circuits are not subjected to burn-in procedures.

Manufacturers of active hybrid circuits must assure themselves of the reliability of their bonding if the full reliability potential of their circuits is to be realised.

The bonding of aluminium wires to fritless gold conductors is considered to be more reliable than to fritted gold.

REFERENCES

1. Military Standardization Handbook (MIL-HDBK-217B), "Reliability Prediction of Electronic Equipment", Dept. of Defence, U.S.A., Sept. 1974.