SOME ASPECTS OF MULTILAYER CERAMIC CHIP CAPACITORS FOR HYBRID CIRCUITS

W. NOORLANDER

Philips Elcoma Division, Eindhoven, The Netherlands

(Received June 23, 1977)

It is shown that both European and American standardization committees specify the dimensions in the same grid and that there is no standardization of the thickness in relation to the capacitance.

Of the ceramic dielectrics, special attention is paid to the instability of capacitance and losses of type II materials due to temperature and voltage treatment.

The conductivity of the inner electrodes determines the losses at 1 MHz in type I dielectrics. It is shown that the economically interesting partial replacement of Pd by Ag can cause an increase in the losses: other substitute metals seem more promising.

The last aspect discussed is the end terminations of the capacitors. In the case of silver/palladium end terminations the Ag/Pd ratio should be smaller than two.

1. INTRODUCTION

Multilayer ceramic chip capacitors (MCCCs, Figure 1) are an invaluable aid to efficient hybridization. This fact has been accepted by an increasing number of hybrid circuit manufacturers and, as a result, MCCCs are now to be found in a wide range of military and civil equipments. However, feedback from end-users does indicate that an explanation of certain facets of

MCCC development technology would give the user a better insight into the apparently unpredictable behaviour of MCCCs. The aim of this paper is to help the user to appreciate some design considerations before formalizing his hybrid circuit.

Again, emerging from feedback, the following properties are of importance and will be discussed:

a) Dimensions

FIGURE 1 MCCCs cutaway view.

- b) Electrical properties
- c) Inner electrodes
- d) End terminations.

2. DIMENSIONS

Initially, MCCCs were only used in highly professional fields; out of the hesitant growth of MCCCs a standardization of dimensions has been born. Both the EIA and IEC (the American and European standardization committees) now specify their preferred sizes in the same grid (Figure 2). When the size of a capacitor chip is quoted, the first dimension is length, i.e. from end terminal to end terminal. Dimensions are given in 10^{-2} inches, e.g. 0805: the length is 8×10^{-2} inches and the width 5×10^{-2} inches (2 mm and 1,25 mm respectively). For the thickness, only a maximum (1,9 mm) and a minimum (0,5 mm) value is specified.

It is noteworthy that to date there is no standardization of thickness specified in relation to capacitance. An end-user with a specific objective must therefore bear this point in mind when ordering MCCCs.

EIA	mm	IEC
0805	$2,0 \times 1,25$	0805
	$3,2 \times 2,5$	1210
1805	$4,5 \times 1,25$	1805
1808	$4,5 \times 2,0$	
	$4,5 \times 3,2$	1812
	$5,7 \times 5,0$	2220
2225	$5,7 \times 6,3$	

EIA = Electronic Industries Association.

IEC = International Electrotechnical Commission.

FIGURE 2 Preferred MCCC sizes.

3. ELECTRICAL PROPERTIES

The capacitance, C , is determined by:

$$C = \epsilon_0 \epsilon_r \frac{A}{T} n \text{ (F)} \quad (1)$$

in which:

$$\epsilon_0 = 8,856 \times 10^{-12} \text{ F/m;}$$

$$\epsilon_r = \text{dielectric constant;}$$

$$A = \text{electrode overlap area in m}^2 \text{ ;}$$

$$T = \text{the thickness of the dielectric layers in m;}$$

$$n = \text{the number of active layers.}$$

From Eq. (1) it can be seen that capacitance is directly proportional to the dielectric constant. In ceramic materials, the dielectric constant may vary from about 10 to 10,000 or more. Both EIA and IEC classify ceramic dielectrics as class (type) 1 or 2, with class 1 dielectrics occupying the lower end of the range to about 200.

Definitions of these classifications are as follows:

Class 1: Temperature compensating ceramic dielectric fixed capacitors of a type suited for resonant circuit or other applications where high Q and stability of capacitance characteristics are required.

Class 2: Fixed ceramic dielectric capacitors of a type suited for bypass and coupling applications or for frequency discriminating circuits where Q and stability of capacitance characteristics are not of major importance.

A characteristic of class 1 dielectrics is the variety of temperature coefficients of the capacitance available. Temperature coefficients between $P(+)$ 100 ppm/ $^{\circ}\text{C}$ and $N(-)$ 5600 ppm/ $^{\circ}\text{C}$ are possible, but to date in hybrid circuitry there is only a demand for P100 and NPO (neg. pos. zero).

End-user questions usually arise when class 2 materials are handled. The instability of these materials is dependent upon such factors as: temperature, time and the effects of d.c. and a.c. voltage on both the dielectric constant and the dissipation factor. These factors are so interrelated that independent discussion of each is difficult. To the end-user, a remarkable effect is the capacitance change as a function of time (aging).

Practically all class 2 dielectrics are based on barium titanate (BaTiO_3). Well known methods to control the properties of ceramic barium titanate are the application of additives to the material to prevent grain growth during firing. Another method is the partial substitution of barium and titanium oxide to shift the Curie temperature to the vicinity of room temperature to make use of the peak in the capacitance versus temperature curve (Figure 3). The Curie temperature is that temperature above which the ceramic has a cubic structure; below the Curie point the material has a tetragonal structure in which the

FIGURE 3 Capacitance vs. temperature Z5U characteristic.

c/a ratio is 1,01. This means that one of the crystallographic axes is 1% longer than the other two. This coincides with the splitting up of the crystals in domains of the same crystallographic orientation, as shown in Figure 4.

Fine crystalline dielectrics are those in which the crystal size is in the order of a domain, each domain being about one micron (no 90° domains).¹ For ceramic dielectrics with the X7R characteristic (see below), materials are usually chosen in which not

FIGURE 4 Domain structure in BaTiO_3 based ceramic.

only are the crystals very fine, but also the peak in $\epsilon(T)$ is suppressed by additives. The aging of the capacitance can be less than 1% per time decade (logarithmic scale).

The (re)orientation of the domain structure is influenced by the crystal size and the defect structure of the material. Figure 5 shows the capacitance of an X7R dielectric (specification: $C = \pm 15\%$ between -55°C and $+125^\circ\text{C}$) as a function of time. It can be seen that the aging rate is only 0,55%/time decade.

Figure 6 shows the capacitance of a Z5U dielectric (specification: $C = \begin{smallmatrix} +22 \\ -56 \end{smallmatrix}\%$ between $+10^\circ\text{C}$ and $+85^\circ\text{C}$) as a function of time. This is a material in which the

FIGURE 5 Capacitance and DF vs. time of a material with the X7R characteristic.

FIGURE 6 Capacitance vs. time of a material with the Z5U characteristic.

characteristic is achieved by the partial replacement of BaO and TiO₂ to shift the Curie temperature to the vicinity of room temperature. It can be seen that the aging rate of this Z5U dielectric is about 6%/time decade. Experiments were carried out to show the influence of heat and voltage treatment on the aging of capacity. Ten capacitors were each given a temperature treatment at 72, 500, 1000 and 2000 hours after the burn-in of the end terminals. This temperature treatment was at 250°C for five minutes to simulate soldering conditions. The conclusion was that with a temperature treatment above the Curie temperature, the capacitance is completely rejuvenated regardless of the duration of shelf life. This temperature treatment (i.e. soldering) has the same effect on the dissipation factor (D.F.). Ten other capacitors were subjected to approximately +350 V d.c. for one minute at the same time points. This treatment also has a rejuvenating effect on the capacitance, but not as complete as the heat treatment. It should be noted that either a.c. or d.c. voltages have a rejuvenating effect on both capacitance and dissipation factor.

4. INNER ELECTRODES

The firing temperature of the ceramic dielectrics, which is between 1200°C and 1400°C, and the oxidizing circumstances, compel us to use a noble metal with a high melting point. Another factor determining the choice of electrode material is the

kind of dielectric used. In ceramics in which no bismuth-containing compound is used palladium with its melting point of 1550°C is attractive.

The electrical properties are of course affected by the electrodes. The continuity of the electrodes has an influence on the spread of capacitance and the conductivity determines the series losses. The losses due to series resistance are given by:

$$\tan \delta = \omega R_s C \quad (2)$$

in which:

$$\begin{aligned} \tan \delta &= \text{dissipation factor;} \\ \omega &= 2\pi f \text{ (} f = \text{frequency (Hz));} \\ R_s &= \text{series resistance } (\Omega) \\ C &= \text{capacitance (F).} \end{aligned}$$

The electrode resistance is determined by grinding away one of the end terminations until the capacitor is short-circuited. It is then end terminated again. The resistance is measured by the four-point contact method as shown in Figure 7.

The square resistance is calculated as follows:

$$R_{\square} = \frac{V}{I} \times \frac{W}{1} \times N_s \quad (3)$$

in which:

$$\begin{aligned} R_{\square} &= \text{square resistance in } \Omega; \\ I &= \text{current in amperes;} \\ V &= \text{voltage over the chip.} \\ W &= \text{width of inner electrode} \\ 1 &= \text{length of ground chips} \end{aligned} \left. \vphantom{\begin{aligned} R_{\square} \\ I \\ V \\ W \\ 1 \end{aligned}} \right\} \text{in equal units;} \\ N_s &= \text{number of short-circuited layers.}$$

FIGURE 7 Four-point contact method of measuring electrode resistance.

The capacitance and losses of six experimental lots of NPO capacitors (500–1000 pF) were measured on a Danbridge 1MHz capacitance deviation bridge CB1, and the $R_{\square}$ of the electrodes determined. Figure 8 shows the dissipation factor plotted against the square resistance; the straight line shows the relative proportionality. The main contribution to losses at this frequency is the resistance of the inner electrodes

(the ceramic used is a secondary contribution). Internationally accepted specifications state that at 1 MHz the dissipation factor must be lower than 10×10^{-4} at a maximum capacitance of 1000 pF. With the rather arbitrary choice of a $R_{\square} < 100 \text{ m}\Omega$, this demand is amply fulfilled.

The price of the electrode material greatly influences the product price, particularly with high capacitances. Recent developments speak of a partial replacement of Pd by Ag.² From the point of view of firing, there is no objection as can be seen in the phase diagram, Figure 9, for instance in materials with a firing temperature of 1250°C, 50% of the Pd could be replaced by Ag. However, from the point of view of conductivity, there might be objections. As can be seen in Figure 10, the conductivity of a composition containing 60% Pd and 40% Ag is four times lower than that of palladium. In this case the calculated $R_{\square}$ in layers of 3 μm and 5 μm (in practice, the electrode thickness in MCCCs is between these values) is 120 m Ω and 80 m Ω respectively, although in practice Pd electrodes have an $R_{\square}$ of about 60 m Ω . Practical experience will have to show if electrode resistances are linearly proportional with specific resistances or not. One has to deal with the fact that the losses increase proportionately with frequency (Eq. 2). From the point of view of economy it is important to

FIGURE 8 Dissipation factor vs. square resistance.

FIGURE 9 The silver-palladium phase diagram.

aim at the replacement of precious metal electrodes by base metals, e.g. nickel or cobalt. There could be no objections to the use of these base metals on the ground of series resistance as can be seen from the table.

Comparative specific resistances

60% Pd/40% Ag	Pd	Pd	Ni
44 $\mu\Omega$ cm	11 $\mu\Omega$ cm	9,8 $\mu\Omega$ cm	7,8 $\mu\Omega$ cm

5. END TERMINATIONS

After a capacitor is made, there are three phases of its life to be considered: time on stock, mounting and the final functioning phase.

If soldering techniques are used to mount the capacitor on the substrate, the wettability of the end terminations and their resistance to molten solder (leaching) should be determined. During an MCCC's shelf life, its resistance to atmospheric conditions can have a major effect on the wettability.

If the capacitor is to be glued onto the circuit, the question is how the bonding strength of the connection is influenced by the surface state of the end termination (which may be oxidized or sulphurized after shelf life). This raises a second question: whether or not the series resistance is increased and, if so, by how much.

In the functioning phase, the quality of package sealing is of importance. In a partially sealed package (i.e. one still subject to atmospheric conditions), there will be the possibility of silver migration. Hermetically sealed packages raise a degassing problem of both components and mounting material, e.g. remnants of flux in the solder bond, solving media or softener in the glued contacts and absorbed moisture.

Summarizing, one can say that in the development of end terminations, one has not only to deal with the adhesive force between the metal layers and the

FIGURE 10 Electrical resistivity and temperature coefficient of silver-palladium alloys.

component,³ but also with:

- a) leaching in molten solder;
- b) silver migration;
- c) storage influence.

6. LEACHING

The leaching of the end terminations was investigated by dipping the chips in 60/40 tin/lead at 250°C for one minute. To increase the severity of the tests, the samples were coated with solder paste with an activated flux before being dipped.

It was proved that resistance to leaching increased with the Pd content; at an Ag/Pd ratio ≤ 2 , the results were satisfactory. Experiments were also carried out which showed that the solder resistance increases when pure silver is coated with electrolytic Ni, in accordance with DeMatos.⁴

7. SILVER MIGRATION

The migration problem was investigated by two experimental methods. The first was conducted under the following conditions:

Humidity: 95%
Voltage: 500 V d.c.
Electrode distance: 15 mm

In the second experiment, a method was chosen which was a closer adaptation for multilayer configurations. In this experiment, the voltage was 50 V d.c., the electrode distance 4 mm, and a drop of de-ionized water was carefully placed on the chip, avoiding contact with the end terminals.

The first series of experiments proved that a 5% replacement of Ag by Pd was sufficient to prevent migration. However, the second series, with condensation, proved that the Ag/Pd ratio should be ≤ 2 . In the second test it was also found that silver migration was not stopped by protecting the end terminations with an electrolytic Ni layer.

8. STORAGE INFLUENCE

During storage, oxidization and sulphurization of the end terminals can occur. As can be seen in Figure 11, the resistance against sulphur increases with the Pd content, although at an Ag/Pd ratio of 2 the optimum is not reached. Using an Ag/Pd ratio of 2, we there-

fore carried out the following tests:

- a) An accelerated oxidization test for 48 hours at 250°C in air.
- b) An accelerated moisture test for 6 days at 55°C using the IEC 68-2 test method. This method recommends tests for 16 hours at 55°C with 95-100% humidity, followed by 8 hours at room temperature. Six cycles were completed.
- c) Sulphidization tests for 24 hours in 50, 100 and 200 ppm hydrogen sulphide.

After each test, the electrical properties were measured and the solderability checked. After the 50 ppm H₂S test, a slight increase in dissipation factor was noted. After all other tests, including the 100 and 200 ppm H₂S tests, no changes in properties occurred and the solderability stayed excellent.

When Ag/Pd ratios > 2 are used, solderability after storage might give problems, but a heat treatment of around 900°C improves solderability.

The conclusion is that MCCCs with an Ag/Pd ratio ≤ 2 in the end termination can be satisfactorily

FIGURE 11 Sulphidation of silver-palladium alloys.

mounted using the techniques mentioned; a good shelf life is also guaranteed.

REFERENCES

1. G. H. Jonker and W. Noorlander, Grain size of sintered barium titanate, *Science of Ceramics I*, Academic Press (1962).
2. W. Payne and K. A. Hill, Pd/Ag compatible Z5U dielectrics for ceramic multilayer capacitors. Presented at the Fall meeting of the American Ceramic Society, November 2, 1976.
3. R. V. Allen, S. V. Caruso, L. K. Wilson and D. L. Kinser, Thermal expansion compatibility of ceramic chip capacitors mounted on alumina substrates. Presented at the International Microelectronic Symposium, 1972.
4. H. V. DeMatos, New end termination for ceramic chip capacitors. Presented at ISHM 1970 Hybrid Microelectronics Conference, Beverly Hills, California.

Figures 4, 10, 11 from *Palladium: Recovery, Properties, and Uses*, by Edmund M. Wise, Academic Press (1968).