A HYBRID THIN-FILM LOGIC CIRCUIT USING GALLIUM ARSENIDE FIELD EFFECT TRANSISTORS

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(Received July 15, 1977)

High speed systems demand faster logic than current silicon bipolar technology can offer. Hybrid or monolithic circuits using gallium arsenide FETs provide an answer. The FETs require careful handling if electrical or mechanical damage is to be avoided. The problems of bonding a large number of these devices to a thin-film circuit to produce a working hybrid logic element are discussed. Techniques for their solution are given with reference to a completed experimental hybrid circuit.

1. INTRODUCTION

The gallium arsenide metal-semiconductor field effect transistor (GaAs MESFET) has progressed very rapidly from the research laboratory to the market-place and is the key component in a wide range of low noise microwave amplifiers. Whereas silicon bipolar transistors are not suitable for applications at frequencies beyond 4 GHz, GaAs FET amplifiers work beyond 20 GHz.^{1,2}

There has been less discussion concerning use of the GaAs FET device in logic circuits, although its outstanding frequency performance makes it suitable for very high speed systems.^{3,4} The GaAs FET will enable information transmission rates to be extended upwards to speeds at which only Gunn-diode logic^{5,6} can be used. This will probably be at around 7 Gbit/s.⁷

The highest level of integration so far reported on a single chip of GaAs is a divide-by-eight logic circuit that works up to 4 GHz.⁴ Further progress in this area can be expected, in spite of the difficulty of the work and the low volume of applications. Consequently GaAs FET logic may be produced as hybrid circuits using readily available chip transistors. Certain limitations, such as restricted choice of transistor (particularly with regard to gatewidth), difficulty in electrically matching devices, poor thermal tracking, and the reduction in speed imposed by the relatively large size of the circuit, will have to be tolerated. Because high frequency performance must be good, thin-film is preferred to thick-film technology.

This paper reports on the practical experience

gained when fabricating a logic circuit using twenty FETs and four diodes on a thin-film hybrid circuit (see Figure 1).

2. THE LOGIC CIRCUIT

The most complex indispensable single element in a practical logic system is a master/slave bistable. It is equivalent to four simple gates. The logic circuit made aimed for this minimum required level of integration.

FIGURE 1 Fabricated logic circuit using 20 FET's and 4 diodes on a thin film hybrid circuit. (Substrate 1 in. square).

FIGURE 2 GaAs FET (Plessey GAT 2 device). (Chip size approximately $800\ \mu\text{m} \times 100\ \mu\text{m}$).

It is not easy to test a single high speed bistable so a circuit consisting of a master/slave D-type bistable incorporating logical feedback was made so that it could be run as a divide-by two circuit.

The electrical design and layout of the circuit will not be discussed here. Suffice it to say that resistor material of about 100 ohms/square was needed, which can be produced with thin film techniques.

The substrate used was 99.6% alumina, one inch square and 0.025 inch thick, with an as-fired smoothness of 3 to 4 microinch centre-line average on the A-face and 4 to 5 microinch CLA on the B-face. Three holes were drilled through the substrate in anticipation of the through-connections provided by three screws. After cleaning, the substrate was placed in an evaporator chamber and raised to 320°C . Using a pressure of less than 10^{-5} torr a film was evaporated from a 80:20 NiCr alloy wire source. When the resistor material was the required resistivity, evaporation ceased and the film was annealed at 320°C for 15 to 20 minutes. The temperature was reduced to 200°C before evaporating a thin film of gold. Similar films were deposited on the other side. The conductor and resistor patterns were generated on the A-face using standard photolithographic techniques. The first mask enabled the conductors (and the ground-plane on the B-face) to be built up by electroplating.

A short etch removed the thin gold. The second mask protected the resistor areas while the excess exposed NiCr was etched away. The thickness of the NiCr was 0.03 to $0.04\ \mu\text{m}$, and of the electroplated gold about $6\ \mu\text{m}$. The narrowest gold tracks were $100\ \mu\text{m}$ wide at the top and $76\ \mu\text{m}$ wide at the bottom, the corresponding width of the photomask being $88\ \mu\text{m}$.

The FETs themselves were Plessey GAT 2 devices

(see Figure 2). They are moderately priced, medium-performance GaAs FETs (minimum f_{max} of 8 GHz) with a $2\ \mu\text{m}$ gate length that probably do not realise the full speed capability of the substrate but can give creditable results.

In order to minimize costs, initial practice in general handling, die-attachment and bonding was obtained using mechanical samples supplied by the manufacturer.

3. GENERAL PRECAUTIONS

The GaAs FET is notorious for its fragility (electrical and mechanical). This is due more to users' familiarity with its robust bipolar counterpart than any fundamental weakness. Once correct handling is learnt, losses will be few and far between, and each one should be identifiable with a lapse on the part of the operator.

The fundamental consideration is that the FET (and in particular its gate, which can be destroyed by an energy spike of $30\ \text{nJ}^8$) should be protected from spurious transient electrical signals caused by mains-borne interference, static discharge or inductive pickup.

It is essential that in the course of circuit fabrication anything that is associated with a conducting path to the FET contact pads is solidly earthed to a star point. Care must be taken in the design to avoid forming earth loops. Any electrically powered equipment used in the fabrication or testing of circuits (e.g. bonders, curve tracers, power supplies) should only be plugged in via a substantial "mains filter" i.e. a radio-frequency interference suppressor. Where large currents are changing in nearby equipment (e.g. in large transformers, switching power supplies and induction ovens) there is a risk from inductive pickup. If possible the equipment should be moved away, but failing this the device and any leads to it should be shielded. Static discharge from human beings is another danger and earthed wrist-bands should be worn. If tweezers are used to work on a circuit, these should be wired to earth. Probes are similarly suspect, and our practice has been to mount them in insulating holders and earth them immediately prior to use.

Sources of transients are highly insidious and their influence is very difficult to measure. In practice the general philosophy must be one of overkill.

When handling the chips mechanically nothing should be allowed to touch the upper active layer of the device. An exception can be made for the vacuum

pickup of a die-attach machine but even this should be avoided if possible. The chip should be handled by its edge using a vacuum probe. Ideally the probe should have a teflon tip, but a metal tip can be used with little risk. Tweezers should only be used along the longer edges of the chip, and then only with extreme caution as quite small forces can cleave or break the crystal.

Excessive moisture on the surface of a FET can cause damage when normal voltages are applied. This should not be a problem in the development lab.

4. DIE-ATTACHMENT

GaAs FET manufacturers offer advice on die-attachment with their specification sheets. All manufacturers indicate that Au-Ge or Au-Sn preforms can be used, but we judged that the high temperatures required presented an unnecessary stress. An idea of the thermal treatment that can be tolerated by these devices can be gained from manufacturers' limits on temperature and time for this operation:—

- i) Plessey. Greater than 356°C but “not for prolonged periods”.
- ii) NEC. 400°C ± 20°C for not more than 3 s, or 300°C ± 20°C for not more than 5 minutes.
- iii) Hewlett-Packard. 320°C for not more than 30 s.

Much more attractive for development work is the use of low-temperature epoxy. Plessey specify Able-bond 41-1 as a preferred epoxy, NEC give no recommendations, while Hewlett-Packard do not mention the possibility of the use of epoxy.

The thermal resistance from chip to substrate should be at a minimum, requiring a very thin layer of epoxy with good thermal conductivity. Satisfactory results can be obtained with electrically-insulating epoxies, which also have the advantage of not prejudicing *r.f.* performance in any way. We have used Araldite, a general purpose epoxy from Ciba-Geigy, which cures in 30 min to 60 min at 80°C to 100°C. In practice the epoxy hardens sufficiently on the heated stage used in the subsequent thermocompression bonding, and the curing step is omitted. Also, as described later, by raising the circuit temperature to 150°C this epoxy can be softened enough for a chip to be easily removed. The remaining excess adhesive can then be scraped away and a new chip attached in its stead.

A simple die-attach machine is quite adequate. The adhesive can be applied to the substrate using an

epoxy dispenser or by hand using a probe tip, as preferred. Ideally the vacuum pickup should have a rectangular collet of the appropriate size and with corner relief. However, a suitable hypodermic needle can be used if its tip is flat, polished, and parallel to the substrate surface. This can be achieved with the help of successively finer grades of emery paper. Although the hypodermic did touch the corners of the active, mesa area of the device, the slight pressure necessary for the attachment did not perceptibly impair the electrical performance. Similar experience with GaAs IMPATT diodes, however, does suggest that this might affect the long-term reliability.⁹

5. THERMO-COMPRESSION BONDING

Although Hewlett-Packard do suggest ultrasonic bonding as an alternative it has occasionally been known to harm a device.¹⁰ However, all the manufacturers are happy with thermocompression bonding, and they recommend various combinations of wire diameter, stage temperature, tip temperature and bonding force. We have had good results using a ball-bonder with 0.0007 inch diameter half-hard gold wire, a stage temperature of 170°C (chip face at about 150°C), a tip temperature just below 200°C and a bonding force of 18 g. wt. These conditions stress the devices less than any of the manufacturers' recommendations, and do not appear to be particularly critical. Ball-bonds are made to the FET contact pads and two stitch-bonds (in anticipation of de-tailing) are made to the thin-film conductors. There was no sign of purple plague at the aluminium gate pads. Bond strengths were tested and ranged from 2 to 5 grams weight. The bonds always broke within the annealed portion of the gold wire fairly close to the ball-bond.

An important precaution (which experience suggests may be vital) is to ensure that FET contacts are bonded to parts of the circuit that are at earth potential.⁸ This means that an earth point on the top surface of the thin-film circuit must be arranged if necessary, and all the conductors on the circuit should be attached to this point by “safety” bonds before any device contact pads are touched at all. Normal bonding can then proceed. This circuit used four diodes in addition to the FETs, and wires could not be bonded directly to them. At this stage the opportunity was taken to apply conducting epoxy with a probe tip where the diode contacts and wires met. After a curing step the circuit was de-tailed using tweezers. Finally the circuit was “activated” by

removing all the safety bonds, starting with those furthest from the earth point.

6. CIRCUIT TESTING

As already mentioned any test gear used with FETs or FET circuits should have some protection from mains spikes. There is the additional hazard in a circuit that if one device is blown and supply voltages are applied indiscriminately, destructive voltages might appear across other devices. A fully-developed circuit will have some built-in protection, but exploratory work demands a careful approach.

All the test gear should be switched on and turned to zero supply volts before being connected to the circuit. It is best for the ground connection to be made first. Voltages can then be increased progressively, in steps, in an order which has been previously worked out and for which the consequent node voltages for all parts of the circuit are known. This scheme should be designed to keep gate voltages well below source voltages wherever possible. For initial test, the node voltages should be monitored as each step is made. Subsequently it is wise to use the same scheme whenever reconnecting d.c. supplies.

For testing we mounted the circuit on a copper block whose upper surface was gold-plated and identical in size to the substrate. The r.f. connections were made using SMA microstrip launchers bolted to the side of the block. The d.c. was supplied by wires which had access to the bottom of the substrate via a channel in the top of the block. By placing the assembly on a probe table it was a simple matter to monitor the d.c. node voltages using a DVM.

7. REWORKING THE CIRCUIT

If a device is blown it needs to be substituted in some way. The best approach is to remove the old device and put a working one in its place. The procedure below was followed.

i) Break the bonds to the device. It is quite easy to ensure the fracture is close to ball-bond, where the wire has been annealed. This leaves longer, easily detached ends bonded to the thin film conductors.

ii) Put the circuit on a heated stage at around 150°C. The Araldite will be fairly soft and gentle pressure at the junction between the longer side of the chip and the substrate will break the die-bond. This can be done by hand using, for example, the

blade of a jeweller's screwdriver, if care is taken to prevent overrunning.

iii) Excess epoxy can be scraped from the (cold) substrate if necessary.

iv) Proceed as before with die-bonding of the new chip.

It is quite possible to recover working devices from old circuits in this way. The recovered chip can be die-bonded afresh with little difficulty. The ball-bonds will interfere a little with the vacuum pickup but on the other hand will protect the surface of the device. When rebonding the device there is plenty of room on the source and drain pads next to the old ball-bond. For the gate, the alternative contact pad can be used although as a last resort one can bond to the top of the old ball-bond.

Such procedures carry an element of risk. Alternatively, it is possible to avoid removal of an old chip by scraping the bonds from its surface and attaching the new chip directly to the top of it. However, this will entail a thermal penalty, and may make the subsequent wire-bonding rather difficult.

In the development phase a circuit can withstand a surprising degree of reworking and brutal modification before it becomes unserviceable.

8. RESULTS

The work so far has enabled a fully-operational divide-by-two circuit to be made. Clock frequencies up to 550 MHz can be handled.¹¹

This result can be related to the 4 GHz performance of a monolithic GaAs FET logic circuit.⁴ By using better devices (produced as matched pairs with 1 μm gate lengths) and improving the layout of the circuit, the way to a three or four-fold speed improvement in the hybrid can be seen.

9. CONCLUSIONS

Despite the reputation of the GaAs FET for fragility it is quite possible to make and rework hybrid circuits using a large number of devices. Losses will be limited if the precautions outlined are followed.

ACKNOWLEDGEMENTS

The authors are grateful to S. O'Hara for his support and encouragement. K. I. Chaudry made the thin film circuits, and J. A. Turner gave useful advice on the FETs.

Acknowledgement is made to the Director of Research of the British Post Office for permission to make use of the information contained in this paper.

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