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HIGH DENSITY PACKAGING TECHNOLOGY

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A chip and wire, high density packaging approach has resulted in a low cost, large scale, high density, multi-chip package (MCP). The package includes 76 ICs, 1 resistor, and 34 capacitor chips on a 2 in × 3 in multilayer ceramic substrate (MLS) with 92 I/O leads. The package has a solder-sealed, metal cover over the chip-mount area, and a heat sink on the back side of the MLS.

The primary yield was found to be around 70%. The rest was reworked with no significant labour. The software as well as hardware to minimize the test/rework labour would be a key to success in chip and wire MCPs. Also, efforts were made to reduce the material cost and the assembly labour. The thick film MLS was replaced by the ceramic MLS. The wire bonding was automated. Overall efforts reduced package cost to 1.25 times the conventional DIP-on-PCB counterpart (7.5 in × 9.1 in). Estimating its effectiveness at a system level, the reduction in the number of boards, connectors and cables would give MCPs an advantage over their counterparts. The improvement in reliability would be another advantage

A comparison with other high density packaging technologies, chip carrier, and chip on tape, is also described.

1. INTRODUCTION

The increasing scale of electronic circuits, associated with system requirements for greater complexity and more multifunctions, is making it difficult to take the conventional, DIP-on-PCB approach for packaging devices into a limited physical volume. To solve this problem, the LSI technology and the high density packaging technology are used individually, or in combination. Though combined with LSI technology, high density packaging produces a multiplied packaging density effect. Even if used alone, it has merits of much lower cost and shorter period for development than the LSI.

Among the high density packaging techniques are chip and wire, chip on tape (or tape carrier), chip carrier, and flatpack, in the order of low packaging cost per chip. Packaging densities, compared with DIP on PCB (=1), are 6 ~ 12, 5 ~ 10, 3 ~ 4 and 1.5 ~ 2, respectively.[1] Namely, chip and wire technique makes it possible to achieve highest density and lowest cost packages. Chip on tape, comparable to chip and wire in packaging density, presently has disadvantages such as poor availability on the market, a vast sum of investment necessary for in-house processing, and less effectiveness in small and moderate production volumes.

However, it has been said that chip and wire hybrids become low yield and costly as the number of chips per package increases, since bare chips are unable to be tested prior to assembling.

The chip and wire method was considered to be the most effective high density packaging technology. The authors intended to develop a low cost, large scale, high density, multi-chip package (MCP), aiming at cost comparable to that for DIP-on-PCB.

2. APPROACH

A multi-channel counter circuit was chosen, including about 5,700 gates. The original board had 52 MSIs (16 pin), 24 SSIs (14 ~ 16 pin), 1 resistor and 43 capacitors on a 210 mm × 235 mm double-layer PCB.

In principle, a chip device would be substituted for a discrete device, on a one for one basis, and assembled on a 2 in × 3 in ceramic, thick, film multilayer substrate (MLS) using chip and wire technique. A metal cover/solder seal technique would be chosen for reworkability and reliability. As a dual-in-line form could not provide necessary 74 I/O leads with 0.1 in pitch for the substrate (56 leads max.), 92 leads, including unused leads, would be arranged on the periphery of the substrate in a flatpack form. 7 watts of power dissipation per substrate would require a heat sink on the back side of the substrate for forced cooling.

The built package is shown in Figure 1 in contrast with the original circuit board, and in Figure 2.

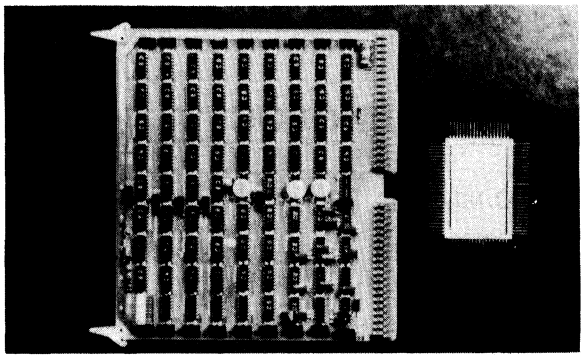

FIGURE 1 MCP vs. DIP-on-PCB per multi-channel counter circuit.

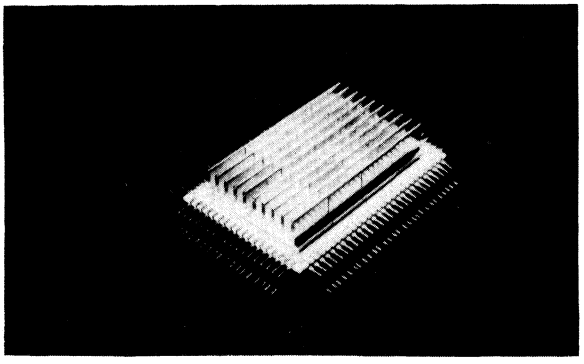

FIGURE 2 Multi-chip package.

3. PACKAGING

The overall package assembly, and the MLS structure are shown in Figure 3 and Figure 4, respectively.

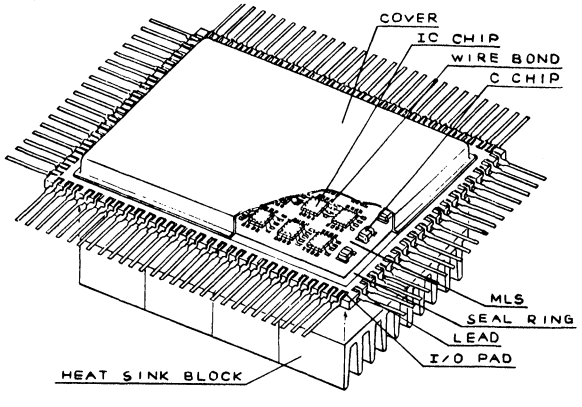

FIGURE 3 Multi-chip package structure.

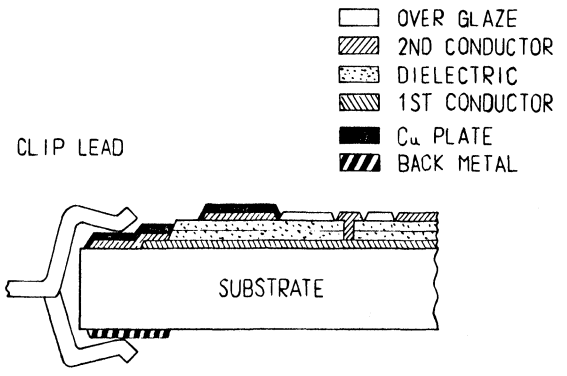

FIGURE 4 MLS cross section.

3.1. Multi-layer Substrate (MLS)

The ceramic substrate is 2 in × 3 in × 1.5 mm thick, 97% alumina. Multilayer thick film technology provides 2 gold conductor layers, 1 isolation layer, and 1 overcoat layer on the alumina. Conductor lines are 150 μm lines separated by 150 μm spaces, except for ground and power lines. A seal ring and I/O pads (2nd conductor layer), where soldered and copper plated to prevent the gold from leaching into the solder. On the back of the substrate, thick film Ag/Pd pads, corresponding to I/O pads on the top are provided for lead attaching.

The MLS is open/short tested by an automatic substrate tester prior to assembling.

3.2 Lead Assembly

The lead frame uses Tokyo Tanitsu T11116-D-13 edge clips. The MLS fitted with the lead frames is edge dipped into Sn10/Pb90 solder at 320°C, using Alpha 5002 flux.

3.3 Chip Assembly

IC chip dies and capacitor chips are bonded on the MLS using Epo-Tek H-20E conductive epoxy. Then, IC chips undergo thermosonic wire bonding with 30 $\mu m\phi$ gold wire. The chip assembled MLS is given its first test prior to sealing.

3.3 Hermetic Seal

The seal ring of the MLS and the seal area of a Kovar cover are presoldered with Sn63/Pb37 solder. After both are cleaned, a cover having a vent hole is attached to the seal ring by flux-less reflow soldering. Then

follows vacuum baking in 10^{-2} torr at 100°C for 30 minutes, processing a helium atmosphere in a glove box, and sealing of the vent hole with Sn63/Pb37 solder in the box. Hermeticity is tested using Veeco MS17 helum leak detector.

3.4 Heat Sink Assembly

Heat sinks divided in 8 blocks, each aluminum block is 16 mm × 20 mm × 12 mm high with 5 fins. Heat sinks are attached to the back of the MLS, using Castall 1520 epoxy adhesive. The heat sink is divided to relieve expansion and contraction stress on the MLS.

4. RESULTS

4.1 Performance

Performances of the MCP, compared with the original DIP on PCB assembly, are listed in Table I. The packaging area was reduced to 1/11. As the overall line length was shortened, the maximum clock frequency was improved to 1.3 times the DIP-on-PCBs.

TABLE I
MCP vs. PCB per multi-channel counter circuit (76 ICs)

	Size (inch)	F max. (MHz)	Number of bypass capacitors
PCB	7.5 × 9.1	20	27
MCP	2 × 3	26	17
MCP/PCB	1/11	1.3	0.6

4.2 Primary Yield and Rework

Generally, the package yield is given as a product of individual chip yields. The curves shown in Figure 5 give the defective percent for chips (D) necessary for producing a desired package yield (Y) vs. the number of chips per package (N). Assuming that the package yield limit is 60%, from the productivity point of view, the percent defective should be below the slanted line area in the graph.

The MCP (N = 76) resulted in 60–70% primary yield (D = 0.5 ~ 0.6%) in moderate production volume. The term 'primary yield' means the yield at the 1st electrical test.

In order that the 60% primary yield has no significant effect on the package cost, the rework labour for the

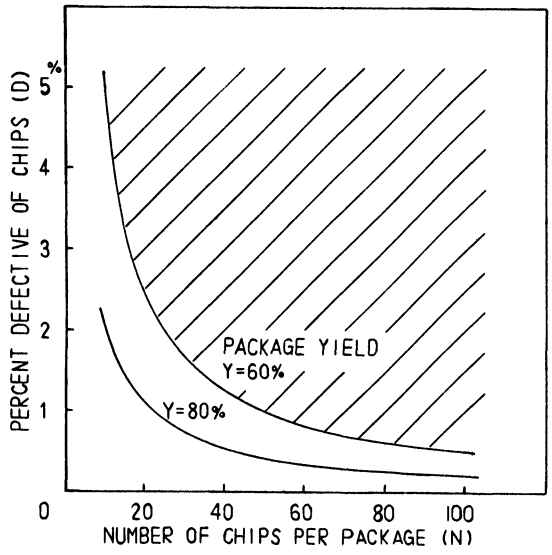

FIGURE 5 Percent defective of chips vs. number of chips per package at desired package yield.

40% should be minimized. The rework labour includes:

1) Testing and localizing a failed location
2) Replacing a chip

The test/localize labour was minimized using a microcomputer controlled auto-tester developed for the particular MCP. Epoxy die-bonded chip is easily replaced at elevated temperature.

As a matter of fact, most of the failed packages in the 1st test were repaired by 1 rework cycle with 1–2 chips replacement. Therefore, the secondary yield was almost 100%.

4.3 Final Yield

Sealed packages were submitted to a 70°C 96 hour aging test. The aging yielded about 5% of failure, including the initial ICs failure and the packages leak failure. After removing the solder sealed cover by reflow, failed packages are submitted to rework/repair. The rework/repair resulted in an almost 100% final yield.

4.4 Reliability

Reliability tests were conducted according to MIL-STD-883. Results are listed in Table II. It was found that the MCPs met at least condition A of the MIL-STD-883 requirements. The MCPs (cavity

TABLE II
Reliability tests per MIL–STD–883

Test	Method	Conditions	Result
Thermal shock	1011	1. 0°C to 100°C, 15 cycles	Cond. 2
		2. −25°C to 125°C, 15 cycles	Qualified
		3. −55°C to 150°C, 15 cycles	
High temperature storage		100°C, 2,000 hrs.	Qualified
Moisture resistance	1004–1	Vcc = 5V, 30 cycles	Qualified
Vibration	2007	20 ~ 2,000 HZ, 20 G	Qualified
Shock	2002	1. 100 G	Cond. 2
		2. 500 G	Qualified

Each qualification was made by both electrical test and leak test (reject limit is 2×10^{-7} atm. CC/Sec).

volume 8 cc) maintained at worst 10^{-8} atm cc/sec order of leak rate throughout the tests.

5. COST

Factors determining the cost of MCPs and the corresponding measures taken for cost reduction are listed in Table III.

Table IV gives a relative cost comparison among DIP-on-PCB, MCP/thick film MLS, and MCP/ceramic MLS on the realized cost basis. As a result of implementation of the measures listed in Table III, the MCP cost was reduced to 25% up the DIP-on-PCB's.

If the mechanization of the sealing process is implemented including review on the seal method, more cost reduction will be possible. Though the package cost was up 25% in comparison with the DIP-on-PCB costs, packaging space was reduced to 1/4 at the system level. When taking into account savings on

TABLE III
Cost reduction factors and measures

Factor	Measures for cost down
Substrate cost	Thick film multilayer → ceramic multilayer (reduce the quantity of gold)
Assembly parts cost	Gold plating → tin plating
Wire bonding labor	Manual bonder → auto bonder
Sealing labor	Semi/auto mechanization
Testing labor	Auto-tester
Rework/repair labor	Epoxy die bonding/solder sealing/auto-tester

TABLE IV
MCP/DIP-on-PCB cost comparison

	DIP-on-PCB	MCP/thick film MLS	MCP/ceramic MLS
Substrate	1	1.2	0.55
IC	1	1	1
Assembly labour	1	3.3	3.3
Total cost	1	1.43	1.25

boards, connectors, cables and main frame cost due to increase in circuit density per board, of the improvement in reliability of the package itself, and of maintenance ease, the entire cost would overtake the DIP-on-PCB cost in estimation.

6. KEY IN CHIP AND WIRE, HIGH DENSITY MULTICHIP PACKAGING

The important factor through the overall process would be how to reduce the test labour, and the software as well as the hardware techniques.

6.1 MLS open/short test

The MLS auto-tester, which had been developed in the author's group, is shown in Figure 6. A 16 bit minicomputer TOSBAC 40C was used as a controller and a data processor. 1,090 points per MLS were automatically measured in less than 10 minutes.

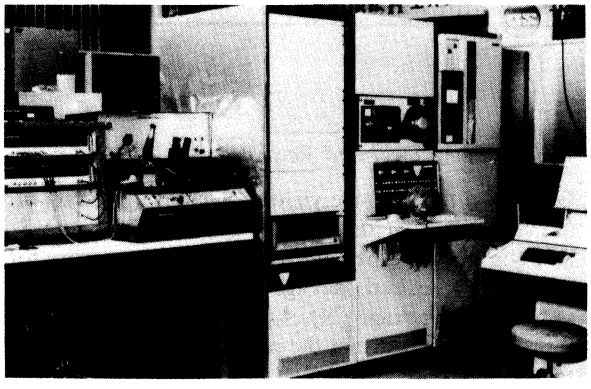

FIGURE 6 MLS auto-tester.

6.2 Package Function Test

The auto-tester, using an 8080 microprocessor, was developed for the particular MCP. The tester gives displays of GO/NO-GO and error steps. It is possible

to find an error location on the MLS with ease, consulting a provided error dictionary.

Required test labour will be further reduced by improving soft/hardware.

7. COMPARISON WITH OTHER HIGH DENSITY PACKAGING TECHNOLOGIES

Experience was gained years ago on a chip on tape (or TAB), high density packaging (110 max. CML TAB chips in a 80 mm × 80 mm MLS, see Figure 7). In recent years, chip carrier packaging has also been experienced (see Figure 8, TLCS-12A microcomputer unit). Chip and wire technology merits will be discussed in comparison with these other high density packaging technologies. A general comparison is given in Table V.

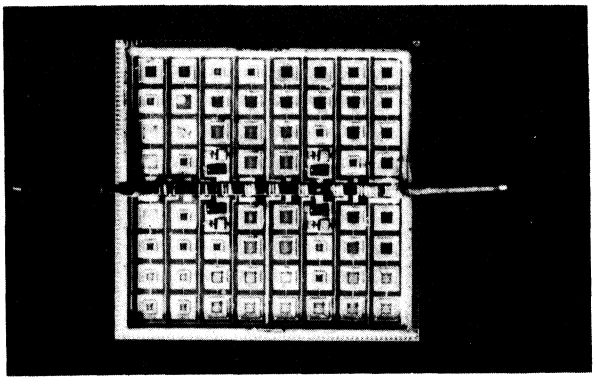

FIGURE 7 Chip-on-tape high density packaging (logic package for a large computer).

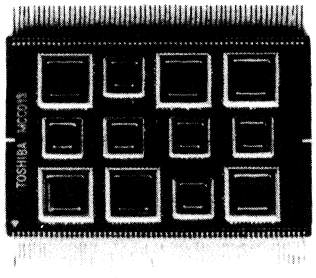

FIGURE 8 Chip carrier high density packaging (12 bit microcomputer unit).

The chip carrier (CC) has less that half of the chip and wire (C & W) packaging density. The chip carrier cost is greater than the chip and wire cost. The difference is caused by the packaging around the chip carrier. The ability to pretest a chip is the only merit

TABLE V
Comparison between high density packaging technologies

	Chip and wire	Chip carrier	Chip on tape
Packaging density (DIP-on-PCB = 1)	6 ~ 12	Δ 3 ~ 4	5 ~ 10
Chip availability	Wide	Wide	Δ Limited
Pretest	Δ Impossible	Possible	Possible
Packaging cost per chip	Low	Δ High	Δ High
Productivity	○	○	○

Δ, Demerit; double mark, higher grade.

superior to the C & W. Therefore, CCs are suitable for applications where highly sophisticated chips like CPUs are used and pretesting of chips prior to assembling is inevitable, even at the cost of packaging density.

Though the chip on tape (TAB) is considered to be the ideal form as it has merits of both high density comparable to C & W and pretestability as CC, for the present, the availability of TAB chips on the market is extremely limited. In order to fabricate TABs in-house, a vast investment sum is necessary in facilities for wafer bumping and inner-lead bonding. The TAB process, inherently, does not pay in small volume and wide variety of chips, which are likely to be characteristic of the hybrid packages.

Consequently, the chip and wire will be able to be dominant as the lowest cost, highest density packaging technology in the high density packaging field until the chip on tape will become available as widely as bare chips in the market place. However, it should be emphasized that the assembly process automation and the minimization of test/rework labour are keys to successful chip and wire multi-chip packages. The chip carrier will be viable in the application where pretesting of chips is inevitable, or in the military field.

CONCLUSIONS

1) A low cost, large scale, high density multi-chip package, including 76 IC chips (5,700 gates) on a 2 in × 3 in chip, was realized using the chip-and-wire technology. Keys to successful chip-and-wire multi-chip packages on production basis are:

Soft/hardware technology to minimize the test/rework labour

Thorough reduction in assembling labour by automation/mechanization

Material cost reduction by reducing the use of gold (ceramic multilayer substrate uses less gold than its thick film counter part)

Rework/repairability (solder seal is advantageous)

Reliable seal (hermetic seal is the best)

2) The cost goal 'comparable to DIP on PCB' has not been reached, but the goal is close at hand (25% higher). Measures taken in order to reach the goal will include a review of the seal method as well as the mechanization of the seal process.

However, estimating the entire cost at the system level, including the material saving and the improved reliability/maintainability, the multi-chip package will have surpassed the DIP on PCB even in cost.

3) The authors assess the chip-and-wire in comparison with other high density packaging technologies as follows:

The chip-and-wire makes it possible to realize lowest cost, highest density multi-chip package on a production basis, excepting highly sophisticated devices which inevitably require pretest prior to assembling.

The chip carrier is effective in applications where pretesting of devices is inevitable, even at the cost of packaging density, and in the military field.

Though the chip on tape is considered to be the ideal form, as it has merits of both high density comparable to the chip-and-wire and pretestable as the chip carrier, it will not be dominant in the hybrid field until the chip on tape become available as widely as bare chips in the market.

REFERENCE

1. Packaging technology responds to the demand for higher densities, Jerry Lyman, *Electronics*, p. 119 (Sept. 28, 1978).