COMBINATION OF THICK-FILM DIELECTRIC/THIN FILM CONDUCTOR FOR FINE PATTERN FORMATION OF MULTI-LAYER SUBSTRATE

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Presented in this paper is a realization of Multi-Layer Substrate with $30\ \mu\text{m}$ signal pattern width and $100\ \mu\text{m}$ square via holes on a $100\ \text{mm}$ square ceramic substrate. To obtain this fine signal pattern width, a thin film technique, "GSP" process, has been applied on a thick film dielectric layer. For the $100\ \mu\text{m}$ square via holes through the thick film dielectric, a new thick film technique, "DD" process, has been developed utilizing a photolithographic technique. This paper describes the processes and the results obtained by the method.

1. INTRODUCTION

Large-scale Multi-Chip Packaging Technology is vital for logic modules for high speed large computers. To realize higher system performance based on high speed semiconductor LSI chips, reduction in propagation delay time between chips should be carefully designed on a multi-layer ceramic substrate interconnection with high impedance and low resistance. For these requirements, high density and fine pattern are necessary on signal lines of ceramic substrates. The printing process is generally used for pattern formation of thick-film multi-layer substrate. It is, however, difficult to get a pattern width less than $100\ \mu\text{m}$ or via holes less than $200\ \mu\text{m}$ square. The thin film process has an advantage of fine pattern generation. On the other hand, the thick film process has an advantage that it is easy to make multi-layer structures. To obtain a finer multi-layer substrate, combination of some features from these process, a thin film for signal and a thick film for dielectric layer has been developed using a photolithographic techniques.

2. PROCESS AND MATERIALS DESCRIPTION

The method, which is used for $30\ \mu\text{m}$ signal pattern width is the thin film technique and is called "GSP" (Gold Selective Plating) process. The substrate is

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sputtered with base metals, laminated with a thin layer of an organic photo-sensitive film, and then exposed to UV light through a photo-mask. After the substrate is developed, it is gold plated selectively on $30\ \mu\text{m}$ patterns, and then photo-resist is removed and excessive base metals is etched off the substrate surface. The method, used for $100\ \mu\text{m}$ square via holes through the thick film dielectric is essentially a photolithographic process and is called "DD" (Direct Development) process. The substrate is covered with a thick film of dielectric paste on the entire surface by using a screen printing technique. After this thick film of dielectric paste is dried, the substrate is laminated with a thin layer of an organic photo-sensitive film, and then exposed to UV light through a photo-mask. The film is exposed and developed selectively for the via holes and an organic developer etches off the materials

FIGURE 1 Sectional view of multi-layer substrate.

FIGURE 2 Gold selective plating process for signal pattern.

all the way to the dried dielectric film, creating the desired via holes. Next, a thick film conductor paste is squeegeed into the via holes, dried and then fired. The sectional view of a realized mutli-layer substrate is shown in Figure 1. The process sequence is shown in Figure 2 and Figure 3. Photos 1-5 show examples of this process.

FIGURE 3 Direct development process for dielectric layer.

PHOTO 1 1st conductor layer.

PHOTO 2 30 μm signal lines and 100 μm square via holes.

PHOTO 5 Chip pad, ground and power layer (3rd layer). (100 μm $\times$ 100 μm substrate.)

PHOTO 3 2nd conductor layer (30 μm wide signal patterns and power distribution lines).

PHOTO 4 1st and 2nd signal lines (30 μm wide signal patterns).

2.1 GSP Process

2.1.1 Substrate The substrate used in this process is a square piece of 97% Alumina ceramics of 100 mm square, 2 mm thickness with 0.4–1.2 μm CLA (Center Line Average) surface smoothness and 50 $\mu\text{m}/100$ mm camber. The substrate is ultrasonic cleaned in a Tetrachloroethylene solvent, fired at 900°C, and then cleaned with oxygen gas in a plasma reactor.

2.1.2 Sputter titanium and palladium A double metallic layer is sputtered over the entire substrate for a base metal for the gold plating. The first metal layer is titanium and its thickness is about 1000 Å as the adhering layer. The second layer is palladium and is about 1000 Å in thickness prior to the gold plating to provide a high conductivity layer for the subsequent plating operations. These layers are sputtered onto the substrate surface continuously without interruption.

2.1.3 Laminating A Riston dry film, 15 μm thickness is used for this application as a photoresist. A hot roll laminator is applied for laminating of the dry film. Immediately prior to laminating, a substrate is heated to 120°C to obtain good adhesion of the dry film to the substrate.

2.1.4 Exposure Exposure of the dry film laminated substrate is done using a mask aligner with a 1000 W Hg lamp of 360 nm region UV radiation. On the average the substrate is exposed for 2 seconds at a power density of 4 mW/cm² using a positive photo-mask for 30 μm width signal patterns. After the exposure, the substrate is left alone for 15 minutes at a room temperature for a complete photopolymerization of the dry film.

2.1.5 Development Development of the exposed substrate is done using a centrifugal type spray developer designed inhouse. The MYLAR protective covering is removed from the surface of dry film immediately prior to the development. 1-1-1 trichloroethylene is used for the development solvent.

2.1.6 Gold selective plating Following a development of the dry film, the substrate is ready for selective gold plating. Prior to the plating, substrate is cleaned with oxygen gas in a plasma reactor to completely remove organic contaminations from the developed conductor patterns. It is not necessary to pretreat the substrate for other metal finishing operations prior to the gold plating, because the base metal is sputtered with palladium, and the storage time is short. The plating is performed in the SEL-REX NEWTRONEX-210, neutral and noncyanide bath, at a current density of 0.6 A/dm². The power source used is constant current DC. Gold reached a thickness of 10 μ m in about 20 minutes of plating.

2.1.7 Removing photoresist The plated substrate is dipped into a methylene chloride solvent for 5 minutes, and the dry film photoresist is removed mechanically by fine brushes.

2.1.8 Etching base metals The base metal which is sputtered palladium and titanium over the entire substrate is chemically etched leaving the gold plated patterns untouched. The etchant for palladium is a mixture solvent of hydrochloric acid and ferric chloride, and the one for titanium is a mixture solvent of hydrofluoric acid and nitric acid.

2.2 DD Process

2.2.1 Printing and drying A thick film dielectric paste, DuPont-9805, is used for this process. The paste is printed over the entire substrate using screen printer with a 325-mesh stainless steel screen. The printed substrate is left alone for 15 minutes at a room temperature for levelling of mesh mark, and then dried at 120°C for 15 minutes.

2.2.2 Laminating A Riston dry film is used in the same way as is previously described for the GSP process.

2.2.3 Exposure An exposure of the laminated substrate is done using the mask aligner for the via hole patterns. An average exposure time is 10 seconds at a power density of 4 mW/cm² through a positive photomask.

2.2.4 Development and etching The method used is the same as the one which was previously described for the conductor pattern development of the GSP process. The developing of Riston dry film for the via hole patterns is done by spraying an organic solvent, 1-1-1 trichloroethylene, and then this solvent continuously etches the material all the way to the dried dielectric thick film creating the via holes.

2.2.5 Squeegeeing DuPont-9791 gold thick film paste is squeegeed into the via holes which are using the double wet pass cycle of a screen printer without any screen but with a neoprene-made right angle squeegee.

2.2.6 Firing A firing furnace is used for this process. The firing conditions used are 10 minutes of peak temperature of 900°C and total of one hour profile based on paste manufacturer's recommendations. This process burns off the Riston dry film, and also fires the conductor paste which fills the via holes and the dielectric paste.

3. RESULTS

3.1 Electrical Resistance of the Signal Lines

On the average resistance per unit length of the signal line with 32 μ m pattern width and 10.5 μ m pattern thickness was 0.87 ohm/cm.

3.2 Line Capacitance of Signal Pattern to the Ground and the Power Layer

The average line capacitance per unit length of signal pattern with 60 μ m thickness for 1st and 2nd dielectric layers respectively is 1.5 PF/cm.

3.3 Reliability of the Via Contacts

An evaluation of reliability of the via contact was performed by using a particularly designed test pattern which has series connected 11,000 via contacts between the 1st signal layer and the 2nd signal layer.

3.3.1 Heat cycle test The test samples were processed in heat cycle up to ten times through a firing furnace at ten minutes 900°C of peak temperature for the total of one hour profile. The sample did not show any failures in their electrical connections. The increase in electrical resistance of the via contacts between the heat cycle tests was 3% at most and this increase occurred once after the first heat cycle.

3.3.2 High temperature and high humidity storage test The test samples were stored under high

temperature (150°C), high humidity (80% R.H.) environment with 10 mA constant DC current applied to the test circuits. After 1 150 hours elapsed, the electrical resistance of the via contact increased by 6% on the average over the initial value. After a lapse of 2 038 hours the electrical resistance of the via contacts increased by 6.3% over the initial value, but the test samples did not show any failures in their electrical connections.

4. CONCLUSIONS

The process for a fine pattern formation we developed can achieve the following results and characteristics.

1) To obtain a large size and higher integrated multi-layer substrate which has 30 μm width signal lines with 127 μm pitch and 100 μm square via holes, a feasible combination of DD process for a thick film dielectric and the GSP process for a thin film conductor is achieved.

2) Electrical resistance per unit length of the signal line which has 30 μm width and 10 μm thickness is 0.87 ohm/cm.

3) Electrical capacitance per unit length of the signal line to the ground and power layer is 1.5 PF/cm with 60 μm thickness for the 1st and the 2nd dielectric layers respectively.

4) The reliability of the via contacts is fair.

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