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IMPROVEMENTS IN MULTILAYER CERAMIC CAPACITORS†

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The increased use of Multilayer Ceramic Capacitors in both chip and encapsulated formats is mainly due to their excellence at decoupling Integrated Circuit Random Access Memories.

As a result of this excellent performance, large volumes of this type of capacitor are currently used and indications are that further increases in volume will continue over the next decade. There is therefore a market requirement for continued improvements in performance, reliability and cost.

There have been major processing changes for cost reduction reasons, which have resulted in new dielectric systems, changes in electrode types and greatly reduced dielectric thicknesses.

Studies of the failure mechanisms in these capacitors have been made, and this paper outlines the effect of process and materials on the reliability of these capacitors.

In addition, critical process stages are highlighted and control levels indicated. Some new work on testing techniques and its relevance to delaminations is also reported.

1. INTRODUCTION

The current world market for Dynamic Random Access Memories (DRAMS) is of the order of 500.10^6 per year. This figure is estimated to increase to 2000.10^6 by 1986. A distinctive feature of this component is both the high speed of gate switching, 50-150 nano seconds and the resulting high speed current peaks (150mA), (see Fig. 1). DRAMS are generally used in quantities and are arranged in arrays on printed circuit boards. These fast current peaks will result in acute regulation and interference effects on the power supply rails, and it is very necessary to supply adequate decoupling. In addition, for proper operation of each memory, instantaneous power must be made available to it on demand. The most usual method of achieving both the decoupling and this reservoir need is by the use of capacitors within the memory board arrays, (see Fig. 2). In this figure, a 0.1 μF capacitor is shared between two DRAMS on the V_{DD} line and one capacitor between four DRAMS on the V_{BB} line. This arrangement is typical of that adopted for professional designs for 4K and 16K DRAM devices. These devices have used two power rails typically V_{DD} V_{BB}. The new 64K DRAM needs only a single 5V supply. Information to date has projected that one 0.1μF capacitor per 64K DRAM will be needed. This semiconductor market growth will be repeated as a capacitor market growth as well. Because of this type of application, it suggests that capacitance values of around 0.1μF at 50V rating or lower will be most popular.

The multilayer Ceramic Capacitor has been found to be very suitable for this application, particularly due to the following factors:-

- small size
- $-55°C/+125°C$ operating
- available as Chip, DIL, Axial or Radial mounting
- excellent reliability

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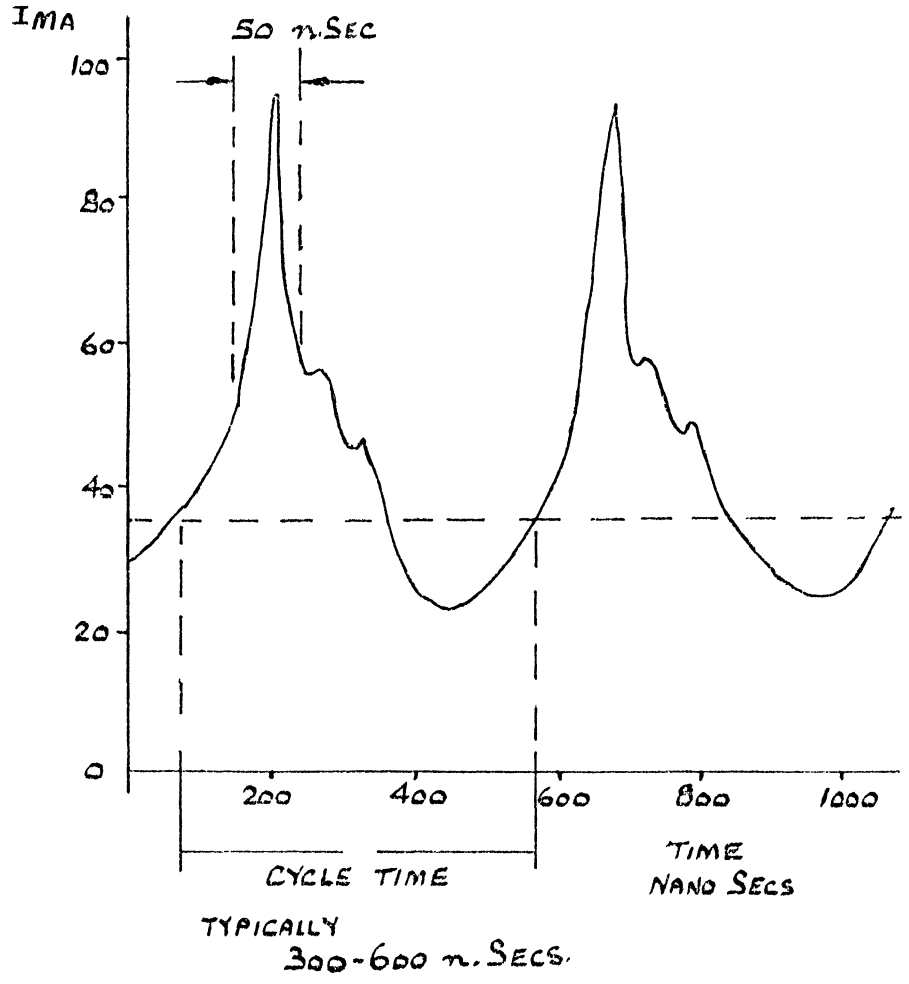

FIGURE 1 Current time graph 16K DRAM.

It has been the role of the Capacitor manufacturing industry over the last 10 years to make major improvements in cost, performance, and reliability. This has been achieved by major research efforts in materials and processes. This paper summarises some of the improvements and highlights the critical steps.

2. MANUFACTURING PROCESS

Fig. 3 outlines a typical manufacturing process for the manufacture of a Multilayer Ceramic Capacitor Chip. The items marked * are those that will dictate the performance level of the capacitor and are further described. All operations of course, must be carried out in accordance with standard operating procedures. For proper process control, it is essential that all steps are always repeated accurately and that an adequate monitoring system is used.

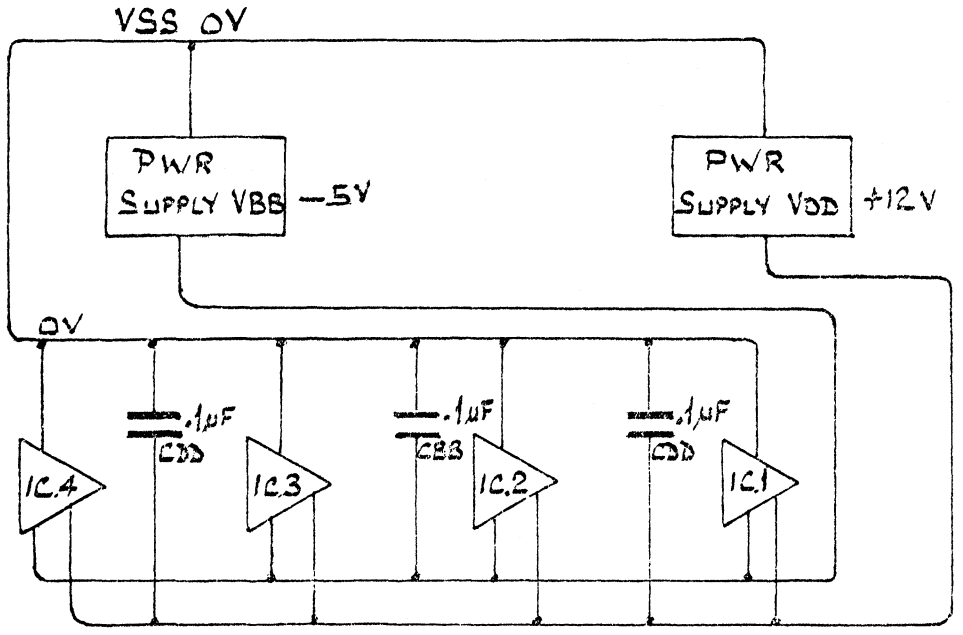

FIGURE 2 Memory board decoupling

i. *Milling*

In order that a uniform dielectric layer is produced, it is desirable that the dielectric powder is milled to produce as uniform a particle size as possible. This should be preferably less than 1μ with no large particle present.

ii. *Film Production*

The two most popular routes are:-

- doctor blade casting
- drawing or vertical casting

control and monitoring of these processes needs to concentrate on:-

- no pinholes
- uniform thickness
- uniform density

Fig. 3(b) shows the constructional details of the capacitors and some typical specimens are shown in Fig. 3(c).

iii. *Electrode Material Preparation*

The control of particle size of the metal alloy is as important as the dielectric powder.

iv. *Electrode Print*

This process is usually achieved by screen printing, and it is necessary that the print thickness is the minimum necessary for good electrical performance (ESR). Excessive print thickness is one cause of delamination.

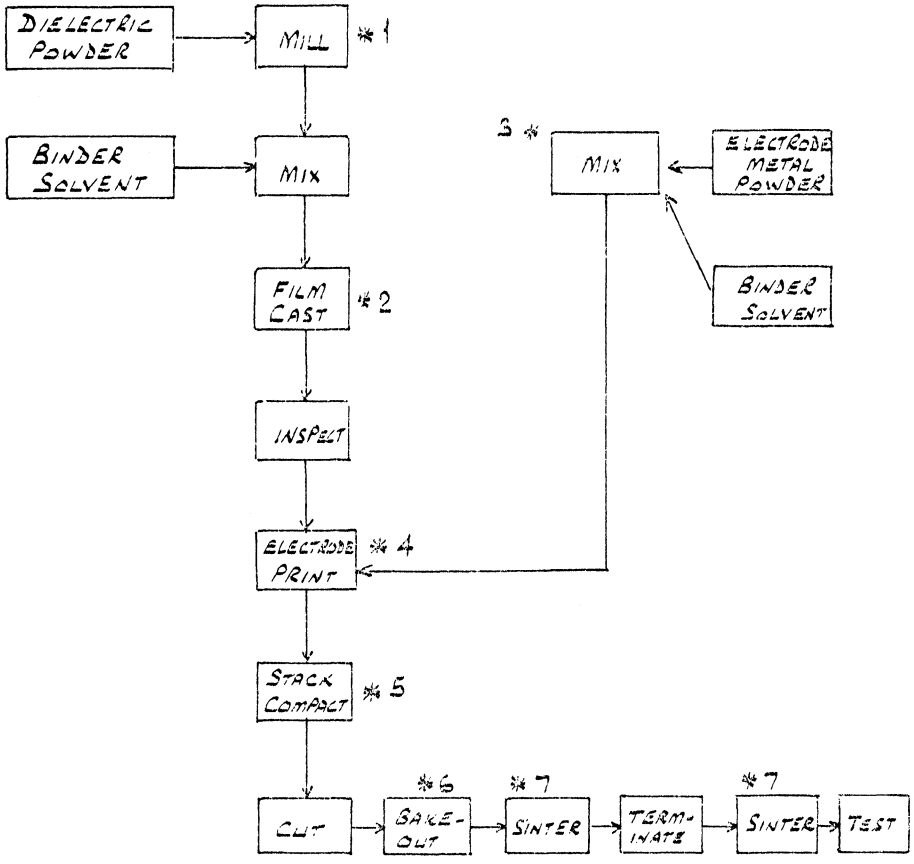

FIGURE 3 Manufacturing process, construction, and final product of multilayer ceramic capacitor chips. Fig. 3(a) Manufacturing process chart

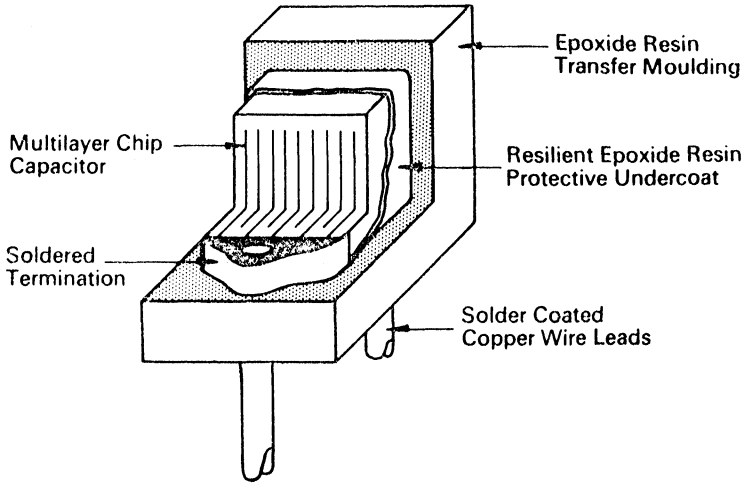

Fig. 3(b) Capacitor construction

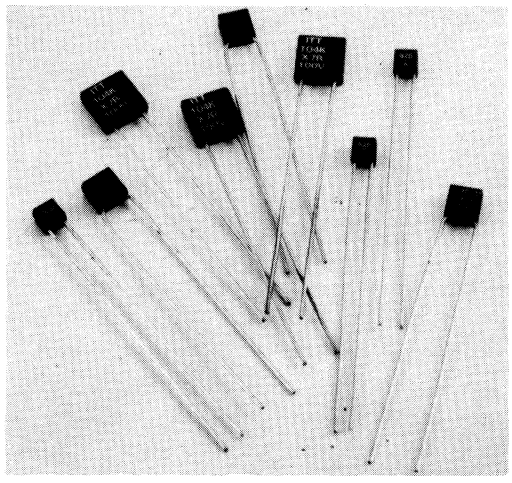

Fig. 3(c) Sample capacitors. (The largest specimens (0.104 F) are 10 mm × 10 mm × 4 mm.)

v. *Stack*

Layers of printed ceramic sheets are sequentially stacked (Fig. 4). The offset of each alternate plate is achieved in this process. Inaccurate stacking is the major cause of electrical breakdowns, in which electrode plates short circuit (see Fig. 5). In Fig. 5 proper design and manufacture allows equal insulation bands between the electrode end 'X' the chip edge and end termination, which of course is of the opposite polarity. Bad stacking

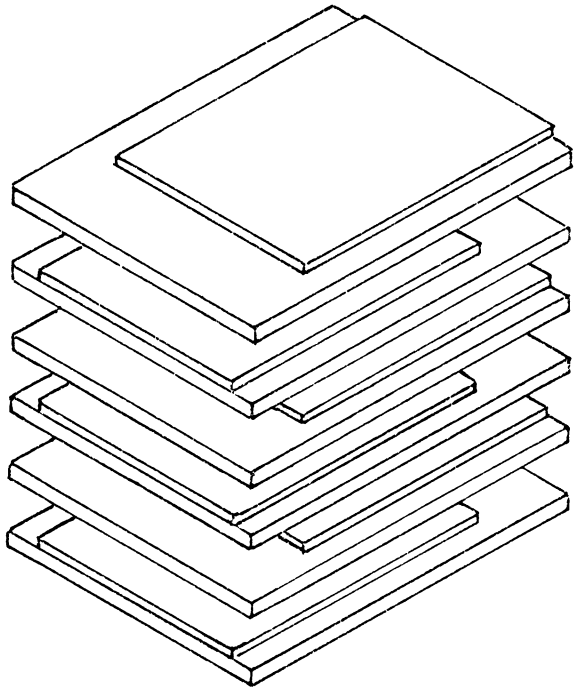

FIGURE 4 Multilayer offset plate stacking.

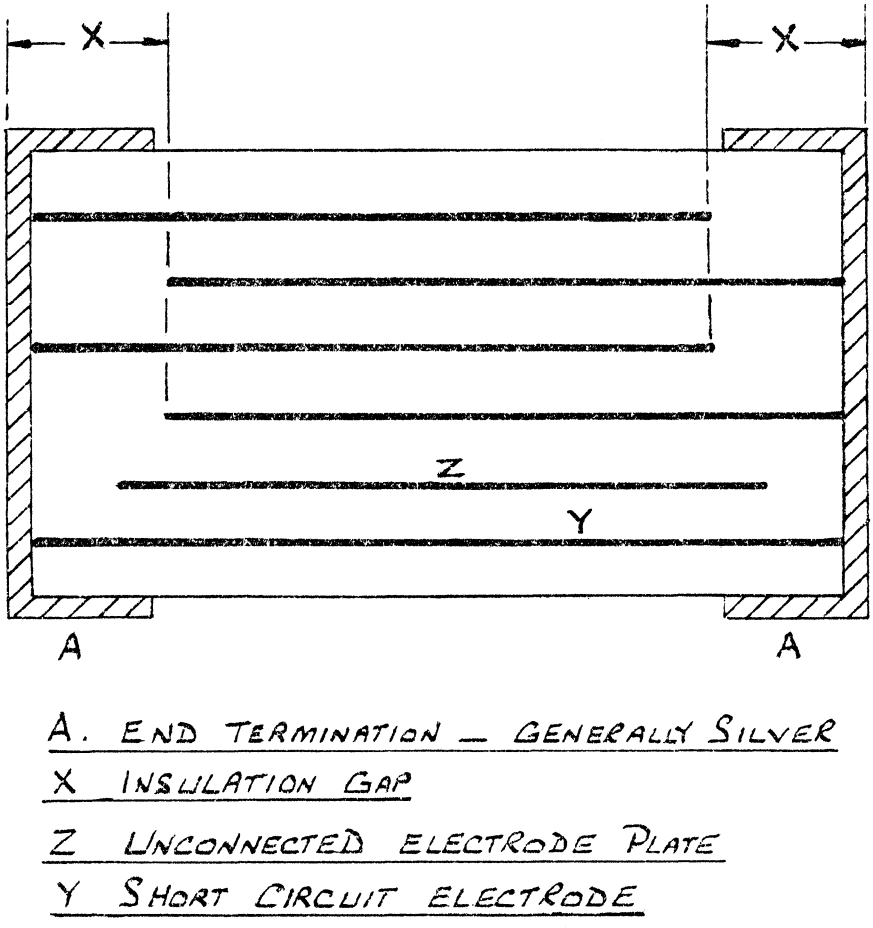

FIGURE 5 Electrode Registration.

or incorrect chip cutting leads to floating electrodes 'Z', or electrodes that short circuit end to end, 'Y'.

vi. *Bakeout*

The binder and solvent systems used are normally complex hydrocarbons. The bakeout process is designed to remove these materials before the ceramic sintering process takes place. If the bakeout process is too rapid at any point or the organic materials are allowed to exotherm, internal voids (delaminations) are produced. Fig. 6 contains diagrammatic views of delaminations. 'A' shows a gross fault encompassing more than one electrode layer. 'B' is a gross fault, between two electrode layers (of opposite polarity) and may also be described as a gross void, which whilst totally undesirable may perform satisfactorily. 'C' is a *minor* delamination and may also be layer parting which rarely causes any reliability problems. 'D' is another minor delamination, similar to 'C', but, as will be discussed later, is a potential hazard. 'E' is a void and normally of no consequence.

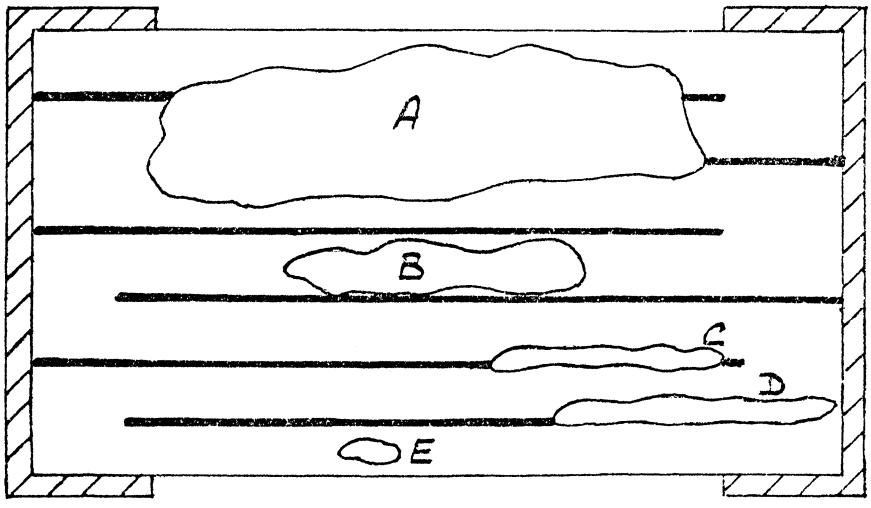

FIGURE 6 Delaminations – diagrammatic.

vii. *Sintering*

It is necessary in both the ceramic sintering and end termination sintering process that the temperature profiles used are chosen so that they do not stress the ceramic structure. Excess stress can cause internal micro-cracking.

The major process changes that have occurred in the last ten years may be summarised as follows:-

– simpler binder/solvent systems
– improved milling techniques
– improved particle analysis equipment
– substitution of electrode systems

The changes in the binder and solvent systems have been due to a need to reduce costs, or obsolescence of the original material. The significance lies in the amount of development necessary to introduce the replacement materials and the necessity to complete extensive analysis using Thermal Gravimetric Analysis (TGA), and Differential Thermal Analysis (DTA) to ensure that the bakeout cycle is correct (vi). The very fine metal particles particularly those of Platinum and Palladium have a tendency to be pyrophoric and when in the presence of a flammable organic solvent, exotherm can take place with the production of large quantities of gases. A correct bakeout cycle removes both solvent and binder without any mechanical effect on the multilayer stack.

The improvements in milling techniques are due to the availability of improved equipment and media. In a similar manner particle analysis equipment such as the Sedigraph, for determining the range of particle sizes is available now, and cheap S.E.M. for particle shape analysis is also a useful tool.

The most significant process change has been in the electrode composition and the resulting dielectric composition changes. In the early days of multilayer capacitors, conventional single layer (disc, tube) dielectrics were used with sintering temperature requirements in the range 1250°C-1400°C. Barium Titanate based dielectric materials upon which the majority of ceramic capacitors rely, needs a good oxidising atmosphere to

mature correctly. The oxygen bonding to the Titanium atom is relatively weak so that these materials will reduce easily. The electrode compositions must be capable of withstanding these temperatures and conditions without oxidising or melting. Melting will cause globules of metal to form which will give rise to discontinuous electrodes.

The original electrode compositions were generally mixtures of Platinum, Palladium and Gold, the so-called ternary systems. This combination of dielectric and electrodes, whilst adequate is of course expensive in material and sintering cost, and difficult to control. The need to reduce the cost of the electrode, for instance by changing to mixtures of Palladium with Silver additions and then Silver with Palladium additions means that dielectrics that sinter completely at lower temperatures (1180°C-1250°C) were required. These systems have been developed and are now current, and apart from the obvious cost advantages are easier to control in the process stages, this of itself leads to a more reproducible process and better reliability.

3. TESTING AND QUALITY EVALUATION

Structure

The first evaluation takes place immediately after the ceramic sintering process. A Destructive Physical Analysis is carried out on a representative sample from each batch by sectioning, to determine that the correct internal structure has been made. This analysis particularly concentrates on electrode registration, (Fig. 5), and delamination detection, (Fig. 6). Delamination is nearly always due to a reaction between the electrode material and the dielectric material. A multilayer structure produced with the omission of the electrode layers never contains delaminations.

To control this electrode/dielectric reaction, critical control is required as follows:-

– electrode powder – surface area and particle size

– electrode print thickness

– bakeout schedule

A typical Quality Control Procedure at DPA would incorporate the following delamination standard:-

– A major defect is:-

either (i) any delamination or void, greater than 1/3 of the electrode length which at any point, is wider than 1/2 of the dielectric thickness.

or (ii) any void which leaves adjacent electrodes opposed to each other.

After this stage a representative sample of capacitors will have end terminations applied and electrical measurements may be applied.

It should be noted that in production, a routine DPA is carried out after the end termination process, which itself can contain a sintering process of up to 900°C.

Electrical

Routine electrical inspection on the quality sample will include measurement of capacitance, power factor, voltage proof (or dielectric withstand voltage) and insulation resistance. These tests give, after analysis, useful indicators to the state of the process:-

Capacitance. The variation of the batch average capacitance value compared to design

normal, is an indication of any movement in dielectric constant or variation in firing temperature. In addition, the spread of capacitance values achieved is a direct indication of the adequacy of the production process.

Power factor. This may be related to electrode plate uniformity and dielectric sintering.

Voltage proof. May be directly related to dielectric porosity (including pinholes), uniform dielectric thickness.

Insulation resistance. Is directly related to the dielectric quality.

Failure Mechanisms

Ceramic capacitors both single and multilayer normally fail in the short circuit mode. Failures that occur and are detected in the production process and test, or early in life, are generally due to bad registration or cutting, (Fig. 5), gross delaminations, (Fig. 6A), or gross cracking, (Fig. 7). Gross cracking which can be caused by bad mechanical handling in process is more normally caused by thermal shock due to inadequate profiles at either:-

- dielectric sintering
- end termination sintering
- lead out soldering
- encapsulation curing

The majority of failures in life are again due to the same manufacturing faults which cause the short life problems.

STC Components – Capacitors, in conjunction with our Research Laboratories – Standard Telecommunications Laboratory, Harlow, and our Central Applications Laboratory, Harlow, and a joint investigation with British Telecom have carried out extensive work into the effect of delaminations on reliability and the so called Low Voltage Failure effect.

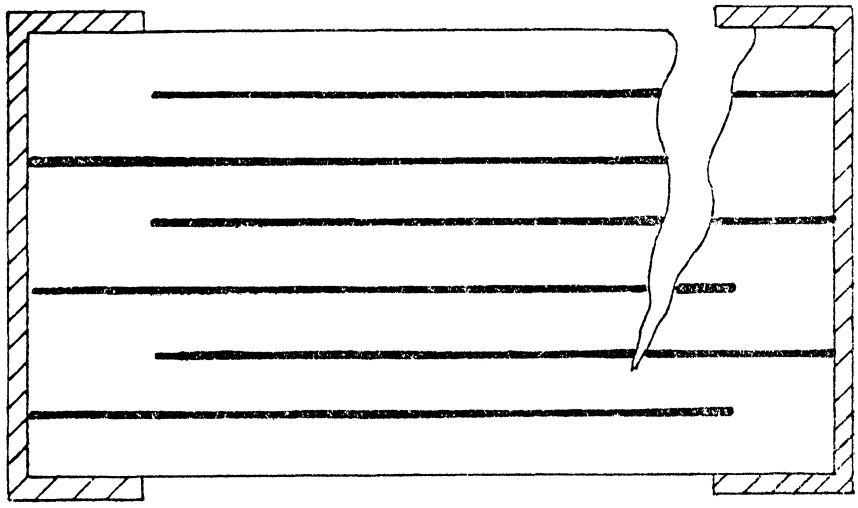

FIGURE 7 Failure mechanisms – gross cracking.

Delaminations

At the beginning of this study, the immediate concern was firstly to ensure the manufacturing process did not exhibit this fault, secondly to determine whether a non destructive test was available to ensure that no grossly delaminated product was shipped. It has been reported elsewhere on the use of X-Rays, neutron radiation, scanning laser acoustic microscopy, and harmonic detection for this purpose. Very satisfactory results have been achieved by STC with an electrical test we call the RAMP test. The equipment is shown in

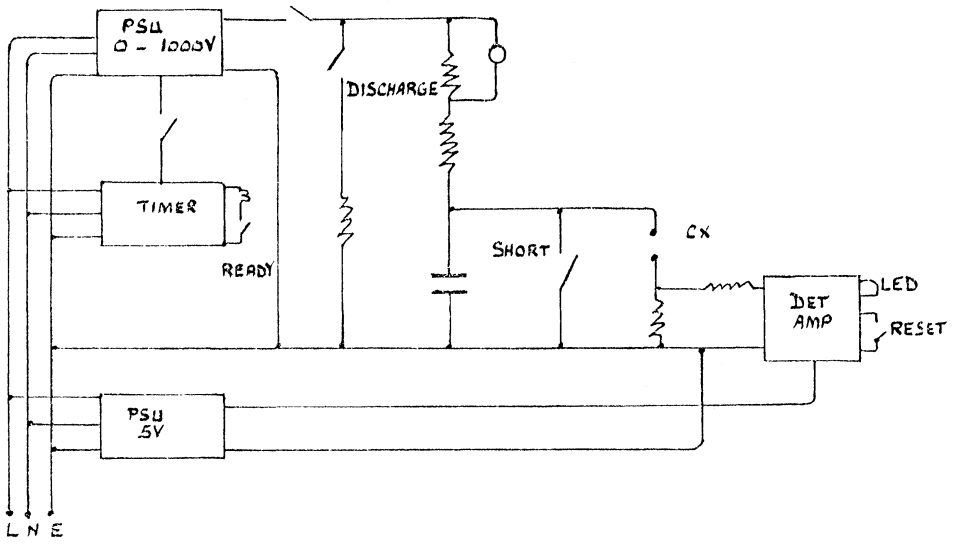

FIGURE 8 Ramp tester.

Quantity of chips Ramp tested	**56861 pieces**
Quantity passed Ramp test	32632 pieces –57%
Quantity failed Ramp test	24229 pieces –43%
DPA RESULTS	
Sample from Ramp pass	**1000 pieces**
Delamination free	799 pieces –79%
Minor delamination	207 pieces –21%
Major delamination	4 pieces –
Sample from Ramp fail	**1000 pieces**
Delamination free	381 pieces –38%
Minor delamination	180 pieces –18%
Major delamination	439 pieces –44%

FIGURE 9 Ramp test analysis.

block diagram form in Figure 8, and in principle the component under test is voltage ramped from 0VDC to 450VDC in 5 seconds and held at that voltage for 15 seconds. Any non linear charging current or pulse is detected by the circuit and a fault indicator given. The table shown in Figure 9 shows that 50,000 capacitors were tested and analysis of 1,000 good and 1,000 bad by DPA showed excellent correlation with the test results.

Low Voltage Failures.

A low voltage failure is generally interpreted as a capacitor exhibiting an IR of less than 100KΩ when operating with not more than 5V applied, with a series impedance of greater than 30KΩ. As part of this investigation programme, a tester was designed and built with the block diagram shown in Figure 10. This tester is known as the Matrix tester and is suitable for detecting this type of failure.

It should be pointed out that the number of failures due to this cause is low enough to be impossible to measure statistically, and we would suggest that it may be of the order of 1 part in 10^7 *components* (not component hours).

The investigations into this failure mode suggest that the following conditions are necessary for low voltage, or more correctly low power failures to occur in multilayer capacitors:-

– micro cracking so that a path exists from electrodes of opposite polarity, (Fig. 11A) or from one electrode to a termination having the opposite polarity, (Fig. 11B).

– silver, or palladium, or alloys of both in electrode and/or terminations.

– water

unless all three are present, low voltage failures do not occur.

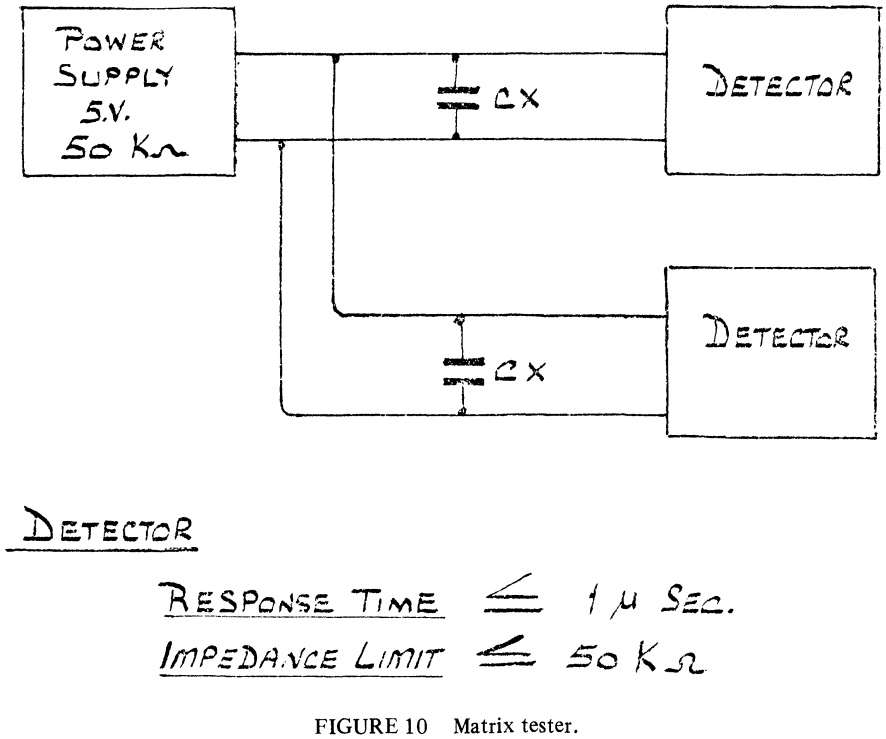

FIGURE 10 Matrix tester.

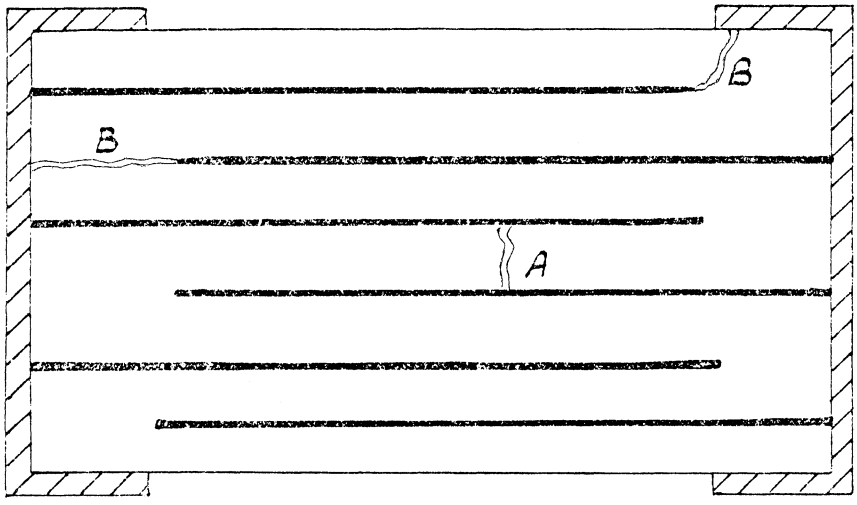

FIGURE 11 Low voltage failure – sites.

4. CONCLUSIONS

The control of the manufacturing process for the Ceramic Multilayer is the key to the reliability of the product in service. The monitoring of routine processes should automatically occur, but in addition the accurate determination of these processes and their limits is a key engineering development task.