

# VERSATILE PACKAGING CONCEPT USING THICK FILM HYBRIDS FOR ANALOG AND DIGITAL CIRCUITS

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The design parameters of a packaging concept are described, which allows the realization of a complex electronic module in a closed casing using commercially available components. These are soldered to multilayer thick-film circuits, mounted on metallic heat sinks. The multi-layer structure contains silver bearing conductors and supports trimmable resistors. The information presented concerns mainly the fabrication of the thick-film circuits and the thermal design.

## 1. INTRODUCTION

The realization of a complex local communication network with loop structure (SILK<sup>R</sup>) necessitated the development of a flexible, compact hardware packaging concept for the access ports. Many different solutions are known from the literature, e.g.<sup>2,4,5,6,12,16</sup>. For this application, several conditions had to be satisfied, namely:

- 1) Forced cooling is not allowed. Breakdown of such a cooling system could adversely affect the electronic parts. The reliability of these systems is not sufficient.
- 2) The electronic system must be able to work in an uncontrolled environment.
- 3) A wide range of components in different packages has to be connected. The reasons for this condition are, e.g., source independence; possibility for quick design changes; low numbers of each component type used; testability; analog digital circuits mixed.
- 4) The packaging has to support digital (up to 35 MHz) and analog circuits, e.g. clock extraction from the line signals.

The design chosen fulfils these conditions. A closed casing with a special cooling profile on the surface contains the electronic module and the power supply (figures 1, 2).

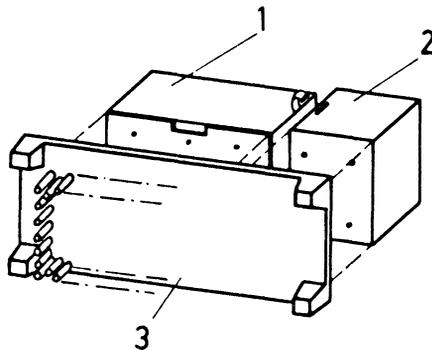


FIGURE 1 Electronics Module (1) and power supply (2) mounted to the radiator (3).

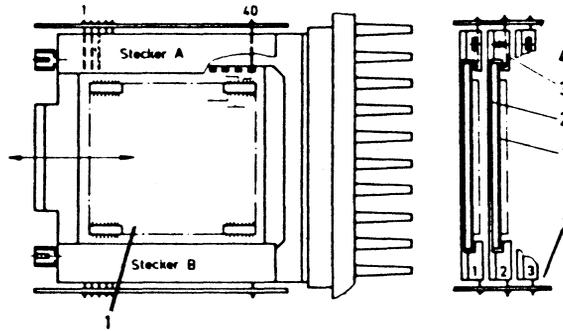


FIGURE 2 Thick-film Circuit (1) mounted on metallic heat conductor (2) and connected by two ZIF-connectors (3) to the motherboards (4).

The electronic module consists of two motherboards and a thermally highly conductive construction on which 18 Circuit-Modules are mounted. The modules are connected at two ends to the motherboards by special single-sided zero-insertion-force (ZIF) connectors with 40 pins (figure 3). The contact springs and additional hold-down springs keep the multilayer circuit in intimate contact with a thermally highly conductive metal plate, connected and screwed directly to the massive casing of the complete block (figure 6). The multilayer boards are manufactured using thick-film technique on  $4 \times 4$  inch alumina with Ag-containing conductors and thick-film resistors. In the following the emphasis is laid on those details of the packaging concept and thick-film-concept which are not already described in detail in the literature for similar solutions.

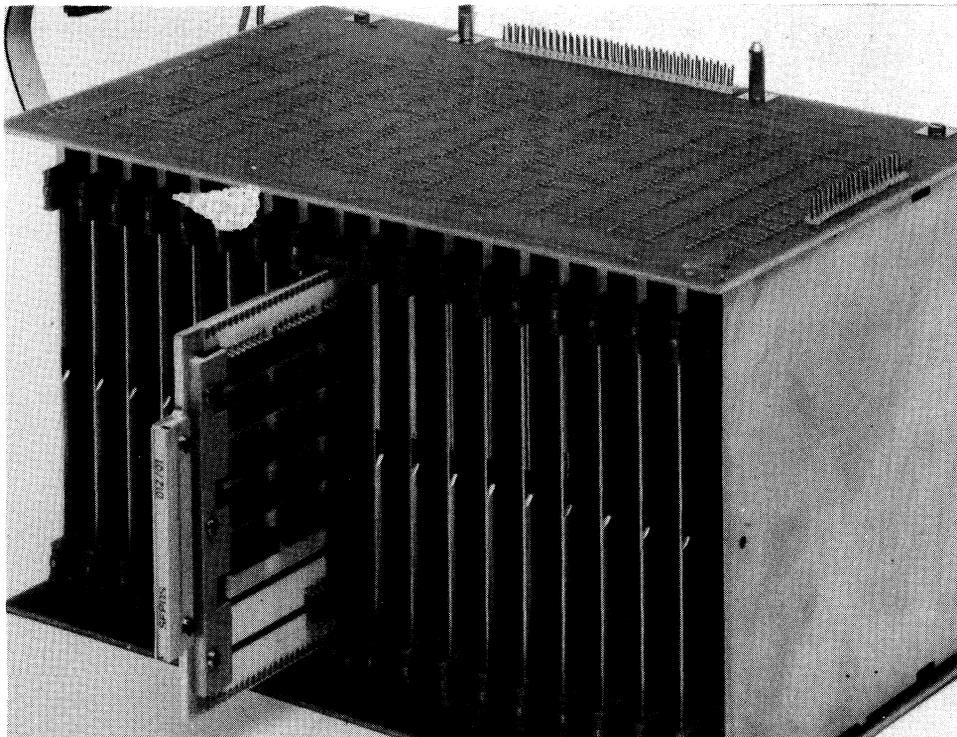


FIGURE 3 Electronics Module.

## 2. THERMAL DESIGN

The aim of a conservative design, imposed by the above-mentioned conditions, excluded highly sophisticated solutions described in the literature. The standard DIL plastic or ceramic-package may be used, if the temperature of the surface and the leads is held down.<sup>12,17</sup> Calculation and measurement showed that the combination of cooling by heat flow through the leads to the cooling metal plate and convection and radiation from the body to the neighbouring plate is sufficient for the power handling and environmental conditions in this case. Measurements were made with the CA 3046 for the junction temperature and with a thermocouple on the substrate. The electronic circuits produce 35 W and the specified environmental temperature is 45°C.

## 3. ELECTRICAL DESIGN

The speed of the electronic circuits to be connected by the packaging system imposes short signal paths and a sound grounding concept. The line interfaces are mounted on a separate connection board on top of the electronic module. The signals fed into the circuits which extract clock and data are situated at one end of the electronic module. The thermal conduction plates between multilayer circuits act as insulated ground planes. Ground is fed onto the multilayer board on four corners and distributed in a lattice over the surface, buffered by chip capacitors connected to  $V_{CC}$ . Even higher capacitance and lower inductance between ground and  $V_{CC}$  may be realized by putting these conductors one on top of the other. The distributed capacitance attained is 3.5 nF, at a resistance from edge to edge of 250 mΩ. This grounding scheme proved to be sufficient. A current step from zero to full load at one corner produced a short duration voltage drop of less than 150 mV at the opposite corner. CMOS circuits are sensitive to capacitive load. This must be taken into account for during layout. ECL circuits are sensitive to impedance changes along the signal paths. By shortening the length and adjusting the parameters of the signal paths, reflections can be reduced to an insignificant level. Schottky circuits require short paths and low impedance, both requirements can be met (example in figure 7).

## 4. THICK FILM MULTILAYER CIRCUITS

### *Conditions for Design*

The multilayer circuits must fulfil a number of conditions:

- Connect densely packed logic circuits
- Allow for impedance design on signal paths
- Contribute to the thermal conduction
- Support complex analog circuits with trimmable components
- Support a wide variety of components
- Be accessible for testing and repair.

Thick film multilayer circuits on alumina substrates with soldered components fulfil all these conditions. Other concepts considered were PC boards with thermal conductors included and enamel steel substrates with low temperature thick film processes.

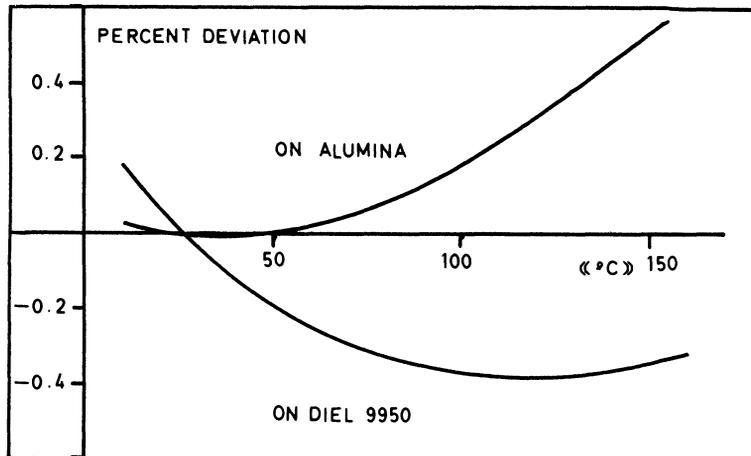


FIGURE 4 Temperature dependence of 1641-resistors (10 k/square).

### Thick Film Design

The first parameter fixed is the size. The realization of complex circuits on one board required a size of  $4 \times 4$  inch and 80 electrical connections. The limited number of connections sometimes imposed circuit adjustments, but did not put constraints on the designer. The second parameter fixed is the thick film conductor material. The soaring price of gold excluded this material for large circuits. Copper multilayer systems were at the time of conception not in the production stage and even today there are no high quality resistive systems. The price advantage compared to silver is reduced by process costs. The decision for a silver bearing system was made, being aware of the silver migration problem. To prevent silver migration,<sup>13,16</sup> every variable in the layout, process sequence, choice of material and soldering method was exploited:

The *first* step is to produce a well spaced layout. The layout is done with the program PPLS on a UNIVAC 1110 computer followed by manual adjustments on an interactive graphic terminal. The conductor distance chosen as input to the computer program, is so high, that approximately 90% of all connections are laid out automatically. The rest are introduced manually. A three layer system proved to be sufficient in most cases (figure 5) and a distance between conductors of 0.83 mm could often be attained with this system.

The *second* step against silver migration is careful process control during the manufacturing of the dielectric insulation layers (section 4.3).

The *third* step is the choice of a paste system which is in itself stabilized. The dielectric chosen is DuPont 9950, the lower conductors are DuPont 6120, the top conductor 4093. The paste systems are in constant development, as is the experience of a thick film manufacturer. EMCA-pastes and other systems are in the test stage as well. The dielectric 9950 supports the resistors for the 1600 DuPont series, or the 17-series. It is stable during multiple firings and usually shows good printing characteristics.

The *fourth* step is the sealing of the multilayer system. The connector pads are printed with a gold paste, the surface of the circuit is covered with a sealing glass and the soldering pads are covered by solder alloy.

The *fifth* step is the careful cleaning and handling of the finished circuits. Impurities increase silver migration by a considerable factor. Analog circuits often require high stability of resistors and precise trimming. Resistors may be realized as soldered chip

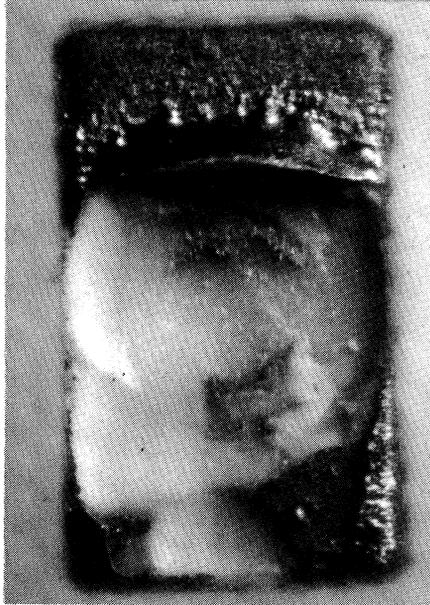


FIGURE 5 Cavity pulled out of the multilayer structure with a force of 23 N.

components, as soldered thick film subunits, as thick film resistors on top of the multilayer structure or in windows of the structure on the substrate surface. In this multilayer concept the choice is dependent on the number of resistors with similar values and on the absolute tolerance requirements. Trimming is achieved either by automatic laser trimming or in special cases with a manual sandblaster, mainly for high stability.

#### *Multilayer Production*

Commercially screen printers were adopted for precision multilayer printing. They are installed under vertical flow boxes, so that operators and visual inspections personnel work in a clean, low velocity air flow. Screen size is  $8 \times 10''$ . The substrates are automatically cleaned, transported into a hollow, positioned by pins with ball-bearings, printed on and transported to the dryer or the visual inspection stage. It was found necessary to automate the printer for clean and consistent results.

The best printing/firing sequence was found to be C1e D11e V1D12e V1C2e D21e V2D22e V3C3e, where C<sub>x</sub> = Conductors, D<sub>xy</sub> = Dielectrics, V<sub>x</sub> = Vias, e = firing. D<sub>x2</sub> is printed in transverse direction to D<sub>x1</sub> (see <sup>2</sup> for different sequences).

The sequence proved to print well and prevent conductor cracking.<sup>1,2</sup> The surface produced is flat even without dielectric thickness compensation. Resistor printing on top of the dielectric is a standard printing operation, but the variance of resistor values goes up if the underlying dielectric surface is not flat enough or if the firing is not done very carefully. The layout has to be corrected for the changed square resistance values of the pastes (figure 4 shows the influence of the dielectric).

Printing of resistors in windows of the multilayer structure on the surface of the substrate is much more difficult and requires special screens, due to the rim around the printing area. Even so, the standard 25 microns could not be attained. However, up to now, TCR and stability — especially under climatic test conditions — seem to be better than for resistors on top of the dielectric.

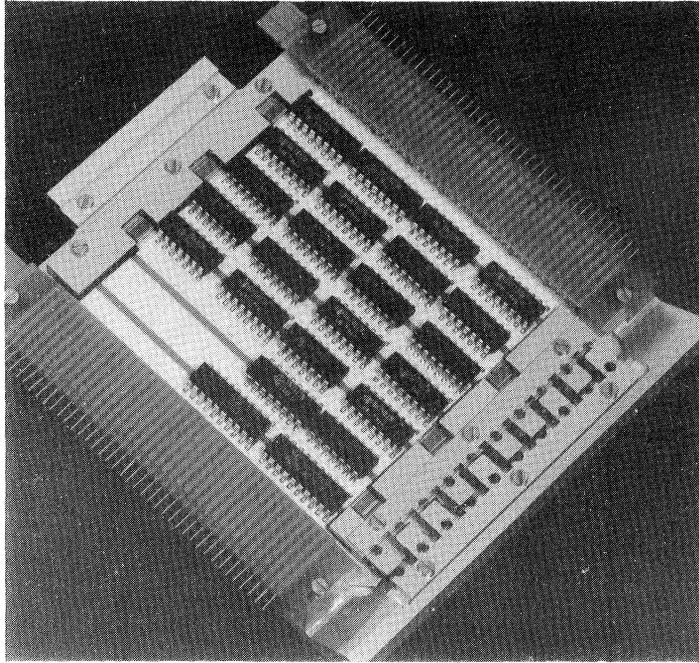


FIGURE 6 Multilayer circuit mounted on a heat sink. The single-sided ZIF-Connectors contribute to the force assuring intimate thermal contact.

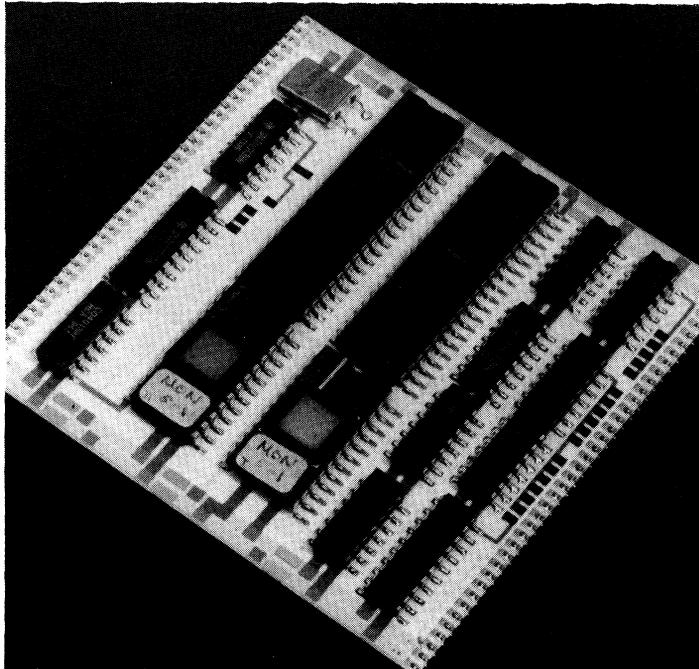


FIGURE 7 Example of a digital circuit.

The glass encapsulant is printed twice, but very thinly, to close holes and prevent cracking.

The finished circuit is automatically 100 percent tested on a GenRad 2245 with a special test adapter. Samples are tested separately for insulation resistance and for conductance of vias and conductor lines.

### *Soldering*

To assure good solder acceptance, a number of parameters have to be controlled, e.g. conductor thickness,<sup>2</sup> conductor firing, surface contamination and oxidation, solder composition and the soldering itself. Soldering has proven to be one of the most difficult aspects of the thick-film multilayer manufacture. Adhesion tests on standard IC-terminals, separated before or after soldering, proved to be the best test method for control of the parameters, these tests being used as production tests (figure 4). Reflow of solder paste, printed or applied by dispenser, was done with hot gas, hot plate, Browne-belt, infrared, resistance heating, solder-wave and solder source. The best method was a combination of gas and infrared, where the thermal masses and conductances can be accounted for. During development stage, soldering was monitored by measuring the chip temperature with CA 3046, measuring the temperature of the IC package with a loss mass thermocouple and the temperature of the solder paste on a terminal pad. Using this method, the preheat-equilibrium and the reflowpeak could be optimized for minimal thermal load of the thick film and the integrated circuits.

### *Testing*

Some inspection and testing methods during manufacturing have already been described. Tests of the thick film design described included vibration and mechanical shock, 3000 hours at 125°C, 1000 hours at 40°C/96% r.h. under 50 V load, and temperature cycling. Electrical continuity, insulation resistance and mechanical adhesion of the components were measured. Silver migration could be observed in these early designs, where silver bearing conductors were unprotected with a distance of less than 0.5 mm from one another. The protection by the sealing glass proved to be efficient. The tests are being continued to combine mechanical and thermal stress on a higher level. The tests carried out have proven to be sufficient with respect to the applications of the manufactured circuits.

## 5. CONCLUSION

The packaging concept described is actually used in a communication system. It has proven to be very effective when used for the realization of complex mixed analog/digital circuits consisting of very different types of components. The multilayer circuits in thick-film technology with silver-bearing conductors are a cost-effective connection means with good thermal characteristics. Future developments will encourage a wider application of chip carriers for active elements and develop the multilayer manufacturing process for higher packing density under retention of the achieved reliability, the moderate cost and the versatility.

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