

# MOUNTING OF MICROPACKAGES IN VAPOUR PHASE SOLDERING AND STUDY OF AGEING MECHANISM

CHRISTIAN M. VAL

*Thomson-CSF. CIMS A, 10-12 av. de l' Europe, 78140 Velizy, France*

and

JACQUES D. AGNIEL

*EFCIS, av. de l' Europe, 78140 Velizy, France*

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In this paper, the metallurgical aspect of conductor/solder/metallisation are analysed after cycling and ageing and the mechanism of degradation of the micro-solder is considered. As a consequence a new solder process of reflow is analysed (vapor phase reflow).

## 1. INTRODUCTION

The development of the LSI devices leads to the rise of micropackages allowing the test of the chip after wire bonding. The yield obtained with these plastic or ceramic packages is much higher than the one obtained from direct bonding on the substrate. Consequently, many components can be mounted on the same substrate. The emergence of a copper multilayer technique provides for economical consideration of large substrates (more than  $4'' \times 4''$ ).<sup>1,2,3</sup> In another way a new technique of soldering, vapor reflow soldering, allows the soldering of several thousands of joints with a very high yield. But it is to clear from the previous studies in our Company<sup>4</sup> that some mechanical problems intervene between components and substrates after thermal cycling and ageing. We have found three different available materials for substrates:

- Special PCB (MICPAC from SOCAPEX)<sup>†</sup>
- Enamelled steel (PES from LCC)<sup>‡</sup>
- Alumina substrate.

The results are shown on figure 1; where it can be seen that:

- 95% failure rate below 300 cycles (from  $-50^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ) for ceramic chip-carrier soldered on enamelled steel and PCB substrates. A shear failure in the solder joint was observed.

- 0% failure rate of those soldered on 96% alumina substrate below 500 cycles; but above 500 cycles it can be seen that an important degradation appeared in the solder joint.

The structural and analytical evolution have been made on solder joints between ceramic chip-carrier and alumina substrate. In the first part of the paper microanalysis on metallographic sections after ageing, cycling and for different vapor phase reflow cycle are discussed. In the second part, the vapor phase reflow soldering process is examined with large substrates.

Consequently, a new method to obtain a good yield in manufacturing was established:

- chip-carrier without gold  $\rightarrow$  Ni, Ag, . . .
- substrate without gold metallisation  $\rightarrow$  Cu
- reflow process at low temperature  $\rightarrow$  vapor phase soldering.

<sup>†</sup>SOCAPEX is a subsidiary of THOMSON-CSF.

<sup>‡</sup>LCC is a subsidiary of THOMSON-CSF.

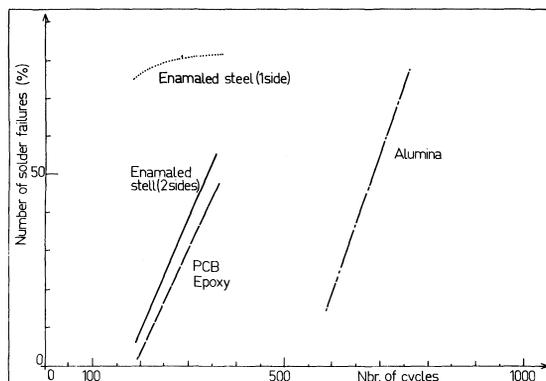


FIGURE 1 Number of solder failures versus thermal cycle [from  $-50^{\circ}\text{C}$  (30mn) to  $+125^{\circ}\text{C}$  (30mn)].

## 2. SOLDER JOINTS ANALYSIS

It has been determined that during the soldering cycle, the Sn-Pb alloy cannot reach the thermodynamical equilibrium conditions.<sup>5,6</sup> We are in the face of an evolutive system; the properties continue to change with time. The mechanical properties of the joints will undergo certain modifications during the ageing of the equipment. Furthermore, the presence of elements which constitute the metallisations of the substrate (Au, Pt, Pd, Cu, . . .) and of the components (Au, Ni, Ag, Pd, . . .) lead to the formation of inter-metallic compounds.<sup>7,8</sup>

Table I lists all the alloys of Au-Pb and Au-Sn that are possible:

TABLE I  
Alloys of Au-Pb and Au-Sn

Intermetallic compounds	Temperature of formation ( $^{\circ}\text{C}$ )	Crystal morphology
Au Sn <sub>4</sub>	217	"Acciculaire" (white)
Au Sn	309	
Au Sn <sup>2</sup>	280	Dentritic (grey)
Au Pb <sub>2</sub>	215	
Au <sub>2</sub> Pb	254	

The studies of P.S. Kay<sup>7</sup> and G.Y. Ewel<sup>9</sup> showed that the presence of these compounds affected the physical properties of the Sn Pb alloys, brittleness, thermal and electrical conductivity, self-diffusion (Kirkendall effect).

In addition to the formation of these compounds, the composition of the solder is modified with the solubility of the metals which constitute the metallisation.

Collated in Table II are the dissolution speeds in Sn Pb of the metals commonly used at different temperatures of work.<sup>10</sup>

Notice that at  $230^{\circ}\text{C}$  the rate of dissolution of gold in Sn Pb is 25 times higher than the copper one; it can reach  $2,5 \mu\text{m}$  per second.

A portion of this paper explores the evolution of the composition and the behaviour of the solder joint. Rather than realising these tests on normalized samples, not representative of the real joints, the tests have been conducted on real microsolders.

TABLE II  
The dissolution speeds of metals in Sn-Pb

Metals	Dissolution-speed $\mu\text{ms}^{-1}$		
	Temperature ( $^{\circ}\text{C}$ )		
	200	215	230
Ni	$5,1 \cdot 10^{-4}$	$6,3 \cdot 10^{-4}$	$1,1 \cdot 10^{-3}$
Cu	$5,1 \cdot 10^{-2}$	$7,6 \cdot 10^{-2}$	0,11
Ag	0,56	0,76	1,14
Au	1,27	1,65	2,54

### 2.1 Methodology

Though the soldering norm specifies a temperature of  $230^{\circ}\text{C} \pm 5^{\circ}\text{C}$  during 5 seconds, we thought it would be of interest to vary considerably these conventions. The appearance of a new reflow technology at a lower temperature ( $< 215^{\circ}\text{C}$ ) allows the use of a larger reflow time, the formation of intermetallic compounds being thermodynamically impossible at this temperature.

Consequently, it becomes possible to intensify the dissolution of gold in the volume of the solder joint. If we cancel the gold gradient of concentration (Fick's law) we thought we could eliminate the degradation of the system induced by the diffusion mechanism. The formation of non-homogenous areas at the interfaces: substrate/solder, component/solder, became impossible. However, the compounds formed during tinning ( $230^{\circ}\text{C}$ , 5 s), if possible, will continue to be present.

To estimate the behaviour of these solders in the equipment during the temperature cycles and storage, X-ray mapping was used to follow the evolution of the main elements.

In Table III tabulate the material and preparation conditions and measured parameters.

TABLE III  
Materials and conditions of preparation

		Measured parameters
<ul style="list-style-type: none"> <li>- Time of vapor phase reflow (<math>215^{\circ}\text{C}</math>):               <ul style="list-style-type: none"> <li>- 19 s</li> <li>- 110 s</li> </ul> </li> <li>- Thermal cycles (<math>-55^{\circ}\text{C}</math>; <math>+125^{\circ}\text{C}</math>):               <ul style="list-style-type: none"> <li>- 0</li> <li>- 500</li> <li>- 1000</li> </ul> </li> <li>- Storage at <math>125^{\circ}\text{C}</math>:               <ul style="list-style-type: none"> <li>- 0 h</li> <li>- 500 h</li> <li>- 766 h</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>- Substrate 96% <math>\text{Al}_2\text{O}_3</math>.</li> <li>- Substrate metallisation Au Pt 9596 DN.</li> <li>- Gold metallisation of chip-carrier "3 M".</li> <li>- Solder composition:               <ul style="list-style-type: none"> <li>Sn 62% by weight</li> <li>Pb 36% by weight</li> <li>Ag 2% by weight.</li> </ul> </li> <li>- Flux: LONCO 7525 TA.</li> <li>- Pre-heating: <math>180^{\circ}\text{C}</math>.</li> <li>- Solder bath temperature: <math>230^{\circ}\text{C}</math>.</li> <li>- Dipping time: 5 s.</li> </ul>	<ul style="list-style-type: none"> <li>- Optical observation of the joints.</li> <li>- X-ray mapping on cross-section:               <ul style="list-style-type: none"> <li>- near the chip-carrier</li> <li>- near the substrate.</li> </ul> </li> <li>- X-ray profile on metallographic cross-section:               <ul style="list-style-type: none"> <li>- near the chip-carrier</li> <li>- near the substrate.</li> </ul> </li> </ul>

## 2.2 Analysis

**Preparation of the samples** The chip-carriers (40 leads) and the substrates have been tinned at 230°C for 5 seconds. Each element (chip-carrier and substrate) as well as the assembly, have been weighted before and after tinning. Thus we have estimated on one hand the weight of each microsolder and on the otherhand we have also estimated the uniformity of the tin process.

Table IV shows these results. It is noticeable that the quantity of solder in the assembly is relatively constant ( $\pm 13,5\%$ ); this fact permits us to ensure the reproducibility of the concentrations of the different elements (Au, Pt, Sn, Pb, Ag) of the samples.

TABLE IV  
Weight of each microsolder

Components	Mean Value (mg)	Standard deviation (mg)	Accuracy at $2\sigma$ (1%)
Substrate	0,263	0,05	$\pm 38$
Chip-carrier	0,407	0,034	$\pm 16,7$
Assembly	0,669	0,045	$\pm 13,5$

These measures have been performed with 1240 solder joints, it is interesting to note that the sum of solder weight on the chip-carrier and on the substrate is well correlated with the weight of solder of the assembly.

During the ageing and cycling tests samples were taken and analysed and metalographic cross-sections were performed on them near the interfaces (see Figure 2).

- solder joint/metallisation Au Pt (area 1)
- solder joint/chip-carrier (area 2).

**Analysis method** Scanning Electron Microscopy (SEM) and energy dispersive analysis of X-rays (EDAX) were used with a CAMEBAX system.

Metallic elements of the solder/metallisation couple were mapped and the concentrations profiles were recorded.

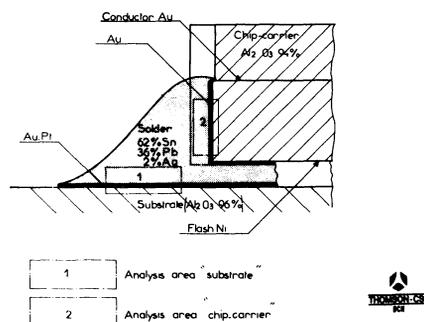


FIGURE 2

### 2.3 Results

To choose the characteristic X-ray of each element and to follow the evolution of their concentration EDAX was used.

The main metals used in the metallizations were the following: Sn, Pb, Ag, Au, Pt, W, Ni.

Looking at these diagrams and at the spectrum analysis, one can be confused by Au and W:

- Au,  $L\alpha = 1,276$  with LIF = 0,317
- W,  $L\beta = 1,281$  with LIF = 0,318.

Thus we excluded the L rays and choose the  $M\alpha$  rays with a crystal TAP and thus eliminated any ambiguity. Let us now analyse the influence of the various parameters listed in Table III.

*Influence of the reflow time at (to before the cycle and the ageing tests).*

- a) *Near the substrate:* Sn and Pb, no noticeable difference.  
Au, the dispersion in Sn Pb is more homogenous at 110 s (figure 3) than at 19 s (figure 4).  
Pt, the concentration does not vary.
- b) *Near the chip-carrier:* we can come to the same conclusion, the dissolution is more important than in the previous case at 110 s.

*Influence of thermal cycling for a reflow time of 19 s.*

- a) *Near the substrate:* On the metallographic cross-sections at 0 cycle (figure 5) and after 1000 cycles (figure 6) we note: a crack and an area with a different aspect between the substrate and the crack (thickness  $\sim 40 \mu\text{m}$ ).

If we compare the experimental X-ray mapping of Sn and Pb up to and after to under initial conditions (figures 7 and 8) with those of Sn and Pb after 1000 cycles an important segregation between Sn and Pb. This is probably due to the diminution of Sn solubility in  $\text{Pb}\alpha$  during the cycle temperatures ( $-55^\circ\text{C}$ ;  $+125^\circ\text{C}$ ).

The gold X-ray mapping at to (figure 4) and after 1000 cycles (figure 11) exhibits an extension of the gold rich area. Superimposing the Sn, Pb, Au concentrations, we note that the gold and tin-rich areas overlap.

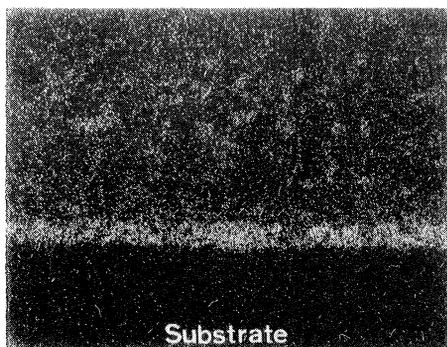


FIGURE 3 Au, X-ray mapping after reflow time of 110 s.

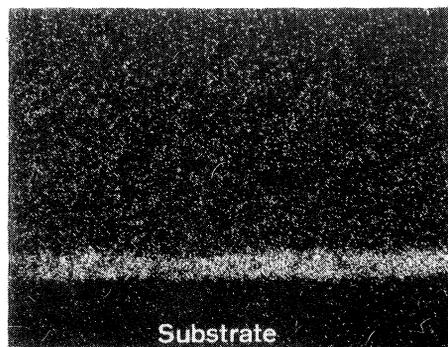


FIGURE 4 Au, X-ray mapping after reflow time of 19 s.

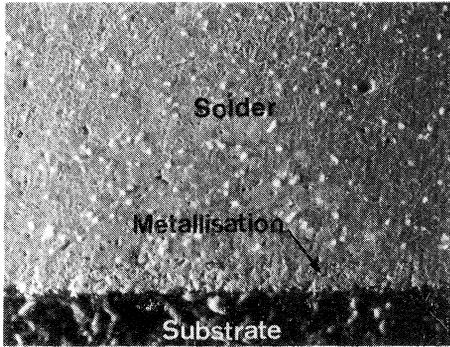


FIGURE 5 Metallographic cross-section near the substrate at 0 cycle (reflow time 19 s).

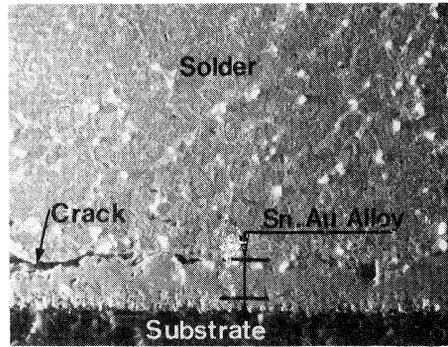


FIGURE 6 Metallographic cross-section after 1000 cycles (reflow time 19 s).

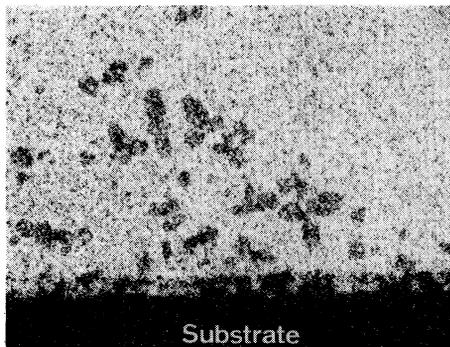


FIGURE 7 Sn, X-ray mapping before ageing (reflow time 19 s).

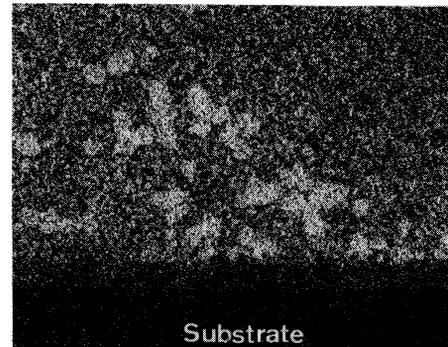


FIGURE 8 Pb, X-ray mapping before ageing (reflow time 19 s).

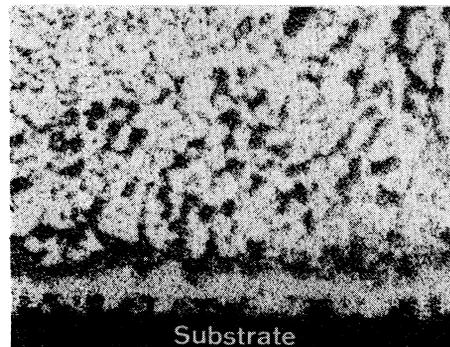


FIGURE 9 Sn, X-ray mapping after 1000 cycles (reflow time 19 s; substrate).

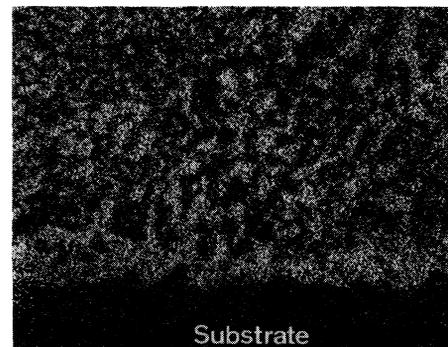


FIGURE 10 Pb, X-ray mapping after 1000 cycles (reflow time 19 s; substrate).

If we compare this area with the cross-section (figure 5) we can note the coincidence of the areas (cf. Discussion).

We can also note that the crack is between this alloy area and the matrix Sn Pb.

- b) *Near the chip-carrier:* The cross-section up to (figure 12) and after 1000 cycles (figure 13) presents the same rather large differences. We can also note a crack at

the same interface of these areas. If we compare the Sn and Pb X-ray mapping of the initial time (figures 14 and 15) 1000 cycles with the Sn and Pb X-ray mapping after 1000 cycles (figures 16 and 17), we are able to note a very important segregation.

As far as gold is concerned the evolution is the same as that which we can see near the substrate. The Ni and Ag concentrations do not vary significantly.

*The influence of the thermal cycles on 110 s reflow samples.*

- a) *Near the substrate:* After 766 h at 125°C, we noted on the Sn, Pb, Au X-ray mapping (figures 18, 19 and 20) a quasi-perfect coincidence of the area.

The gold and tin area overlap (zone A) on about 50  $\mu\text{m}$  from the substrate. Elsewhere we established the presence of a lead deficient area. This necessarily

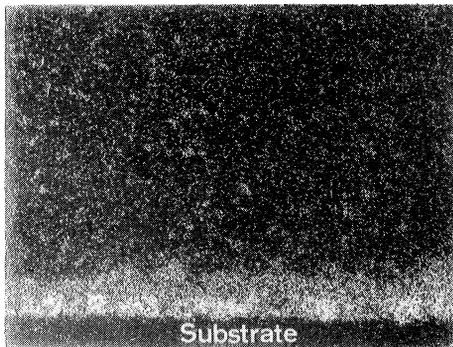


FIGURE 11 Au, X-ray mapping after 1000 cycles (reflow time 19 s; substrate).

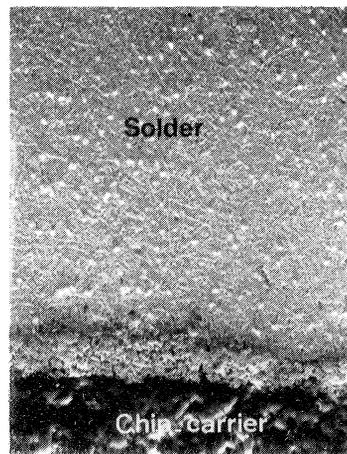


FIGURE 12 Metallographic cross-section before ageing (reflow time 19 s; chip-carrier).

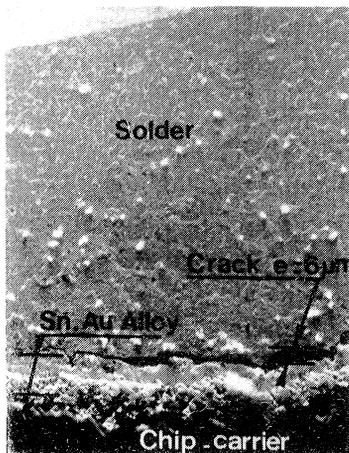


FIGURE 13 Metallographic cross-section after 1000 cycles (reflow time 19 s; chip-carrier).

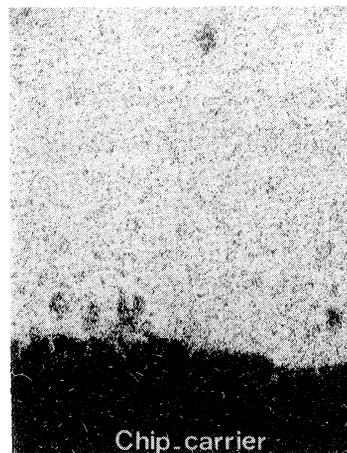


FIGURE 14 Sn, X-ray mapping before ageing (reflow time 19 s; chip-carrier).

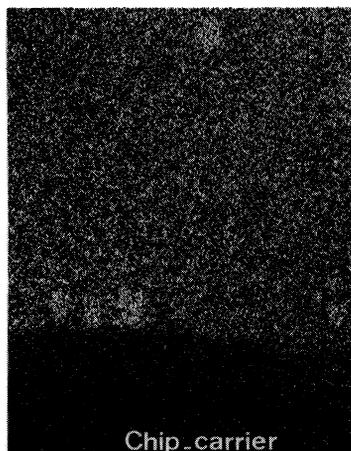


FIGURE 15 Pb, X-ray mapping before ageing (reflow time 19 s; chip-carrier).

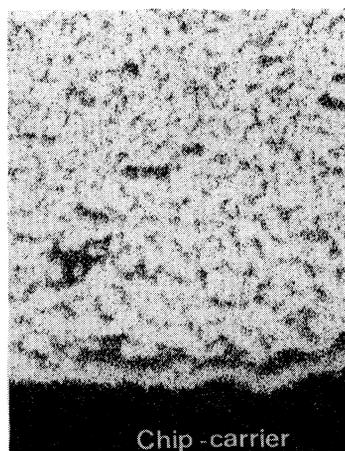


FIGURE 16 Sn, X-ray mapping after 1000 cycles (reflow time 19 s; chip-carrier).

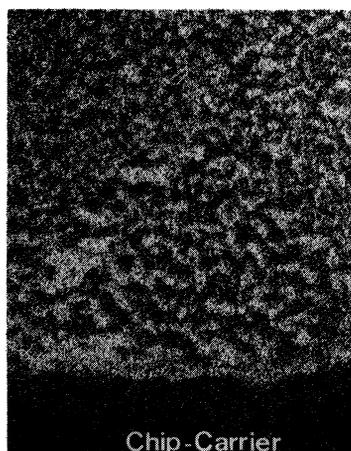


FIGURE 17 Pb, X-ray mapping after 1000 cycles (reflow time 19 s; chip-carrier).

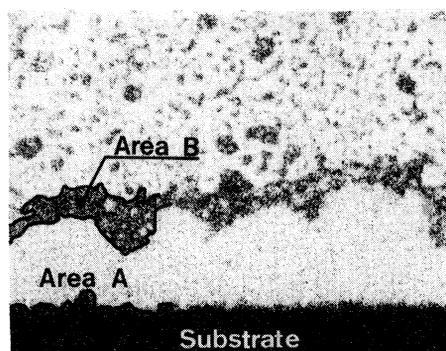


FIGURE 18 Sn, X-ray mapping after storage 766 h at 125°C (substrate).

leads us to think that there is, in this zone, the formation of a binary alloy  $Au_n Sn_m$ .

The zone (B) located above this alloy (figure 21) exhibits a zone rich in lead and deficient in tin and gold.

The metallographic cross-section of the analysis area (figure 21) exhibits two parts with very distinctive aspects. The part close to the substrate is perfectly overlappable with the area A, thus at an  $Au_n Sn_m$  alloy layer. The Sn Pb matrix exhibits after ageing the same segregated aspect seen before.

If we compare the micrographies before storage (figure 5) where no alloy area is detectable, with these after storage (figure 21), we can observe a rapid growth of the gold alloy phase.

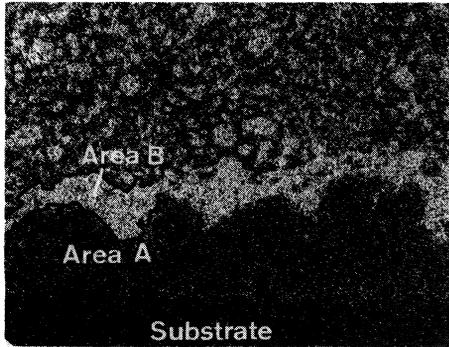


FIGURE 19 Pb, X-ray mapping after storage 766 h at 125°C (substrate).

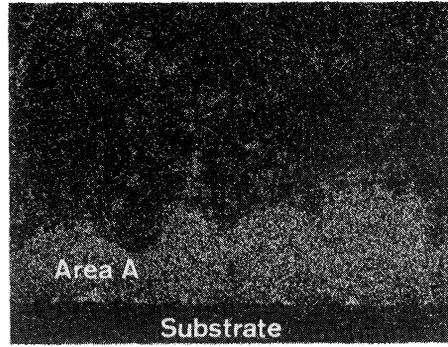


FIGURE 20 Au, X-ray mapping after storage 766 h at 125°C (substrate).

*b) Near the chip-carrier:* After a storage at 766 h at 125°C the tin, lead and gold X-ray mapping (respectively figures 22, 23 and 24) exhibit three separate areas: Pb rich-layer (zone E) (figures 22 and 23) similar to the former area B described before.

$Au_n Sn_m$  alloy area (figures 22 and 24) of mean thickness 12  $\mu m$ . This alloy area is less important than the substrate (area A 50  $\mu m$  thickness).

An area C in which Sn (figure 22) and Pb (figure 23) are deficient contrary to what has been observed near the substrate.

Knowing that there is a layer of nickel under gold, we have continued in all these analyses, the evolution of the nickel concentration (figure 25). This evolution was not very important, except after storage 766 h at 125°C.

In fact, on the Ni X-ray mapping (figure 25), we can observe a high concentration of this element at the upper limit of the area C. The Ni diffusion from the surface of the chip-carrier, to the limit of C, inhibits the formation of the compounds  $Au_n Sn_m$ . This specific effect is not seen near the substrate because nickel is not present. It is known that the Ni diffuses very quickly in gold; this effect is particularly common in thin film technology (Ni Cr + Au).

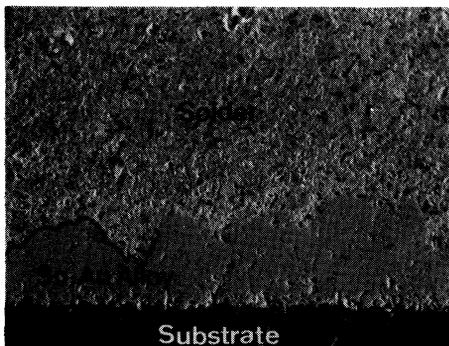


FIGURE 21 Metallographic cross-section (substrate) after storage 766 h at 125°C.

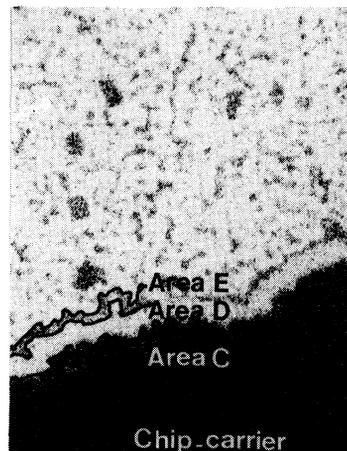


FIGURE 22 Sn, X-ray mapping after storage 766 h at 125°C (chip-carrier).

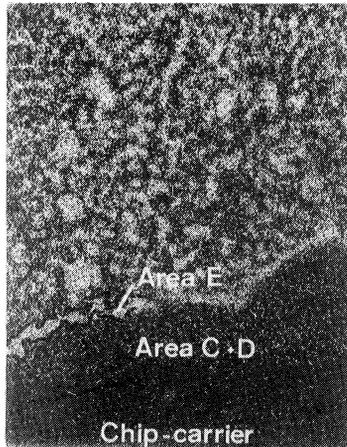


FIGURE 23 Pb, X-ray mapping after storage 766 h at 125°C (chip-carrier).

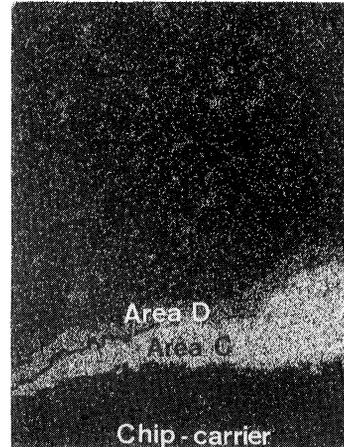


FIGURE 24 Au, X-ray mapping after storage 766 h at 125°C (chip-carrier).

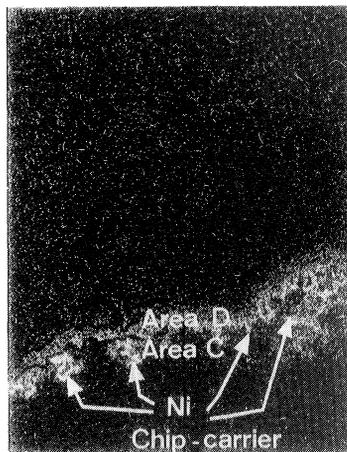


FIGURE 25 Ni, X-ray mapping after storage 766 h at 125°C (chip-carrier).

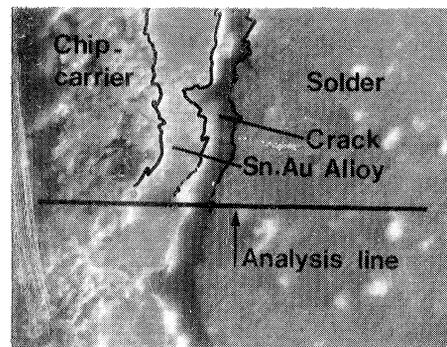


FIGURE 26 Metallographic cross-section through a crack.

#### 2.4 Discussion

The long ageing period intensifies the formation of intermetallic compounds. This fact allows us to confirm that the zones under observation during a thermal cycle, however less developed, are of the same type. We have noticed cracks between 500 and 1000 cycles, and we wanted to determine the concentration profile of Au, Sn and Pb near (figure 26).

X-ray profiles have been performed on these three elements (figure 27) and we note:

- the crack is at the interface  $Au_n Sn_m$  and Pb.
- Sn and Pb peaks clearly show the segregation between those elements after ageing.
- all peaks strictly correspond to segregations as we can see then on Au X-ray mapping of the analysis area (figure 28).

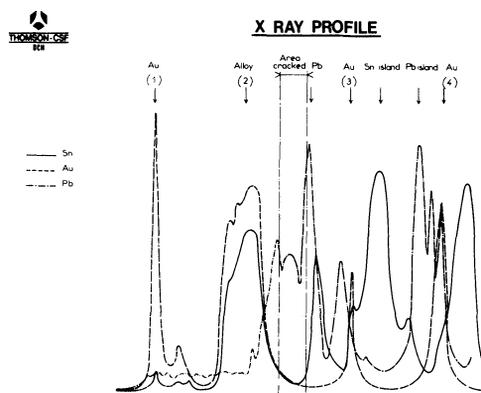


FIGURE 27 X-ray profile.

All these analyses after cycling revealed that the deterioration causes have to be looked for in the solder joint itself. This fact has added to the mechanical phenomenon due to the mismatching of linear expansion coefficients, substrate/components, as we previously demonstrated.<sup>4</sup> The development of microcracks takes place at the interface of the Sn Pb alloyed areas and Pb. Consequently, the suppression of gold would induce the absence of these areas.

We have to note that it is not realistic to measure the failure rate of the microcracks using common optical or electrical systems. We have seen the microcracks grow inside the solder. A non-destructive experimental method, the acoustic microscopy, will probably provide a method of detection. We have actually used this technique in TH-CSF. As far as gold is concerned, we think that we will be able to suppress gold on the chip-carrier and on the substrate.

### 2.5 Removal of Chip-carrier Gold

The chip-carriers have been dipped in a bath of Sn Pb at  $230^{\circ}\text{C} \pm 5^{\circ}\text{C}$  during different periods: 0,5; 30; 60 and 300 s.

The levelling was used to mechanically eliminate the gold rich solder. The Au X-ray mappings show after 0,5 s that the gold has been totally dissolved. These results have led us to add this operation to our fabrication line. It would be desirable for economical reasons to leave the Ni bare and to solder the chip-carrier directly on to the Ni layer. It seems that TEXAS is looking at the possibility of delivering the monolayer chip-carrier without gold.<sup>11</sup>

The substitution of a gold conductor with a copper one on the substrate has been closely examined in our Company.<sup>1,2</sup> It has been found in the last year that copper multilayers production is effective in THOMSON-CSF. The concept chip-carrier, associated with non-noble metals multilayers, allows investigation of the utilisation of a great many micropackages on large substrates (greater than  $10 \times 10$  cm) but the problem of mounting with a high yield stays.

## 3. MOUNTING OF COMPONENTS

Different techniques of mounting using several methods of heat transfer are used:

- convection (IR furnace)

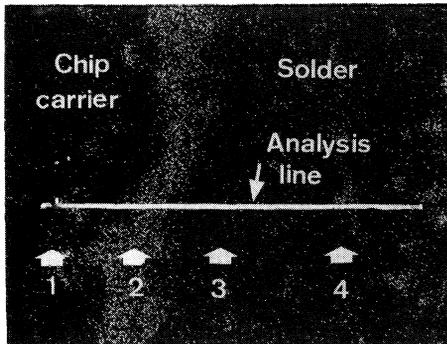


FIGURE 28 Au, X-ray mapping after 1000 h at 125°C.

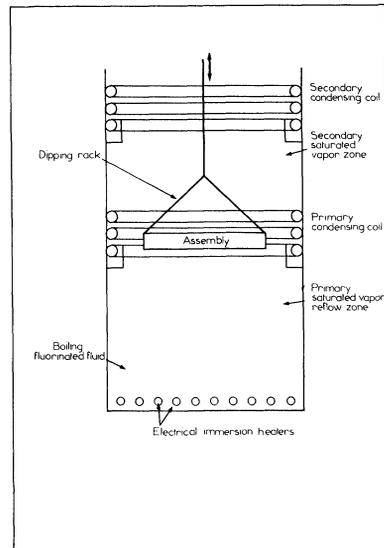


FIGURE 29 Schematic, representation of the basic condensation soldering system.

- conduction (heating, belt reflow soldering system or dipping in a solder bath)
- condensation (vapor phase reflow).

With the analysis results we made on micro-solders and mounting of tin-lead, we have determined the following criteria which must be maintained:

- 1) Temperature uniformity independent of the dimensions of the components.
- 2) Reflow temperature lower than the intermetallic compounds temperature formation.
- 3) The flux to be as little active as possible and easily cleanable. Avoid oxidation and decomposition of this flux. The flux oxidation begins at 170°C and about 290°C the carbonisation is important.

Until now these three criteria were not satisfied by any of the reflow processes. The classical reflow furnace which necessitated a very high temperature peak, to give enough energy to the components with high thermal mass, did not satisfy the criteria.

Dipping in solder bath at  $\pm 230^{\circ}\text{C}$  or in a wave at  $260^{\circ}\text{C}$ , if satisfying the criteria 1, does not respect the other two. The belt reflow soldering does not ensure criteria 1 because the thermal resistance is not predictable either between the down face (the substrate/belt), or the up face (substrate/components) — except for the solder paste.

The vapor phase reflow accepts these criteria. With this process, the potential energy (latent heat of condensation) is stored in the vapor and released during the change of phase to liquid during condensation. The schematic view of the basic condensation soldering system is shown in figure 29.

For two years, we have used this technique in TH-CSF therefore. A task group comprising different specialists from Divisions and subsidiaries of THOMSON-CSF (PC board, connector, hybrid, . . .) settled the specification.

All the trials started with a HTC machine type 14-19 to find the optimum reflow process. Currently a french vapor phase soldering system PIEZOCERAM 30-40 is being used.

### 3.1 Results

Four copper conductor layers on alumina substrate with chip-carriers (from 16 to 64 contacts) are used (figure 30). The temperatures are measured at 3 levels:

- Level 1: inside alumina substrate holes (0,6 mm of diameter) have been made to insert a thermocouple to measure the mass temperature.
- Level 2: a flat thermocouple thermally linked on the substrate permitted recording of the surface temperature.
- Level 3: the temperature inside the chip-carrier was measured by the classic method with a diode (1N 914) to permit us to follow the temperature profile during the cycle.

Typical thermal responses at these levels are shown in figure 31. We can see that:

- the temperature inside and on the substrate are close (197°C and 204°C),
- the temperature in the silicon diode is lower than 165°C.

The selection of the setting points has been done to minimize the temperature-time couple. On the curves (figure 32) surface profiles are presented. On the Table V we notice that the higher the peak temperature, the longer is the time reflow.

The peak temperature also depends on the speed of dipping at constant power and decreases when the speeds increase.

TABLE V  
Preparation parameters for solder dipping

Speed of dipping (cm . s <sup>-1</sup> )	Power (Kw)	Temperature (°C)		Reflow cycle above 183°C (s)
		On the substrate	Inside the substrate	
v <sub>1</sub> 1,07	10	204	197	110
v <sub>2</sub> 1,44	10	198	193	46
v <sub>3</sub> 2,09	10	193	184	14
v <sub>4</sub> 2,56	12,5	205	186	24

If we want to reduce the total cycle we have to increase the down speed but the up speed will be limited by thermal “effects 0”. The FC70 vapours of the F 7 are evaluated by the system. This observation and the shapes of the curves are typical of the thermal capacity charge. The behaviour of the thermal response is typical of a Newtonian heat flow and is governed by the following:

$$\ln \frac{T - T_{\infty}}{T_0 - T_{\infty}} = \frac{hS}{\rho CV} t$$

- C specific heat of the body
- $\rho$  density of the body
- h average surface conductance
- S surface area
- T temperature
- T<sub>∞</sub> temperature of the fluid
- T<sub>0</sub> initial temperature

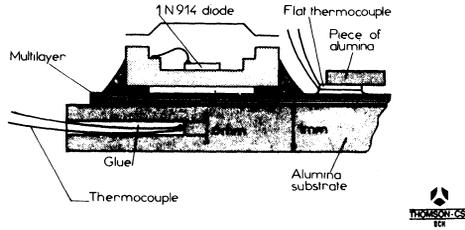


FIGURE 30 Section of the test specimen.

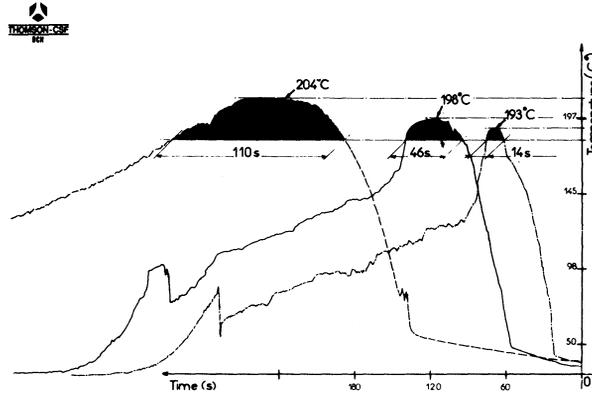


FIGURE 31 Typical thermal response of specimen during vapor phase soldering cycle.

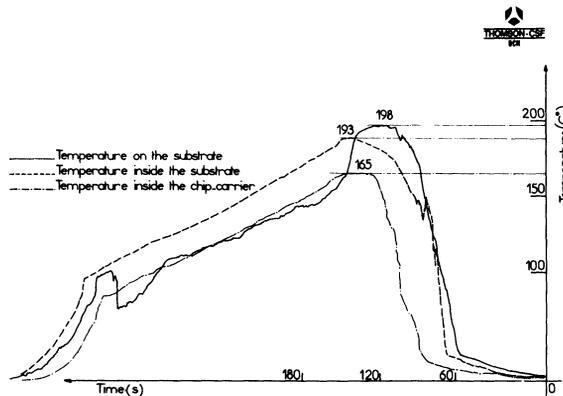


FIGURE 32 Typical thermal response of specimen with different soldering cycle.

The heat transfer ratios were obtained from a semi-log plot of the data on figure 33.

Such a plot indicates that the thermal response is exponential, and, hence, the slope is proportional to the heat transfer coefficient. The plots  $n^{\circ} v_1, v_2$  and  $v_3$  showed two separate linear segments indicating two separate time domains with exponential temperature rise. We can see that the change of the slope is always at the same temperature

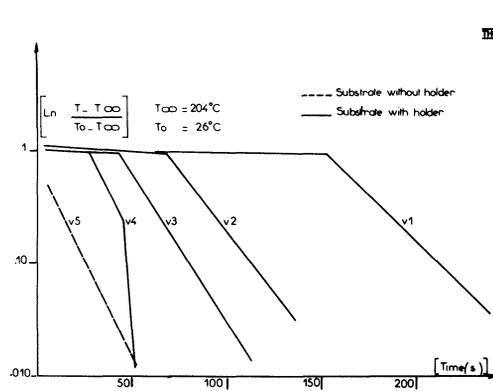


FIGURE 33 Temperature Vs time.

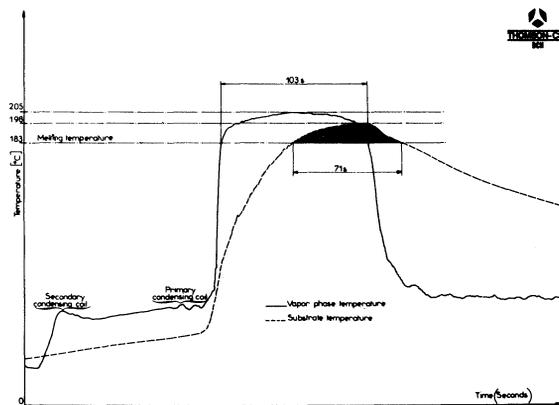


FIGURE 34 Typical thermal response of large multilayer assembly during condensation soldering cycle.

(48°C), the boiling point of trifluorotrichloroethane (flugene 113 from Rhone-Poulenc). The curve  $v_4$  consists of three segments with different slopes, but with a heating power higher than for the curves  $v_1$ ,  $v_2$  and  $v_3$ . The curve  $v_5$  was obtained with the same test specimen but without the holder. Only the thermal capacity of the substrate is to be considered.

Downward and upward speed are quasi instantaneous, the substrate has been directly dipped in the primary vapor phase. It will be seen that the thermal charge of the holder when parallel to the substrate does not influence the slope of  $v_5$  and  $v_1$ ,  $v_2$ ,  $v_3$  are very close. This reflow process has been for different assemblies:

- Gold multilayers with five levels (2,3 × 1,6") and 20 chip-carriers.
- Copper multilayers (1/2 ATR 6,5 × 3,5") with 60 chip-carriers.
- Thermal print head (figure 35) (10 × 2") with 36 chip-carriers with 40 mils pad each every substrate has 1152 solder joints; the defect rate after reflow was less than 1/1000.

The reflow cycle now in operation is presented on figure 34, the reflow cycle time, 63

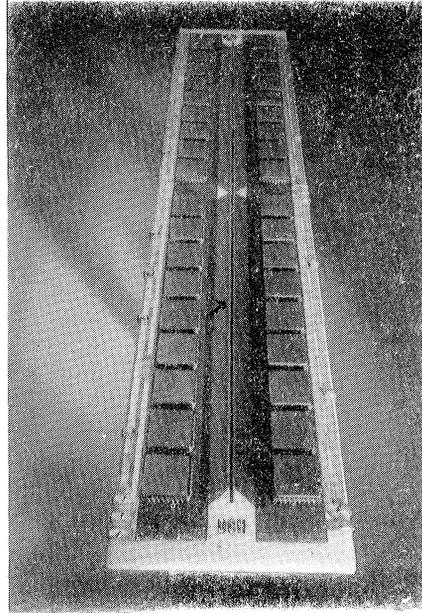


FIGURE 35 Thermal print head (250 × 50 mm).

seconds, has been determined, with 3 parameters in mind:

- The downward speed is the same as the upward speed.
- The upward speed is important in order to avoid vapour loss.
- Reflow time must be sufficient to insure good wetting.

#### 4. CONCLUSION

The new possibilities of chip-carriers associated with alumina substrates or with substrates which have close expansion coefficients as, for example, the Invar/Cu colaminated, allows the mounting of leadless components.

This “chipardisation” does not necessitate holes as in classical P.C. boards. It enables additional methods like screen printing to be used, which are economically feasible, mainly since copper multilayer became available from Dupont and Cermalloy and LEP paste became available. These methods are also probably valid for the mounting of plastic micropackages onto more dilatible substrate as enamelled steel or PC board.

Solder joints analysis after cycling and ageing have shown:

- $Au_n Sn_m$  intermetallic compounds formed in the area A.
- Pb rich area (B) segregated above the alloy area.
- With Ni (chip-carrier) the presence of this element quickly diffused in gold and inhibited the formation of the Au-Sn compound.
- Pt did not significantly diffused in Sn-Pb.
- The same holds for Ag contrary to the what is common believed if field or humidity migration is confused with diffusion.
- Cracks appear between 500 and 1000 cycles.
- These cracks take place at the interface Au-Sn/Pb area.

It was noticed that reflow time at low temperature (183°C to 205°C) has little influence on the behaviour of the joints during the thermal cycle.

As a consequence of this study the process has been modified according to the following:

– Gold removing of the components then tinning; copper tinned substrate.

Gold substitution is not only an economical necessity but is technically a necessity in order to improve the solder reliability.

We need the manufacturers of chip-carriers to modify the surface metallurgy to chip-carriers, and the paste manufacturers to accelerate the development of copper based systems.

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