A SHORT COMMUNICATION — DETERMINATION OF CHIP AND SUBSTRATE TEMPERATURES

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Through making use of the analogy between electrical current and thermal heat flow, thermal calculations for thick film substrates may be undertaken using standard computer aided design programs such as SPICE 2. Chip temperature and substrate isotherms for various conditions can readily be determined. Parameters considered in this paper are chip position on substrate, with and without heat sink, number of chips on a substrate and substrate materials.

1. INTRODUCTION

The continuing increase in size of monolithic circuits and the size reduction of resolvable features will result in VLSI chips of the future with higher power densities, larger absolute power dissipation and higher pin counts. Thick film circuits can provide a fine definition multilayer interconnection board to mount these new devices. The problem of heat removal from a thick film substrate is part of the overall system design with a necessity to examine those factors that influence the final chip operating temperature.

This paper describes results obtained by simulation using the SPICE 2 program. Parameters considered are chip position on the substrate, number of chips and substrate material.

2. SIMULATION OF THERMAL HEAT FLOW

The heat flow problem of a system can be solved using conventional electronic analysis programs such as SPICE 2 if the analogy between thermal heat and electrical current flow is utilized. The two equations are summarised in Table I.

Consequently thermal power flow can be represented by current sources, temperature by voltage and thermal resistance by electrical resistance.

To transform the continuous substrate into a simple lumped network, substrates were subdivided into unit cells using a uniform grid. Being a numerical analysis approach

<table>
<thead>
<tr>
<th>Analogy between electrical current and thermal heat flow</th>
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<tbody>
<tr>
<td>Electrical flow</td>
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<tr>
<td>$E = IR$</td>
</tr>
<tr>
<td>where $E$ is the potential difference (volts)</td>
</tr>
<tr>
<td>$I$ is the current flow (amps)</td>
</tr>
<tr>
<td>$R$ is the electrical resistance (ohms)</td>
</tr>
</tbody>
</table>
(Newton Raphson method) the fineness of the grid and maximum size of substrate could be severely limited by the size of computer memory. In the examples given here a 0.1 inch (2.54 mm) grid on 1 x ½ inch (25.4 x 12.7 mm) substrates is used. Figure 1 shows in three dimensions a unit cell together with the placement of several cells to show edge effects. Away from the edges horizontal (top and bottom) resistors have value 2Rs and vertical resistors Rv.

To allow for radiation and convection of heat from the substrate to ambient, a further series of resistances are added from each node to the common reference node of ambient temperature. In a similar way heat sinks can be accommodated by an additional resistor from each relevant node to ambient, the resistor value being the appropriate fraction of the thermal resistance of the heat sink.

Chips placed on the substrate can be simulated by thermal resistors to appropriate nodes depending on chip position, these resistors being fed by a constant current source, the current being proportional to the chip dissipation. Thus a single chip mounted on a

![Diagram of resistors](image)

(a) Unit cell determined by grid size

![Diagram of edge effect](image)

(b) Edge effect

FIGURE 1  Transforming a continuous substrate into a lumped network using a grid.
DETERMINATION OF CHIP AND SUBSTRATE TEMPERATURES

substrate can be simulated by a passive resistor network as shown in Figure 2.

To simplify feeding this large network in as data to SPICE 2 a simple program was written to generate the data file.

Parameters for various substrates were extracted from manufacturers' literature and are shown in Table II.

With the porcelain steel the outer layers of porcelain were 9.6 mils thick and the central steel 37 mils thick.

While SPICE 2 allows temperature coeffs for resistors, it does not include voltage coefficients. Consequently, the nonlinear effects of thermal conductivity cannot be included. Where possible the value for thermal conductivity at the appropriate temperature was used as datum. Datum for the thermal resistance of a substrate to air was measured by heating a substrate in still air and measuring surface and ambient temperatures. Sub-

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**TABLE II**

Thermal data for substrates

<table>
<thead>
<tr>
<th>Substrate Material</th>
<th>Thermal conductivity W/m.K</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>20°C</td>
<td>25°C</td>
</tr>
<tr>
<td>Alumina</td>
<td>26.3</td>
<td>20.1</td>
</tr>
<tr>
<td>Berillia</td>
<td>280.3</td>
<td>200.8</td>
</tr>
<tr>
<td>Porcelain Steel</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Steel Section</td>
<td>73</td>
<td>69</td>
</tr>
<tr>
<td>Porcelain Section</td>
<td>1.0</td>
<td></td>
</tr>
</tbody>
</table>
strates with and without thick film printing were used and the difference in thermal resistance between substrates with and without printing was small, being less than the estimated accuracy of experimental measurement. For a one inch square alumina substrate, a thermal resistance of 38.5°C/watt was measured and used in the simulation program.

3. RESULTS OF THE THERMAL SIMULATION PROGRAM

The simulation program simply provides the temperature (voltage) at each node in the system. From these both isotherm and chip temperatures can be readily derived.

Four parameters were investigated, namely the effects of chip position on the substrate, a comparison of the three substrate types in terms of final chip temperature, the influence of heat sinks and thermal profiles for multiple chips on a substrate.

Figure 3 shows the various positions selected on the substrate. A thermal resistance of chip to substrate of 2°C/watt is assumed throughout.

Considering first the effect of chip position, chips were mounted singly on a 25 mil thick alumina substrate and fed an input power of 2 watts. Table III gives the chip temperature in degrees Celsius above ambient temperature for each position.

A selection of isotherms are given in Figure 4. Node temperatures above ambient are also shown.

Measured temperature values reported by Stephens⁴ give the same trends although actual temperatures are lower since measurements were not taken in still air conditions.

Returning to Table III, it is interesting to note the effects when a large heat sink is added. For the same substrate but now attached to a heat sink with thermal resistance of 1°C/watt and chips in the same positions but with 10 watts input, chip temperatures are considerably lower.

![Figure 3 Chip positions investigated.](image)

![Table III Chip temperature for various positions on a substrate](image)

<table>
<thead>
<tr>
<th>Condition</th>
<th>Temperature °C for chip position</th>
</tr>
</thead>
<tbody>
<tr>
<td>No heat sink 2 watts in</td>
<td>106 117 141 127</td>
</tr>
<tr>
<td>With heat sink 10 watts in</td>
<td>92 94 114 96</td>
</tr>
</tbody>
</table>
If now we retain both the heat sink and the chip in central position 1 but vary the substrate material, then the calculated chip temperature for 10 watts power into this chip are:

- Alumina: 92°C above ambient
- Porcelain coated steel: 60°C above ambient
- Berillia: 41°C above ambient

The results show that both porcelain coated steel and berillia offer thermal advantages over the more usual alumina substrate.
Finally, various chip combinations were examined. As expected, there is some advantage in spreading the heat load by mounting, say, three small chips each dissipating one-third the power than by using a single chip. Figure 5 shows, by way of example, the isotherms and node temperature for the case of 3 chips at locations 1, 4 and 5 each dissipating 3/4 watt. With no heat sink attached, chip temperatures are all less than 98°C above ambient. (Compare Table III)

4. CONCLUSIONS

The use of the simple electrical/thermal resistance analogy allows existing network analysis programs to simply and quickly predict substrate isotherms and chip temperatures, thereby assisting in the layout of circuits on substrates, selection of substrate material, and design of heat sink if needed.

REFERENCES

1. L.W. Nagel, “SPICE 2: A computer program to simulate semiconductor circuits”, Electronics Research Laboratory, University of California, Berkeley. Memorandum No. ERL-M520.
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