FINE LINES IN A THREE DIMENSIONAL INTERCONNECT †

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The techniques for the generation of fine lines on rigid and flexible printed circuit boards are reviewed, and it is shown how the tracking on the interconnect can be made to match the requirements of chip carriers, TAB chips or beam leaded or wire bonded chips directly mounted.

The use of fine line techniques on planar substrates can be adapted to provide a low cost, high density interconnect which offers a truly three dimensional connection capability without the use of a "back wiring panel". Such a three dimensional interconnect can offer opportunities for improvement in the removal of heat from high dissipation chips, thus offering significantly increased reliability.

1. INTRODUCTION

The term 'fine lines' can mean different things to different people at any given time. For this paper, the width of line generally regarded in the PCB industry as the lower limit for satisfactory bulk production of boards is taken as the upper limit for fine line work. When the line widths used on such boards are reviewed, and examples of good, state of the art designs are plotted as in Graph 1, it is possible to draw a smooth curve showing the boundary of fine lines decreasing by 30% per decade, and standing in 1982 at around 0.2 mm.

There are examples of boards which lie well below this curve, indicated with the symbol ⊗, but they are mainly development projects which helped to indicate the likely future trends.

The amount of interconnect possible in a single unit must also depend on board size, but this is much harder to define in any meaningful way. Some sectors of the industry, such as aerospace, have to work within the confines of limited ranges of case sizes, while other areas such as pocket pagers or calculators and some types of electronic toys or games require that the size of the product be minimised. When such boards are discounted, and the sizes of boards used in large equipments are considered, it can be seen that there has been fairly steady growth in the sizes of through hole plated boards over 20 years, but that growth is levelling out at a larger dimension of around half a metre.

Graph 2 shows a rough curve of sizes of the larger boards in bulk production for general industrial and commercial digital logic systems.

2. THE NEED FOR FINER LINES

Fine lines may be needed to match the pitch of connecting pads on semiconductor chips. If bare chips are to be mounted, then there will be a need for lines and gaps down to around 0.05 mm. Most chips mounted on boards are packaged in some way, and connections to packages can usually be achieved with tracks and gaps of up to 0.5 mm width.

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GRAPH 1

GRAPH 2

However, this figure makes no allowance for tracks which must pass through a row of package pads or pins without connecting to them. On most PCBs the packing density achievable is limited by the tracking which can pass given rows of component terminations rather than by that which connects to them. The sizes of holes, pads, or pillars needed to form the connections to the devices carried and also to change sides or layers on the board can have a decisive effect on the packing density.

The use of surface mounted devices and plated pillars for layer to layer connections on multilayer boards can yield high tracking and packing densities, but usually only at a high interconnect cost, possibly coupled with high line capacitance. What is of major interest is the amount of interconnect tracking which can be accommodated on a double sided board, using normal through hole component mounting techniques, and plated via holes.

FIGURE 1 Typical hole pattern

A fairly conventional component mounting pattern as shown in Figure 1 can be considered, and the number of tracks which can be run through the pattern, assuming equal width tracks and gaps, can be assessed. Via holes placed on the same grid lines as the existing component mounting holes, or placed where the tracks can be bent round to pass the pads, will not affect the numbers of tracks which can be run. It must be assumed that tracks on one side of the board will run vertically through the pattern, with those on the other side horizontal. Graph 3 shows the numbers of tracks which can be accommodated per square cm of board area, averaged over a large area, and using the limits of fine lines from Graph 1. It can be seen that there are significant steps in the graph as first 1, then 2, 3, or more tracks can be run between pairs of pads on 2.54 mm centres. Pad diameters of 1.27 mm have been assumed. It can also be seen that through the 1980s the use of fine lines will allow a sharp increase in the tracking densities achievable. The smooth curve of Graph 3 allows a 'learning zone' which assumes that board designers will be making fully effective use of the tracking densities available only as the next step occurs.

It must be appreciated that such limit tracking densities will occur only in very limited areas on any practical boards.

Fine lines may also be needed for special applications, such as PCB heads for electrostatic printers or in microwave work.

3. LIMITS ON LINE WIDTHS

Good filmwork is essential for fine line work, but this should not prove to be a limit, since semiconductor makers, who use workpieces about one fifth the length of a PCB can process films with lines and gaps of 0.002 mm or less.

The first real limitation in PCB work lies in etching. As the etchant dissolves the copper, it attacks the side walls of the tracks and pads as well as the flat surface of the copper, undercutting the resist as shown in Figures 2 and 3. The use of well designed

FIGURE 2 Undercut

FIGURE 3 Undercut with normal films

spray etchers and properly formulated etchants will minimise such undercutting but it will not eliminate it. Any over-etching will, of course, increase the undercut. On well made boards it is wise to make an allowance for undercutting on each edge of about 60% of the thickness of copper to be etched. Clearly the best way to minimise the effect of undercutting is to arrange the work such that only the thinnest possible layer of copper must be etched.

Lines of a desired finished width can be achieved by adjusting the filmwork such that all features are oversize by the anticipated undercut on each edge. Unfortunately, on densely tracked boards, this may mean that the gaps between adjacent tracks, or between tracks and pads on the film become so narrow that insufficient etchant can penetrate so that the expected undercut may not occur, and there may even be a risk of incomplete etching, whereas where there are no features closely adjacent, the full undercut still occurs. (Figure 4).

FIGURE 4 Loss of gap width with adjusted films

Feature sizes can also change during plating, as the plated-on-metal grows out over a thin resist as shown in Figure 5 on the left. Such growth during plating can be controlled by using a dry film resist thicker than the metal layer to be plated, as shown on the right of Figure 5.

FIGURE 5 Growth of plating

The use of pattern plating techniques with a dry film resist on laminates clad with thin copper foil, in the range 0.005 mm to 0.012 mm, can enable boards to be made with lines and gaps down to around 0.1 mm. Below this level the thickness of the resist and its protective cover film can cause problems with diffusion and refraction of light during exposure.

These optical effects can be overcome, at least partially, by the use of collimated light, or by lasers or electron or ion beam exposure systems. It is possible that the latter may be driven directly from NC data, eliminating the need for films.

Below 0.1 mm width lines the adhesion of the copper to the base laminate may have to be improved if boards are to withstand rough handling. Good adhesion implies a good keying of the copper to the base, and this can make clean etching of thin clad laminate difficult without some noticeable undercut. It is likely that for very fine lines improved additive techniques using dry film type resists may yield the best results.

When gaps are reduced below about 0.2 mm, the electrical properties of the board, especially cross talk, may impose a limit on track densities. Generally the use of fine lines on double sided boards will yield low capacitance lines with characteristic impedances of around 150 ohms, which are very much better suited to TTL or MOS devices than the broader, higher capacitance lines on multilayer boards.

4. OVERALL PACKAGING PHILOSOPHIES

Most of the needs for fine lines arise because of the requirements to run tracks past integrated circuit sites but not connecting to the packages. The use of planar boards, often

carrying 200 or more packages, all plugged into back wiring of some form, usually means that other than at the outer edges of the boards a high percentage of the tracks are passing active devices without connection to them, and the average length of tracks may be fairly high, even with the use of fine lines.

It is not difficult to see from Figure 6 that the use of fine lines alone will not yield a satisfactory solution to the overall interconnect problem, and low average track lengths must imply very high packing densities, often with consequent thermal problems.

FIGURE 6 Conventional planar card packaging. Tracks linking packs A-A and B-B-B both pass many other packs and cannot be made really short

5. THREE DIMENSIONAL PACKAGING

A better solution to the overall interconnect problem must lie in a truly three dimensional packaging format. Such a three dimensional format should be capable of easy, cheap manufacture, and should also be capable of being tested in a planar form. These requirements can be met by the use of folded flexible or flexi-rigid circuits as patented by Exacta Circuits Ltd.

The package comprises vertical areas, which may be rigid, carrying single columns of packages or bare chips, between which are flexible areas on which contact fingers are plated up to a height above the surface of the cover coat. Compliant spacers mounted on guide bars separate the corrugations of the circuit, and press the fingers of one layer into contact with the fingers on an adjacent layer as shown in Figure 7. The assembly can be unfolded and laid flat for testing, with simple jumper links in a frame connecting the contact fingers.

FIGURE 7 Flexi-rigid 3D packaging

Any package on a conventional board can make connections to only four adjacent packages, whereas the folded 3D form offers eight effectively adjacent packages as shown in Figure 8; and if the compliant spacers carry connections and the fingers on the two

FIGURE 8 Direct connections to adjacent packages

sides of the flexible portions are connected by via holes, there can be access to 16 packages without a track needing to pass any other package. The 3D format is also an excellent vehicle for bus oriented systems, where a complete address or data bus can be run in the third dimension.

A variant of this three dimensional packaging is the use of rigid, parallel boards, with columns of packages and connector fingers, separated by compliant connecting strips. The compliant strips can be in the form of plastic bars which carry sprung contacts similar to those used in 'bed of nails' board testers; or they could be formed from the compliant strips made up of alternate conducting and insulating rubbery materials, or pieces of metallised flexible circuit material could be wrapped round compliant spacers to form the connections.

When the whole circuit is made on a double-sided flexible laminate, the base material can be back etched or laser cut out of the package mounting areas to leave the plated up ends of tracks projecting in the form of inverse beam leads to which chip carriers or bare chips can be directly bonded. Cooling and environmental protection for bare chips can be achieved by immersing the entire assembly in an inert liquid, possibly one which can be allowed to boil where it contacts the chips, thus enabling use to be made of the latent heat of evaporation.

External connections to the unit can be made with matching contact fingers on rigid front and back plates, and also at the ends where the successive layers of the flexible circuit are folded over.

6. CONCLUSIONS

With the use of minimum lines and gaps of 0.1 mm, a three dimensional package offers an extremely powerful interconnect capability without increasing the packaging costs significantly above those of currently used planar interconnects.