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THICK FILM CIRCUIT LAYOUT AND EXTRACTION OF PARAMETERS USING THE MAGIC LAYOUT EDITOR

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A Technology file for the Magic layout editor has been developed in order to enable thick film circuit designers to evolve fast solutions for layout with design rule checking, and plotting of the masks of multilayer hybrid circuits. The hybrid design system developed provides for device placement, and automatic routing techniques, in thick film circuits. Device placement is done by recalling from the library the pad pattern that corresponds to the device to be positioned. Automatic routing is implemented not only in multilayered circuits but also in single-layer technology (i.e. two possible types of metal routed on the bare substrate) where dielectric tiles are automatically created at metal crossings, when an electric contact is not desired.

1. INTRODUCTION

The Magic version 4 graphical layout editor included in the 1986 VLSI Tools release from the University of California at Berkeley[1] is a popular package for graphics generation, circuit extraction, and simulation for nMOS and CMOS VLSI circuits. Magic is technology-independent and consequently requires a technology file to describe the layers and the design rules of a particular fabrication technology.

Also, Magic includes incremental design rule checking, automatic routing, CIF (Caltec Intermediate Form) and GDSII (CALMA format) input and output, allowing for interfacing with various plotting devices and a plotting feature which permits areas of the layout to be zoomed or compacted, without having to worry about design-rule violations being created. Magic is based on the Mead–Conway style of design. This means that it uses simplified design rules and circuit structures. The simplifications result in slightly less dense circuits since Magic uses a Manhattan layout style (i.e. edges are vertical or horizontal) and lambda scaled grid, where lambda is the size of the smallest feature which can be drawn. The Manhattan style limits feature shapes to those that follow the X and Y axes, and such a conservative design costs 5–10% in layout density. The physical dimension corresponding to a lambda unit is specified during circuit extraction or CIF or GDSII file generation.

In Magic, a circuit layout is a hierarchical collection of cells. Each cell contains: coloured shapes, that define the circuit's structure, and its eventual function; textual labels attached to the coloured shapes, in order to be able to manage the layout and provide a way of communicating information between various synthesis and analysis tools; and subcells which are instances of other cells.

When a layout is edited with Magic, the system automatically checks design rules incrementally, meaning that the DRC acts on the most recently modified area in the layout and flags layout errors if there are any. In the case of finding a rule violation, Magic will display little white dots in the vicinity of the violation. The dots will remain on layout until the violation is corrected. Correction of the violation is facilitated with the use of special commands which allow the user to get information about the errors occurred.

In Magic, mask layers are represented by tiles, which are layout segments of maximum width and length in a contiguous region and are made of material of the same abstract layers. The design rules are applied at the edges between the tiles in the same plane, in a hierarchical approach; each time a structure is utilized, only the interaction between the structure and its surroundings is checked[2]. The algorithm analyzes the hierarchical nature of the design and checks the DRC violations by examining each cell and the interaction of the cells the first time they are encountered.

The 1986 release of VLSI Berkeley tools incorporated also, a circuit or node extractor program that takes a CIF file and produces as output the underlying electrical network, and other information such as the length/width ratio of each transistor, the resistance and capacitance of each connecting wire, etc. The output of the circuit extractor can only be used by switch-level simulators, such as ESIM[3], to verify functional correctness, whereas the use of a parasitic extractor instead would provide data for timing simulators.

Magic runs on several hardware configurations; in our case Magic was installed on a SUN 3/60 work station.

2. THE TECHNOLOGY FILE

The technology file (see Appendix I) contains all information on what planes will contain the tiles, what layers will be used, and by what names and colours they will be represented. Also, all design rules, such as minimum widths, spacings, overlaps, and extensions are specified. Descriptions of what new tiles can be composed by painting one layer over another are specified in the technology file. Magic can be directed as to which technology is to be used by specifying a flag on the command line when Magic is run.

The version of the technology file proposed here is based on the technology file for scmos and it may consequently replace it without the need to recompile Magic. This means that any system running Magic with the standard technology file for scmos, can without any other modification run Magic with the technology file for hybrid circuits. The technology file for hybrid circuits supports one and two metallization layer technologies. The designer is allowed to choose from up to four resistor pastes per metallization layer. The scmos technology file with minor changes can also support three, four, etc. metallization layer technologies but recompilation of magic would be needed.

This implementation exploits fully Magic's built-in capabilities for circuit parameter extraction, automatic routing, and design rule checking. The circuit element

parameters and the design rules may have to be altered to fit the technology that is going to be used for the implementation of the designed circuit. The design rules also have to be modified to conform with the requirements of each fabrication facility.

The two metallization layer technology is described in the following. The one metallization layer technology may be implemented by using only one of the two sets of resistor pastes and metal lines provided by the technology file. In the proposed implementation four planes have been used:

1st PLANE: The first plane includes the first metallization layer and the resistor pastes associated with it. There are also two types of pads: a metal-type for discrete components (i.e. metallization patterns for connecting to the circuit under design a] SMDs which must be soldered, and b] dies of ICs which must be wire bonded) and a solder-type for printing solder paste for subsequent reflow soldering of SMD's.

2nd PLANE: The second plane includes the second metallization layer and the associated resistor pastes and pads similar to the ones described for the first plane.

3rd PLANE: The third plane includes only the dielectric, and

4th PLANE: The fourth plane includes the overglazing only.

Furthermore, contacts have been defined between the two metallization planes. The pads of each metallization layer correspond to holes in the overglazing plane, and for that purpose they are defined as contacts between their home plane and the O-plane.

It is worth noting that the metallization planes are the most complex constructions. A metallization plane consists basically of the conductor pattern and the four resistor types of that plane. When a resistor paste overlaps a metallization line a new tile-type (a contact) is automatically generated according to the definitions introduced in the compose section. That action simplifies the work of the design rule checker in the area of metal-resistor overlaps, and it also facilitates the writing of reliable design rule checking sections. The other feature of the plane in question is the pad. As it has already been mentioned two main categories of pads have been provided. A wide range of pads of both categories have been included in the pad library, which has been added to the Magic files.

Another feature of the technology file developed is the possibility of contact with the second metallization plane. In order to keep the design as clean as possible the only tile types of the two metallization layers that are allowed to overlap are the two metallization lines. At the crossovers, where vias are not formed, a patch of dielectric is automatically generated in the CIF output file created by Magic, as shown at the bottom part of Fig. 1. The cif output section's part that generates the dielectric mask is the following:

```
layer DI m1
and m2
grow 300
or di
```

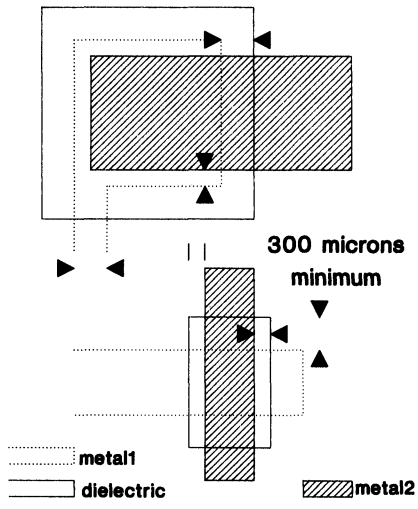

FIGURE 1 Design rules for capacitors and isolated metal crossings.

This enables the free use of the built-in automatic router, something which was not possible in a previous implementation[4].

Moreover, specific thick film process rules and parameters[5,6] have been inserted in the drc and extract sections.

It must be noted that special care has been taken in the selection of the colours for each tile type in such a way that what is seen on the graphics screen is always comprehensible.

It is apparent from the previous description that wirebonding sites, die pads, pads for SMDs, and resistor terminations may be placed by the designer either at

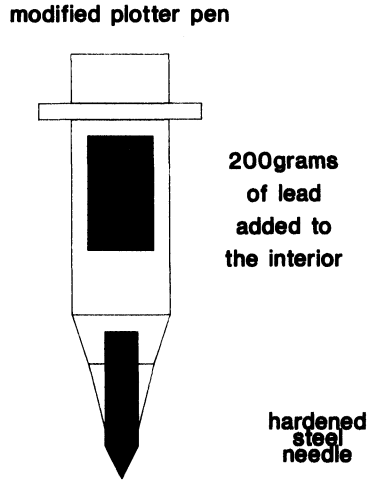

FIGURE 2 The schematic of the home made cutting tool.

the 1st conductor's or the 2nd conductor's plane. This gives a great flexibility to the designer: for example it allows the designer to use an inexpensive conductor such as palladium-silver on the lower level, where good wirebonding characteristics are not required; the upper level of metal may be screened with a gold paste, which is known to have excellent wirebonding characteristics and it may allow for eutectic die attachment.

Copies of our designs may be obtained on a X-Y plotter using Vic[7], SOLO 1400[8] or any other software packet that takes as an input a .CIF file and allows for the driving of a X-Y plotter. The same programs have been used to create the actual masks on rubylith, by replacing one of the pens with a home-made cutting tool, as only one layer at a time may be drawn on the X-Y plotter. A schematic picture of the cutting tool is shown in Fig. 2.

3. DESIGN RULES

Minimum widths are 300μm for metal lines, 1300μm for resistors, 500μm for die pads, wirebond sites, solder prints (to relow solder SMDs) and I/O pads, 1000μm for SMD-pads. Minimum spacings are 300μm between conductor and resistor patterns.

Also, minimum overlaps of 300μm have been implemented for printed resistors and SMDs to allow for misalignment, as shown in Fig. 3.

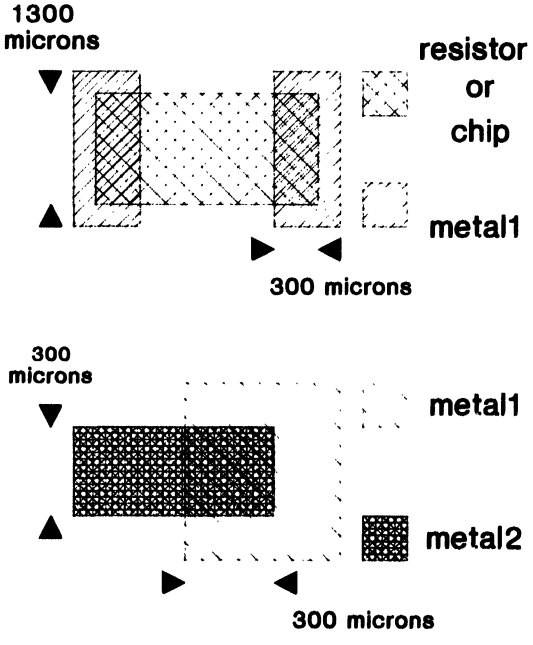

FIGURE 3 Overlap and extension design rules for discrete components, screen printed resistors, and metal lines.

4. THE EXTRACTOR

Magic's extractor computes from the layout the information needed to run simulation tools such as Crystal. This information includes the connectivity, and the resistance and if required the parasitic capacitance of nodes.

Node resistances comprised entirely of a single type of material are calculated, in the case of simple rectangles, together with the perimeter and area of the resistor. The resistance, however, is always taken in the longer dimension of the rectangle. In the case of more complicated layouts, i.e. top hats, etc, the program computes the node's total perimeter and area and subsequently approximates the value of the resistor with that of a rectangle that has the same perimeter and area.

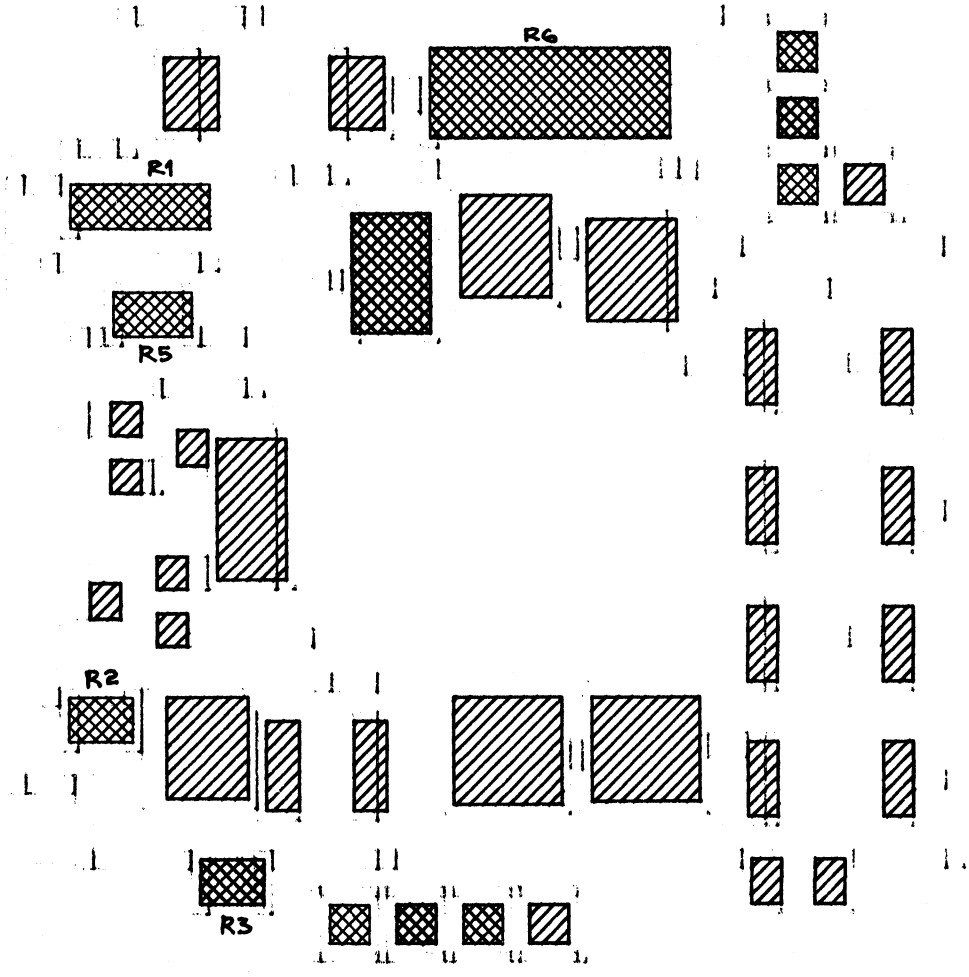

FIGURE 4 Actual pen plot of the electret-type microphone layout.

Three types of internodal capacitance are extracted:

a] Overlap capacitance between two different types of conducting materials, separated by a dielectric, when they overlap,

b] Sidewall capacitance between the vertical edges of two pieces of the same type of conducting material, and

c] Sidewall overlap capacitance between the vertical edge of one type of conducting material and the horizontal surface of a second type of conducting material that overlaps the first.

The extracted values of parasitics of a thick film circuit which has been laid out with the Magic editor is considered to be valuable to the designer since it allows for a quick verification of the values of the resistors and capacitors designed. It also permits a good estimate of the minimum area of the ceramic substrate required for the implementation of the circuit.

5. AN EXAMPLE

As a demonstration an electret-type microphone circuit was designed and constructed using a palladium silver paste, four different resistor pastes, and SMDs for the capacitors and the diodes, using the hybrid design system developed. Fig. 4 shows the actual pen plot layout showing, in a 5:1 scale, the metal, the resistors and the solder pads. Since hierarchical designs are supported, the pad frames of the SMDs together with the solder paste pads, and also the alignment pattern containing substrate and layer-to-layer alignment marks can be saved in a library as separate objects to be called when needed. The remaining of the layout of the circuit was constructed by hand using the painting and wiring features of Magic. Since this design was done with conservative design rules, a quick 5X ruby-cutting was performed using our home-made cutting tool on a HP-7475A X-Y plotter with little loss of accuracy. It is worth noting that the speed of the tool should be defined as 1cm/sec in order to ensure a good, deep cutting.

The extractor has been used in order to confirm the validity of the values of the resistors designed during the layout procedure. The results are given in Table 1.

Three different resistor pastes have been used: 10Ω/sq., 1KΩ/sq., and 100KΩ/sq., for the fabrication of six different resistors.

TABLE 1
Extraction results of the circuit in Fig. 4.

node	Value (Ohms)	Area (Magic Units)	Perimeter (Magic Units)
R4	200,000	800	120
R3	100,000	225	60
R6	25	2220	208
R1	2,667	600	110
R2	1,000	225	60
R5	1,333	300	70

6. CONCLUSIONS

It has been shown that technology files for the Magic layout editor together with the use of other modified programs may facilitate the layout, design rule checking, extraction of circuit parameters, and plotting or rubylith cutting of one and two metal multi-layered hybrid circuits.

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APPENDIX I: The Technology File

```
tech
    scmos
end

planes
    metal1,m1
    metal2,m2
    dielectric,di
    overglazing,o
end
types
   m1          metal1,m1
   m2          metal2,m2
   m1          resistor1,r1
   m1          resistor2,r2
   m1          resistor3,r3
```

APPENDIX I (*Continued*)

```
    m1          resistor4,r4
    di          dielectric,di
    m1          contact1,c1
    m1          contact2,c2
    m1          contact3,c3
    m1          contact4,c4
    m1          via,m2c,v
    m2          resistor5,r5
    m2          resistor6,r6
    m2          resistor7,r7
    m2          resistor8,r8
    m2          contact5,c5
    m2          contact6,c6
    m2          contact7,c7
    m2          contact8,c8
    m1          pad1,p1
    m2          pad2,p2
    m1          devicecontact1,dc1
    m2          devicecontact2,dc2
    o           overglazing
end

contact
    via     m1      m2
    dc1     m1      o
    dc2     m2      o
    p1      m1      o
    p2      m2      o
end

styles
    styletype mos
    di              1
    r1              2
    r2              3
    r3              4
    r4              5
    r5              2
    r5              9
    r6              3
    r6              9
    r7              4
    r7              7
    r8              5
    r8              7
    m1             20
```

APPENDIX I (*Continued*)

m2	21
c1	2
c1	20
c1	32
c2	3
c2	20
c2	32
c3	4
c3	20
c3	32
c4	5
c4	20
c4	32
c5	2
c5	9
c5	21
c5	32
c6	3
c6	9
c6	21
c6	32
c7	4
c7	7
c7	21
c7	32
c8	5
c8	7
c8	21
c8	32
via	20
via	21
via	33
dc1	20
dc1	12
dc1	34
dc2	21
dc2	12
dc2	34
p1	20
p1	13
p1	33
p1	34
p2	21
p2	13

APPENDIX I (*Continued*)

```
    p2          33
    p2          34
    o           34
    error_p     42
    error_s     42
    error_ps    42
end

compose
      compose   c1  r1  m1
      compose   c2  r2  m1
      compose   c3  r3  m1
      compose   c4  r4  m1
      compose   c5  r5  m2
      compose   c6  r6  m2
      compose   c7  r7  m2
      compose   c8  r8  m2
end

connect
     m1,c1,c2,c3,c4,p1,dc1,via/m1,m1,c1,c2,c3,c4,p1,dc1,via/m1
     c1 m1,r1
     c2 m1,r2
     c3 m1,r3
     c4 m1,r4
     c5 m2,r5
     c6 m2,r6
     c7 m2,r7
     c8 m2,r8
     m2,c5,c6,c7,c8,p2,dc2,via/m2,m2,c5,c6,c7,c8,p2,dc2,via/m2
end

cifoutput
style a
  scalefactor 100
    layer CMF m1
    or c1,c2,c3,c4,via/m1,p1/m1,dc1/m1
    layer CVA   r1,c1
    layer CCA   r2,c2
    layer CCP   r3,c3
    layer CSN   r4,c4
    layer CSP   r5,c5
    layer COG   r6,c6
    layer XP    r7,c7
    layer XP    r8,c8
    layer CMS m2,c5,c6,c7,c8,via/m2,p2/m2,dc2/m2
```

APPENDIX I (*Continued*)

```
    layer CPG m1,r1,r2,r3,r4,c1,c2,c3,c4
    and m2,r5,r6,r7,r8,c5,c6,c7,c8
    grow 300
    or di
    and-not via
    layer CAA o
    and-not p1
    and-not p2
    and-not dc1
    and-not dc2
    layer CWN dc1
    or dc2
    layer CWP p1
    or p2
end

cifinput
style a
  scalefactor 100
    layer m1 FML
      labels FML
    layer r1 R1
      labels R1
    layer r2 R2
      labels R2
    layer r3 R3
      labels R3
    layer r4 R4
      labels R4
    layer r5 R5
      labels R5
    layer r6 R6
      labels R6
    layer r7 R7
      labels R7
    layer r8 R8
      labels R8
    layer o OV
      labels OV
    layer p1 FML
    and-not OV
    and PD
    layer p2 SML
    and-not OV
    and PD
```

APPENDIX I (*Continued*)

```
    layer dc1 FML
    and-not OV
    and DV
    layer dc2 SML
    and-not OV
    and DV
end

drc
    edge4way via/m1 ~ (via,space)/m1 1 ~ (m2)/m2 ~ (via)/m1 1 \
      "No dielectric near via" m2
    width m1 3 \
      "Minimum conductor width must be 300"
    width m2 3 \
      "Minimum conductor width must be 300"
    width r1,r2,r3,r4 13 \
      "Minimum resistor width must be 1300"
    width r5,r6,r7,r8 13 \
      "Minimum resistor width must be 1300"
    width c1,c2,c3,c4 3 \
      "Minimum resistor-conductor overlap must be 300"
    width c5,c6,c7,c8 3 \
      "Minimum resistor-conductor overlap must be 300"
spacing m1,via/m1,c1,c2,c3,c4,p1/m1,dc1/m1
m1,via/m1,c1,c2,c3,c4,p1/m1,dc1/m1 3 touching_ok \ "Minimum spacing must
be 300" spacing m2,via/m2,c5,c6,c7,c8,p2/m2,dc2/m2 m2,via/m2,c5,c6,c7,c8,p2/
m2,dc2/m2 3 touching_ok \ "Minimum spacing must be 300" spacing r1 c1,r1,3
touching_ok "Minimum spacing must be 300" spacing r2 c2,r2 3 touching_ok
"Minimum spacing must be 300" spacing r3 c3,r3 3 touching_ok "Minimum
spacing must be 300" spacing r4 c4,r4 3 touching_ok"Minimum spacing must be
300" spacing r5 c5,r5 3 touching_ok "Minimum spacing must be 300" spacing r6
c6,r6 3 touching_ok "Minimum spacing must be 300" spacing r7 c7,r7, 3
touching_ok "Minimum spacing must be 300" spacing r8 c8,r8 3 touching_ok
"Minimum spacing must be 300" edge4way r1 space 3 r1,c1,space space 3
"Minimum spacing must be 300" edge4way r2 space 3 r2,c2,space space 3
"Minimum spacing must be 300" edge4way r3 space 3 r3,c3,space space 3
"Minimum spacing must be 300" edge4way r4 space 3 r4,c4,space space 3
"Minimum spacing must be 300" edge4way r5 space 3 r5,c5,space space 3
"Minimum spacing must be 300" edge4way r6 space 3 r6,c6,space space 3
"Minimum spacing must be 300" edge4way r7 space 3 r7,c7,space space 3
"Minimum spacing must be 300" edge4way r8 space 3 r8,c8,space space 3
"Minimum spacing must be 300" edge4way c1,c2,c3,c4 space 3 m1 space 3
"Minimum overlap must be 300" edge4way c5,c6,c7,c8 space 3 m2 space 3
"Minimum overlap must be 300" edge4way
```

APPENDIX I (*Continued*)

```
m2,c5,c6,c7,c8,r5,r6,r7,r8,dc2/m2,p2/m2,via/m2 space 3 ~ (dc1/m1,p1/m1)/m1
space 3 \ "Metal2 layer types may not overlap metal1 pads" m1 edge4way p1/
m1,dc1/m1 ~ (p1/m1,dc1/m1)/m1 3 ~ (m2,c5,c6,c7,c8,r5,r6,r7,r8,dc2/m2,p2/
m2,via/m2)/m2 ~ (p1/m1,dc1/m1)/m1 3 \ "Metal2 layer types may not overlap
metal1 pads" m2 width p1 5 "Minimum width 500" width p2 5 "Minimum width
500" width dc1 10 "Minimum width 1000" width dc2 10 "Minimum width 1000"
end

extract
  style a
  lambda 100
  step 100

    resist m1 0
    resist r1 0
    resist c1 0
end

wiring
   contact via 4 m1 0 m2 0
end

router
    layer1     m1     3m 1,via/m1,r1,c1,r2,c2,r3,c3,r4,c4 1
    layer2     m2     3 m2,via/m2 1
    contacts   via    3
    gridspacing 3
end
plowing
end
plot
end
```