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INFLUENCE OF INTRINSIC TRAPPING ON THE PERFORMANCE CHARACTERISTICS OF ZnO-Bi_2O_3 BASED VARISTORS

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The lumped parameter/complex plane analysis technique reveals several contributions to the ac small-signal terminal immittance of the ZnO-Bi_2O_3 based varistors' grain-boundary response. The terminal capacitance constitutes multiple trapping phenomena, a barrier layer contribution, and a resonance effect in the frequency range $10^{-2} \leq f \leq 10^{9}$ Hz. A trapping response near to $\sim 10^{5}$ Hz ($\sim 10^{-6}$ s), observed via the loss-peak and a distinct depressed semicircular relaxation in the complex capacitance plane, is common to all well-formed (exhibiting good performance for applications) devices regardless of the composition recipe and processing route. This trapping is attributed to possible formation of ionized intrinsic or native defects, and believed to be predominant within the electric field falling regions across the microstructural grain-boundary electrical barriers. The nature of rapidity of this intrinsic trapping and the corresponding degree of uniformity/non-uniformity can be utilized in conjunction with relevant information on other competing trapping phenomena to assess an overall performance of these devices. The constituting elements, responsible for the average relaxation time of the intrinsic trapping, indicate some sort of possible surge arrester (i.e., suppressor/absorber) applications criteria in the power systems' protection. The factors related to materials' history, composition recipe, and processing variables influence or modify relative magnitudes and increase or decrease the visibility of the constituting elements without distorting devices' generic dielectric behavior.

INTRODUCTION

The ZnO-Bi_2O_3 based highly nonlinear devices are commonly known as metal oxide varistors[1–3] (MOVs). An arrester assembly used as the surge suppressor/absorber is based upon these MOV blocks. These blocks are arranged in a stack or in several electrically series-connected stacks in the valve section between the top and bottom terminals,[4] inside an insulating (ceramic porcelain or polymer rubber) housing. The surge arresters are used extensively to protect electrical equipment and increase voltage stability.[3,4] Also, reliability of electrical power distribution is achieved via transient protection against lightning, switching pulse, temporary overvoltage (TOV), etc. The MOVs are primarily composed of ZnO with small additives of Bi_2O_3 and other oxide constituents.[1–4] These additives control each electrically active grain-boundary (GB) electrical barrier, physically existing within the electrical length (i.e., electrical field falling region), resulting from the charge trapping processes.[3,5–11] In general, the high resistivity exhibited by these MOVs at low electric stress levels is derived from these grain boundaries, which are strongly insulating

with respect to the *n*-type ZnO grains they surround. An overall electrical performance (including protective characteristics) of the device represents lumped behavior of the microstructural operative paths between the electrode terminals. A lumped single electrical barrier is the effective representation of the microstructural network consisting of the "*m*" junctions in parallel with "*n*" junctions in series[5,7] across the sample (i.e., between the electrodes).

Essentially, the performance characteristics of a MOV are controlled by the presence and nature of the defect states, and interactions with the carriers via trapping-detrapping within the GB electrical barriers.[5,6,9] As a result, several simultaneously competing trapping phenomena play a combined role in the MOV's function for their time-dependent applications as a power protective device (i.e., surge arrester). Out of several trapping contributions identified in these devices, a common trapping response described as the intrinsic behavior has extensively been reported in the literature.[3,5,6,10] In general, this trapping is observed in the vicinity of $\sim 10^5$ Hz (corresponding relaxation time ≈ 1 μs) and, thus, often characterized as the common loss-peak[3] and identified as the intrinsic relaxation[10,11] to all devices without ascertaining applications criteria. The intrinsic trapping relaxation can be identified in the Bode-like loss-frequency[3] and complex capacitance[5,6] (C*) planes via a semicircular relaxation of the ac small-signal immittance (impedance or admittance) data. The presence of a finite depression angle in this semicircular relaxation is associated with the loss-component[5,6] (i.e., conductance). These parameters are systematically documented[5,6,10] via utilizing the lumped parameter/complex plane analysis (LP/CPA) technique for these immittance data. A strong perspective of this depression angle represents an average or a lumped distributed process of the carrier trapping-detrapping across the GB barrier region.

Levinson and Philipp[3] (LP) identified this response as a common behavior in the multi-component varistors regardless of the composition recipe. They recognized this behavior as some sort of polarization processes relating to specific cations added to zinc oxide. This presumption did not provide further insight on the actual representation of the traps, and thus, remained unknown. The composition recipe essentially emphasized the devices' potential varistor characteristics. In practice, the well-formed (exhibiting or possessing good performance for applications) varistors were fabricated from the multi-component recipe. They recognized this behavior as some sort of polarization processes relating to specific cations added to zinc oxide. This presumption did not provide further insight on the actual representation of the traps and remained unknown. Cordaro et al.[11] characterized the same behavior for a variety of simple (i.e., not a complex multi-component or easily defined recipe with the additive(s) introduced in sequence) varistor-like materials, and identified as a trapping contribution to the device. This effort presumably considered one-to-one correspondence for each occurrence of the defects via systematic introduction of cations to ZnO, and allowed a simplified approach to the solution of the complex nature of trapping when extended to the multi-component systems. These simple varistor-like materials did not provide a firm clue to the mechanism(s) responsible for the intrinsic relaxation when extended to the identical behavior of the devices with multi-component configuration. A meaningful prediction of the possible mechanism(s) remained as a key feature of these investigations, and could not be utilized as a guideline to satisfy the applications

criteria of the multi-component devices. Further, a systematic trend in the intrinsic trapping of these simple varistor-like materials was difficult to utilize as the uncertainty persists in the performance parameters (i.e., energy-handling, surge withstanding capability, bias-stability, etc.). In general, the simple varistor-like materials did not meet the required characteristics of the well-formed varistors. Cordaro et al. utilized spectroscopic analytical approach for the immittance data as a function of frequency (f) at non-equilibrium experimental conditions these varistor-like materials.

The common trapping response was designated as the "τ_3 relaxation" process in several recent papers by Alim et al.[5,6,9,10] This nomenclature resulted from the order of the relaxation in the frequency domain for the immittance data when analyzed in the C*-plane. The τ_3 relaxation is formed from the series contributions of the in-phase resistive element R_3 and out-of-phase capacitive element C_3. The influence of the τ_3 relaxation[5,6,9,10] on the other combined trapping (such as: τ_4, τ_2, and/or τ_1 described in references 5 and 6) phenomena and their interrelationships on the resulting performance characteristics are important. The limits of R_3 and C_3 are found to restrict the window for other trapping phenomena through an interrelationship among themselves, as each relaxation constitutes parallel operative path[6] in the frequency domain. Thus, τ_3, R_3, and C_3 satisfy the fundamental requirements of the varistor action satisfying impulse tolerance, energy-handling, and bias-stability.

The LP/CPA technique revealed identical information when verified through a cross examination procedure employing the approaches (i.e., spectroscopic and Bode-like plots) described and used by LP[3] and Cordaro et al.[11] The advantage of the LP/CPA technique is recognized by the versatility of separating multiple competing phenomena operative between the electrode terminals[5,6,10] when each of these are clearly identified. Also, this technique resolves each of the relaxation processes into the contributing elements, and eventually produces a plausible equivalent circuit. Desired device properties are achieved via controlling these configurative equivalent circuit elements as a function of composition recipe and processing variables for the application purposes.

The purpose of this paper is to define a meaningful range for the τ_3 relaxation of a well-formed device such that the elements R_3 and C_3 ascertain their maximum and minimum values for the application purposes. This range is expected to predict better effect of a device within the configurational range than the other device, though several devices may satisfy applications criteria concurrently. A description on the role of achieving a desired value of τ_3 via the constituting elements R_3 and C_3 is provided in a generic form attributing to the composition recipe and processing route. Further, the role of the finite non-Debye depression angle (θ_3) for the τ_3 semicircular relaxation in the C*-plane are also considered in conjunction with the presence of the non-0° depression angle, θ_{im}, obtained in the impedance (Z*) plane via a single semicircular relaxation.

TRAPPING EFFECT AND PERFORMANCE OF THE DEVICE

An overall electrical performance of the ZnO-Bi_2O_3 based varistors is attributed to the total nature of competing trapping phenomena[5,6,9,10] within the electrical

barrier regions. It is possible to distinguish each trap with respect to the net behavior of these devices. When each of these traps are carefully examined in a sequential manner, an empirical interrelationship may be achieved.

A thorough evaluation of the τ_3 relaxation reveals that the associated trapping process is systematically related to the device's resulting performance. Several relevant parameters often exhibit a close relationship with the τ_3 relaxation. These are: ohmic leakage current, capacitive current, frequency of high-current short-duration impulse tolerance, energy-handling capability at discharge voltages (i.e., long-time low-current test), thermal behavior (i.e., diffusivity, conductivity, generation, dissipation, specific heat, etc.), accelerated aging and/or transient bias-stability with watts-loss at near room, and elevated temperatures (usually $115 \leqslant \mathbf{T} \leqslant 140°C$) when stressed at MCOV (maximum continuous operating voltage). No direct evidence of correlation between the formation mechanism or origin of τ_3 (i.e., in terms of the constituting elements R_3, C_3, and variation in the loss-peak[3]) and its relation to these performance characteristics is ascertained. However, a passive (or indirect) role in sustaining or degrading the GB electrical barriers also cannot be ruled out.[12,13]

A change in the resulting behavior of τ_3, monitored via electrical testing before and after at necessary experimental conditions, is attributed to the barrier deformation.[12] This response is described as the altered trapping states[13] within the GB barrier regions. These effects are often regarded as the degradation in these devices, and essentially τ_3 is, thus, perturbed.[13] Nevertheless, the relaxation response of τ_3 can be modified via its absolute value and the magnitude of the constituting elements satisfying application requirements. The non-Debye (non-ideal) response of the τ_3 relaxation cannot be averted in conjunction with τ_3's modification, as it is always evidenced via the presence of the depressed semicircle in the C*-plane.[5,6,10] The range of τ_3 and its constituents follow an empirical relationship with other trapping contributions in order to distinguish the performance of the device.

IMMITTANCE-FREQUENCY DISPERSION

Immittance spectroscopy is a viable tool/technique to determine the nature of the microstructural electrical path(s) between the electrodes. This technique provides a basis for understanding the character of a multicomponent/phase heterogeneous device system (such as a MOV), resolving extraneous contributions to the terminal immittance operative within it.[5,6,9,10,14] These contributions are unraveled in the frequency domain. A wide dispersion in the terminal immittance with the frequency encompasses large capacitance, often regardless of the contributing elements to it, for the same range of measurement frequency. Essentially, the resulting performance of these MOVs depend on the nature of this dispersion. An effective judgement on the prediction of an overall performance is possible from this dispersion. Thus, a demarcation between a good performance and a poor response in these devices becomes evident. This demarcation is based upon the acquisition of the ac small-signal immittance data, and subsequent utilization of the LP/CPA technique.[5,6,9,10]

The two-terminal immittance data of the MOVs, acquired over a frequency range $10^{-2} \leqslant f \leqslant 10^9$ Hz, reveal multiple relaxations[5,6,9,10] and a resonance phenomenon[3,5,6,9,14] in the complex capacitance ($C^* = C' - jC'' = C_p - j(G_p/\omega)$; where $C' = C_p$ = terminal parallel capacitance, $C'' = G_p/\omega$, G_p = terminal parallel conductance, $\omega = 2\pi f$, and $j = \sqrt{-1}$) plane. A generic representation of these immittance data at near room-temperature is provided in Figure 1. In this plot, three distinct relaxations [denoted as τ_2 ($=R_2C_2$), τ_3 ($=R_3C_3$), and τ_4 ($=R_4C_4$)], a low-frequency distortion (C_1 or corresponding polarization related τ_1 relaxation with a dc limit), and a barrier layer capacitance ($C_{BL} = C_5 + C_6$) including the dielectric contribution of the lumped grains ($C_6 = C_{ZnO}$) are evident. These six delineated capacitive elements, designated as C_1 through C_6, represent static (i.e., under dc condition) capacitance[5,6] when lumped together. The nomenclature of each capacitive element is cited in references 5 and 6. The relative contribution of each element can reveal experimental dependence under a given set of conditions.

The capacitances C_5 and C_6 (or combined C_{BL}), in general, are nearly identical for all devices (unless otherwise the purpose of application is drastically different), and their lumped behavior is geometric. This concept is prevalent because of nearly uniform spatial carrier density in the ZnO grains and defect states ensuing identical electrical thickness (i.e., electric field falling depletion region) across the GB. Thus, the geometric nature of C_{bL} causes either no or less impact on the extraction of the static (i.e., at $f \rightarrow 0$ Hz) capacitance (i.e., $C_{dc} = \Sigma_{i=1}^{6} C_i$) using ac small-signal electrical data.

The uniformity in the spatial carrier density in the ZnO grains is evidenced by the frequency-independent Mott-Schottky (i.e., $1/C_{BL}^2$ versus applied dc voltage V_{dc}) straight line and successfully demonstrated in reference 6. The net defect states

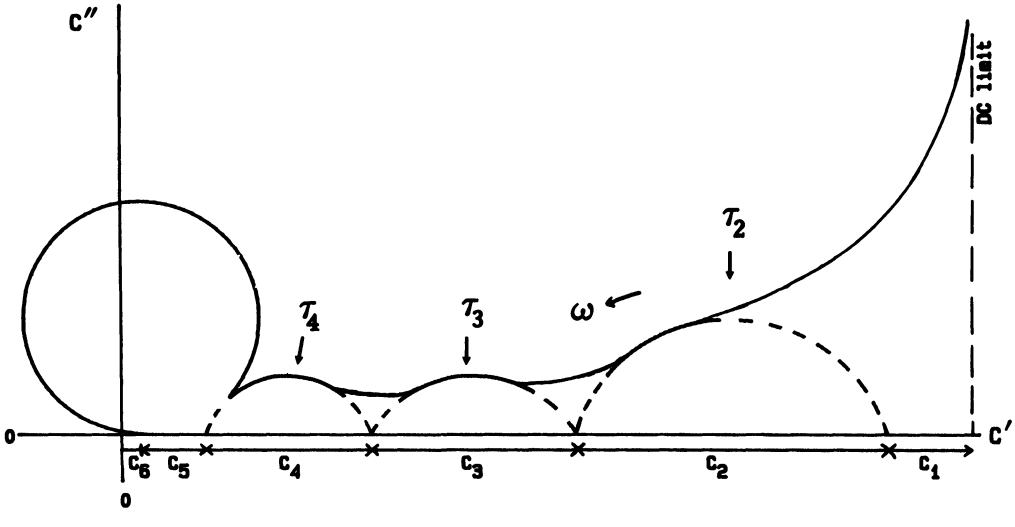

FIGURE 1 Generic complex capacitance ($C^* = C' - jC''$) plot of ZnO-Bi_2O_3 based varistor at near room temperature in the approximate frequency range $10^{-2} \leqslant f \leqslant 10^9$ Hz.

within the electrical thickness are likely to be primarily dependent on the grain-size and phase distribution in the microstructure. The origin of these defects are widely speculated[3,11] but often seem to stand alone lacking firm support. In a multi-component/phase heterogeneous device, the nature of these defects is likely to be more complex than relating them to the singular defect status of the additive species. Nevertheless, the clustered defects within the electrical thickness presumably controls $C_1 + C_2 + C_3 + C_4$ (or $\Sigma_{i=1}^{4} C_i$). Thus, the capacitances C_1 through C_4, attributed to trapping,[5,6] essentially dominate the overall static dielectric behavior of the devices. In general, the aforementioned distinguishable behavior in the frequency domain is a characteristic of the well-formed varistor composites, regardless of manufacturer's materials' history and processing methods. These factors influence relative magnitudes, and increase or decrease the visibility of all the constituting parameters (i.e., R_i and C_i for each τ_i) without eliminating or distorting generic response of this dielectric composite. Typically for good varistors, τ_3 ranges between 1 and 2 μs. These boundary values, depending on the devices, imply that R_3 can range between 10 and 80 kΩ, and corresponding C_3 can range between 12.5 and 100 pF for the 1 μs relaxation. In an identical manner R_3, can range between 10 and 160 kΩ and the corresponding C_3 can range between 12.5 and 200 pF for the 2 μs relaxation. The entire choice of the τ_3 relaxation is depicted in Figure 2. Reasonably good varistor properties can be obtained when τ_3 lies near to the intermediate region (often lower-side of the intermediate region) of these two extreme boundary values in conjunction with the constituting parameters of τ_1, τ_2,

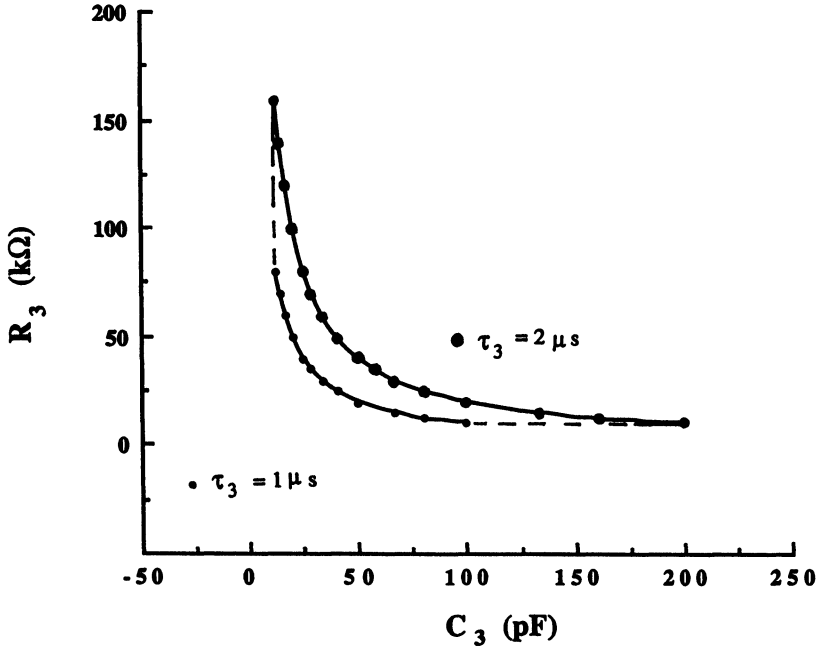

FIGURE 2 Choice of common trapping relaxation (τ_3) via the contribution of the constituting elements (R_3 and C_3) between 1 μs and 2 μs possessing minimum and maximum values.

and τ_4. It is preferred that R_3 be *large* such that an overall relationship between τ_3 and combined effect of τ_2 and/or τ_1 influences the resulting performance of the device.

At high frequencies (usually $10^6 \leq f \leq 10^9$ Hz), a resonance phenomenon emerges as a circle in the C*-plane possessing negative values of the terminal parallel capacitance. This resonance behavior is complex[3,5,6,14] and attributed to the combined external electrode-lead configuration, built-in contact inductance of the sample holder, and possible piezoelectric grain resonance phenomenon. The variation in lead length and sample thickness with a fixed electrode area influences the onset of this behavior with respect to the measurement frequency. Three types of resonance events and their detailed description are documented in a recent paper.[14] These events depend on the nature of the overall lumped GB response in conjunction with the electrode configuration while approaching high frequencies. Only one type of resonance event,[5,6,10] identical to Figure 1, allows a distinct τ_4 relaxation yielding C_5 and C_6. The other two resonance events exhibit a distinct τ_3 relaxation with the masking of τ_4 relaxation.[14]

The left intercept on the abcissa (i.e., C′, Figure 1) for the τ_3 semicircular relaxation may be defined as C_x ($= C_4 + C_5 + C_6$), which is enhanced in a nearly linear fashion with increasing sintering temperature.[10] This lumped capacitance (C_x) is not a device parameter but produces a deceptive Mott-Schottky (MS) straight line. This MS straight line, although appearing like a frequency-independent plot, does not provide device-related parameters such as grain carrier density, built-in potential, barrier height. However, the parameter C_x can be used in lieu of C_{BL} in many suitable cases when the devices do not exhibit straightforward resonance.[5,6,14] Three simultaneous issues are of importance when the behavior of C_x yields a nearly straight line as a function of sintering temperature. These issues are related to the non-sensitive (i.e., too small effect) behavior of C_4 at an applied dc biasing for a specified sintering temperature of the device, and are summarized below:

1. net electrical thickness or depletion region across the sample (i.e., between the electrodes) is reduced due to the grain-size enhancement with increasing sintering temperature,
2. grain carrier density is affected in the increasing order by the increasing sintering temperature, and
3. combined contribution of the above two issues producing geometric changes in C_x yielding a deceptive MS behavior.

CHARACTER OF THE INTRINSIC TRAPPING RELAXATION

The immittance-frequency response and a complete characterization of the intrinsic trapping using the LP/CPA technique is reported in references 5 and 6. The influence of sintering conditions on the intrinsic trapping is summarized in reference 10. Figure 1 illustrates a nearly ideal dispersion of the ac immittance data with frequency in the range $10^{-2} \leq f \leq 10^9$ Hz. The parameter G_p includes the dc conductance as well as the loss associated with each relaxation observed in the C*-

plane. The curve in the low frequency range (usually $f \leq 5$ Hz) asymptotically approaches infinity in this plane. The dc limit signifies the values of maximum parallel capacitance (i.e., $C_p = \Sigma_{i=1}^{6} C_i$) and corresponding leakage conductance (G_p) of the device.[5,6]

Figure 3 depicts the effect of sintering temperature and soak time on τ_3 and θ_3. The effect of sintering temperature on θ_3 is found to be sensitive for a composition recipe and a specific processing route. In general, θ_3 decreases at above a certain temperature (for example: 1100°C) and remains nearly constant at above a specific soak time. The capacitance C_3 exhibits a flat (i.e., nearly constant) response at a range of sintering temperature (for example: between 1100 and 1300°C) for a fixed soak time. This situation indicates a homogeneous and non-varying charge storage via a out-of-phase capacitance in this range of sintering temperature.[10] The capacitance, thus produced, constitutes the relaxation time response when the in-phase loss component (R_3) is incorporated into it. The optimum level of the non-varying charge storage, associated with the native defects, may be achieved via a range of sintering temperatures providing a direct dependence of τ_3 on R_3. A minimum soak time, corresponding to a sintering temperature, is needed to ensure a higher degree of homogeneity in the distribution of the τ_3 traps. The dependence of θ_3 and τ_3 on soak time is very similar to that observed for the Zn content of the Bi_2O_3-rich regions by Olsson.[16] The reduction in Zn content of the Bi_2O_3 phase in conjunction with the existing intrinsic defects in the ZnO grain most probably creates fast responsive trapping centers near the active interfaces within the device. These results suggest that the intrinsic defects in the ZnO grain and their degree of spatial homogeneity remain nearly constant above a certain minimum soak time.

The parameters extracted from the representation of the ac small-signal electrical data using the LP/CPA technique are significantly influenced by the sintering temperature. This implies that the intrinsic defects are perturbed to a new equilibrium concentration for every sintering temperature at a specific soak time. However, a desired property can be ascribed to a MOV composition for a range in sintering temperature in conjunction with a variation in soak time. The alterations in the intrinsic defects might have occurred because of the changes in the chemistry with sintering as may be noted for a variation in certain additive species to the ZnO. A net interaction among the additives plays an important role for the intrinsic trapping parameters. As an example, the increase in Mn and Ni defect concentrations in the bulk ZnO grain with increasing sintering temperature might increase the concentration of ionized Zn interstitials and, thus, result in minor enhancement in carrier density at room temperature.[10] This logic can be supported by the slight increase in the leakage current.

Each semicircular relaxation in the C*-plane may be described by the non-Debye Cole-Cole[17] empirical relation:

$$C^* = C_{\text{left intercept/high frequency}} + \frac{C_i}{1 + (j\omega_i\tau_i)^{(1-h_i)}}$$

where h_i ($= 2\theta_i/\pi$ possessing a limit in the range $0 \leq h_i \leq 1$) is the depression angle parameter of the ith relaxation (precisely $i = 2, 3, 4$). The ultimate low-

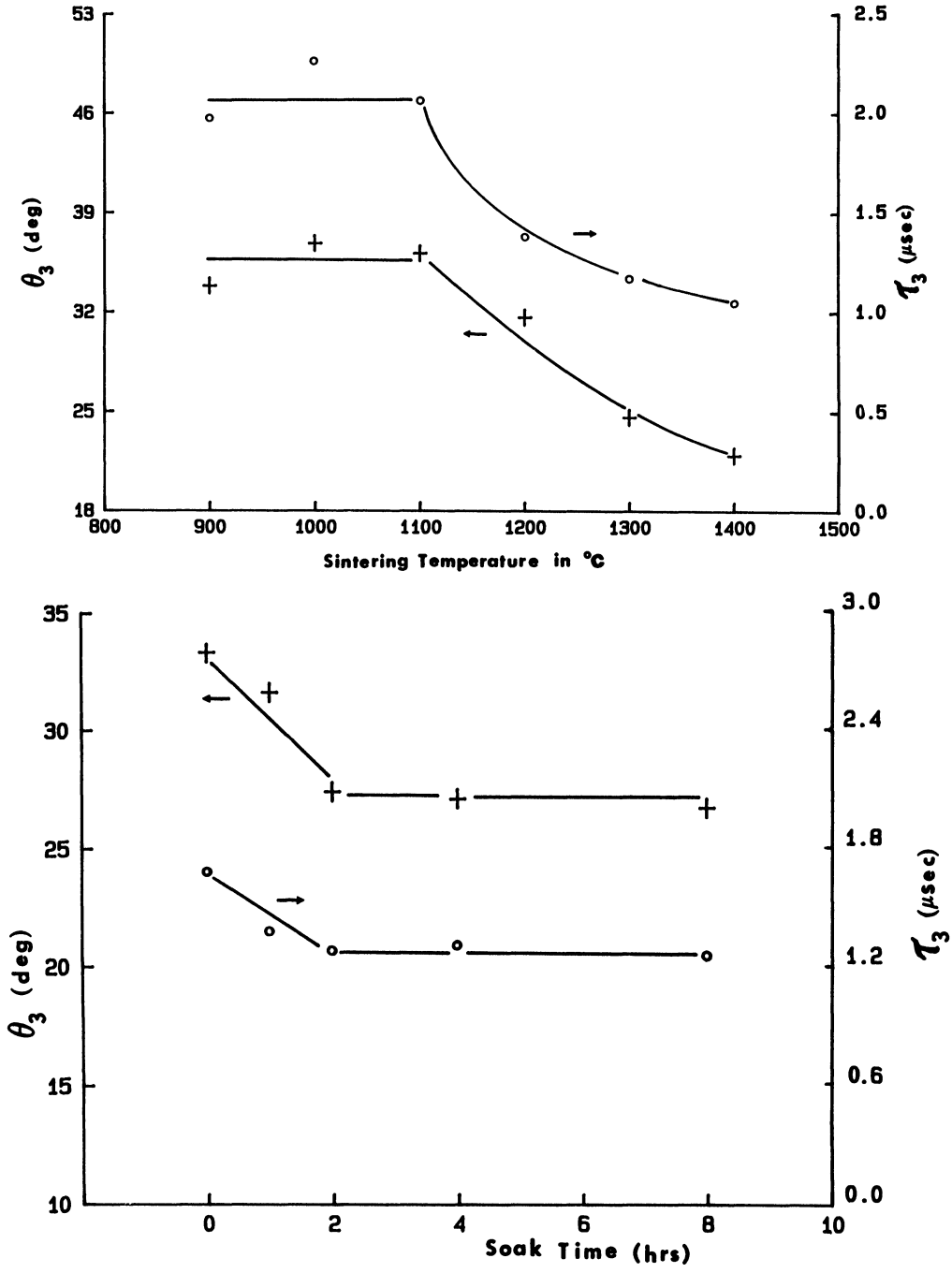

FIGURE 3 (A) Effect of sintering temperature at a constant soak time on the depression angle (θ_3) and relaxation time (τ_3) of the common trapping response (measured at room temperature). (B) Effect of soak time at a constant sintering temperature on the depression angle (θ_3) and relaxation time (τ_3) of the common trapping response (measured at room temperature).

frequency relaxation for $i = 1$ cannot be resolved in the C*-plane as it is always distorted for all devices. The first term on the right-hand side in this equation is expressed by the left intercept of each relaxation. The second term is associated with the ith relaxation. Therefore, the parameter C_i denotes chord length, and τ_i specifies average relaxation time [where the peak of the semicircular relaxation provides $(\omega_i\tau_i)_{peak} = \omega R_iC_i = 1$]. This condition resolves equivalent circuit relationships constituting C_i and R_i corresponding to the ith relaxation-related capacitance and resistance, respectively. Thus, each relaxation can be represented as an individual lumped equivalent R-C series combination.[6,15] for each parallel branch. The presence of a depression angle (θ_i) in the semicircular relaxation indicates nonideal trapping wherein a considerable degree of nonuniformity is associated with the conductance term. A possible meaning of the depression angle of a semicircular relaxation in a complex plane is discussed elsewhere.[5–10,14]

The C*-plane analysis of the ac electrical data allows a convenient way of examining the bulk intrinsic/native defect corresponding to the dispersion near 10^5 Hz designated as the τ_3 relaxation. Several C*-plane plots of various MOV samples exhibiting this relaxation are presented in references 5 and 6. The τ_3 relaxation yields identical trap-related information when examined via spectroscopic analysis[5,6,10,11] and LP/CPA technique.[5,6] This is depicted in Figure 4. Under a small-signal ac stress, the intersection of the Fermi level and the defect energy varies about its equilibrium position. The time dependence of the ensuing charge transition[5,6] of the τ_3 relaxation as a function of temperature yields an activation energy (E_{τ_3}) and capture cross-section (σ_n). The capture cross-section is usually found to be much less than 10^{-14} cm^2 for the well-formed devices. This suggests that this trap is an attractive center, and therefore, referred to as a donor-like[18] trap.

Additional information is available when τ_3, R_3, and C_3 are plotted as a function of the ambient temperature.[5,6] For an ideal situation, the in-phase resistive element (i.e., R_3) must reflect the activation energy for the trapping time constant τ_3. However, Alim[5] indicated (Figure 5) that about 90% of the activation energy is associated with R_3, and about 10% is with C_3. This is a usual case for the τ_3 relaxation. The trap occupation or charge storage capability should not be temperature dependent, and thus, C_3 should not be thermally activated.[5] Another look of this observation suggests that τ_3 trapping is likely to possess minor leaky capacitive effect. This implies that the equivalent circuit capacitance, C_3, may possess a shunt-like deceptive leakage conductance within itself. The presumption about C_3 with its charge storage capability suggests that the τ_3 relaxation is much more complex than a regular (i.e., usual) non-Debye relaxation. Therefore, τ_3 manifests complexity in the specific defect configuration. This complexity is capable of alternating the neighborhood of the associated donor-like charge occupation for the carrier trapping-detrapping processes at a fixed temperature under quasiequilibrium condition. Another explanation of this hypothesis further suggests that the nature of the τ_3 is momentarily opening and closing (i.e., covering and uncovering) the response for holding the donor-like carrier for the effective trapping-detrapping action. Further, τ_3 indicates as an averaged parameter through the presence of the depression angle (θ_3) in the C*-plane semicircular relaxation. The concept of in-

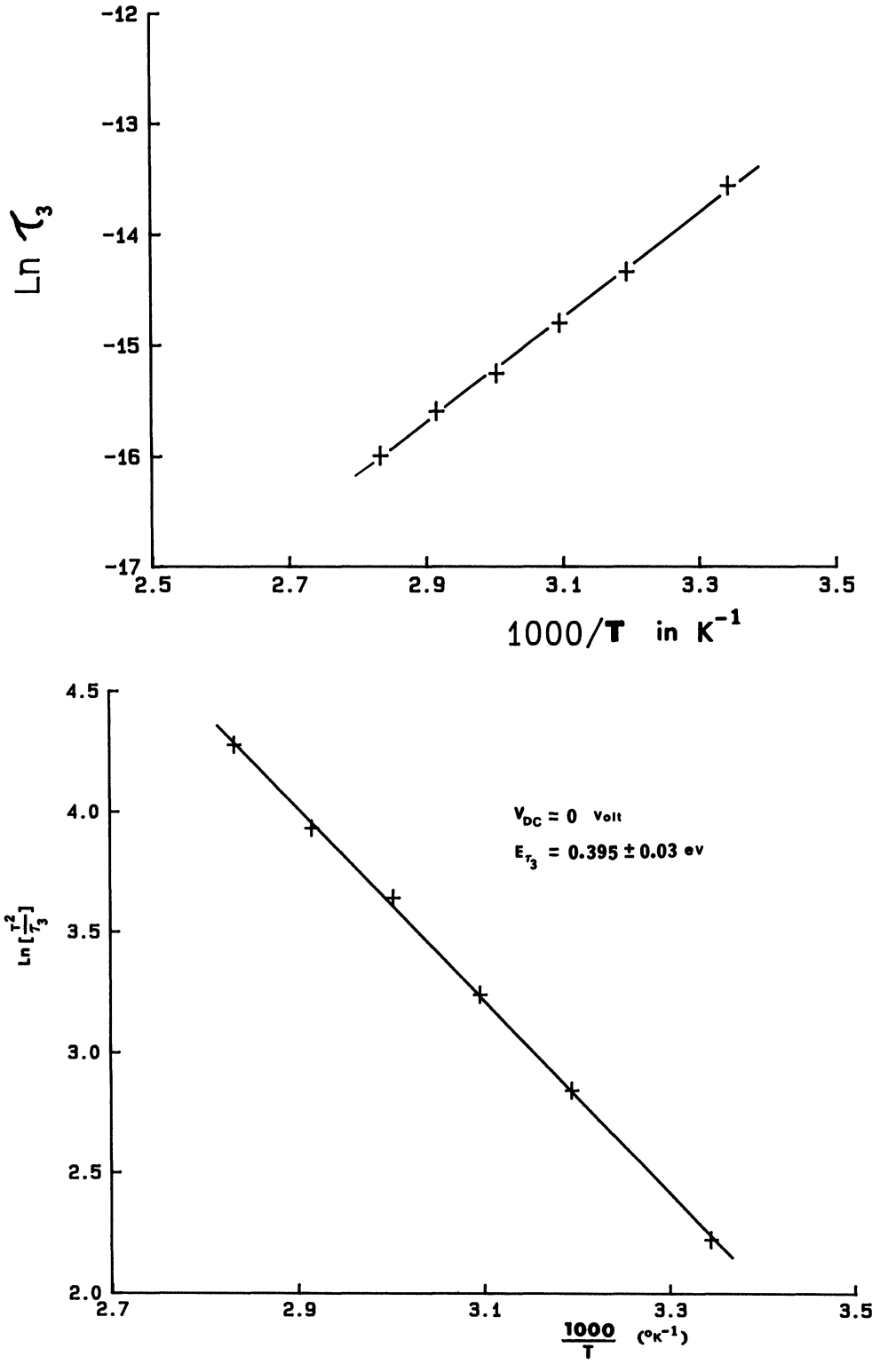

FIGURE 4 Temperature dependence of the common relaxation time (τ_3) using (A) LP/CPA technique, (B) spectroscopic approach.

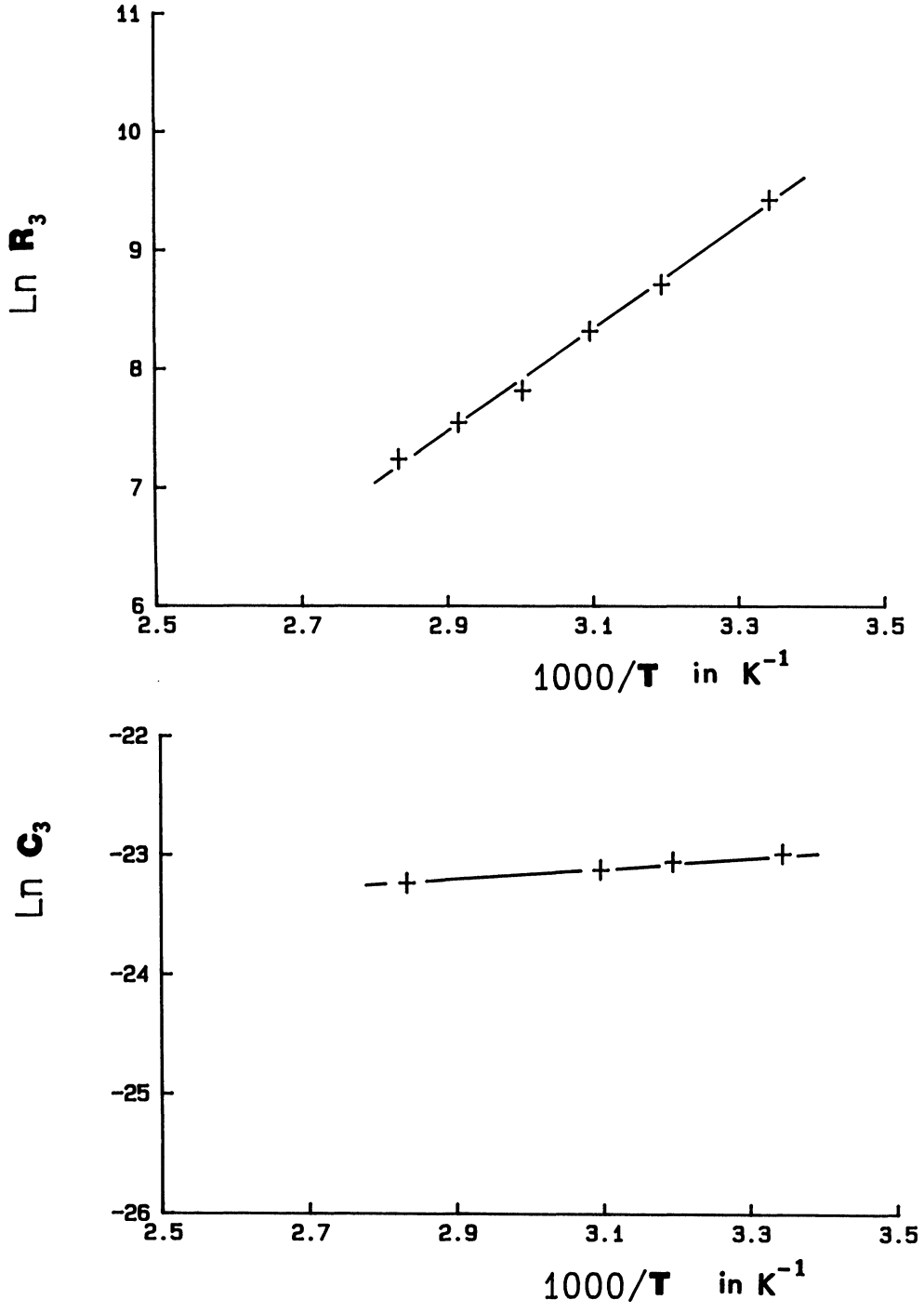

FIGURE 5 Temperature dependence of the common trapping (A) resistance R_3 ($E_{R_3} \approx 0.37$ eV) at zero dc bias, (B) capacitance C_3 ($E_{C_3} \approx 0.04$ eV) at zero dc bias.

homogeneity in the intrinsic defects exists from junction to junction and/or possibly in defect level(s) or energy state(s) within a single junction.[5,6,19] An investigation[16,20] on various single-grain junctions within a ZnO varistor reveals that all junctions are not identical. The origin of these non-uniformities cannot be determined from the measurements of τ_3, R_3, C_3, and θ_3. Therefore, the Debye-like expressions[11,21,22] for the ac conductance and trapping relaxation phenomena are either not valid or cannot be demonstrated for critical examination of this trap. Thus, the total behavior of the τ_3 relaxation is tremendously complex when this information is added to its thermal activation and corresponding presence of the depression angle (θ_3). The origin of such complexity via the concept of radical defect configuration is not known at this time.

The well-formed MOV samples, in general, do not exhibit dc bias ($0 \leqslant V_{dc} \leqslant 80\%V_{1mA/cm^2}$, where V_{1mA/cm^2} is the voltage at current density 1 mA/cm^2) dependence of the τ_3 relaxation and corresponding depression angle (θ_3) as depicted in Figure 6. This indicates that the trap emission or capture rate and cross-section are very nearly independent of dc bias. An invariant response of τ_3 further indicates that the thermal velocity of the released or trapped carriers is not sensitive to the dc biasing. These observations leave no obvious reason leading to the origin of the non-ideal response of the τ_3 relaxation. However, the constituting elements of τ_3 (i.e., R_3 and C_3) exhibit some minor dc voltage dependence in the range $0 \leqslant V_{dc} \leqslant 60\%V_{1mA/cm^2}$). The meaning of this dependence is not very clear at this time.

The insensitive response of θ_3 for the same range of dc biasing (i.e., $0 \leqslant V_{dc} \leqslant 80\%V_{1mA/cm^2}$) implies that the degree of non-uniformity associated with the conductance term remains nearly invariant in this range of dc biasing. The measurement of θ_3 is possible only up to $80\%V_{1mA/cm^2}$ via the C*-plane representation of the immittance data. Above this dc biasing the C*-plane representation is severely distorted, and the data are only representable in the impedance ($Z^* = Z' - jZ''$) plane due to the lossy situation of the device. The Z*-plane representation always exists for the same immittance data at any level of biasing below V_{1mA/cm^2}. Only a single depressed semicircular relaxation results in this plane. Several examples of the Z*-plane representation are cited in references 5 through 8. The existence of the depression angle (θ_{im}) in the Z*-plane semicircular relaxation is associated with the total capacitance,[5,6] $\Sigma_{i=1}^{6} C_i$, at dc condition (i.e., $f \rightarrow 0$ Hz). This total capacitance includes the trapping capacitance C_3. Such a situation constitutes an extraordinary non-Debye response when finite θ_3 is considered concurrently. In general, at $V_{dc} \geqslant V_{1mA/cm^2}$ or within the close proximity $V_{dc} \rightarrow V_{1mA/cm^2}$, the Z*-plane depression angle θ_{im} approaches 0° (i.e., $\theta_{im} \rightarrow 0°$ or equal to 0°). It is worth mentioning that the onset of reduction in θ_{im} takes place near to $80\%V_{1mA/cm^2}$. Alternatively, vanishing θ_{im} indicates a Debye-like conduction state[7] within the device. This behavior suggests that the total capacitance, $\Sigma_{i=1}^{6} C_i$, at the dc condition is achieving a singular value. The behavior of θ_{im} at increasing electric stress levels is documented in Figure 7.

The variation in temperature and dc bias do not alter the meaning of the specific parametric representation of the semicircular relaxation in the Z*-plane. The semicircular loop in this plane yields a chord (diameter for $\theta_{im} = 0°$ at $V_{dc} \geqslant V_{1mA/cm^2}$ or $V_{dc} \rightarrow V_{1mA/cm^2}$) and a very small intercept on its left side on the abcissa.

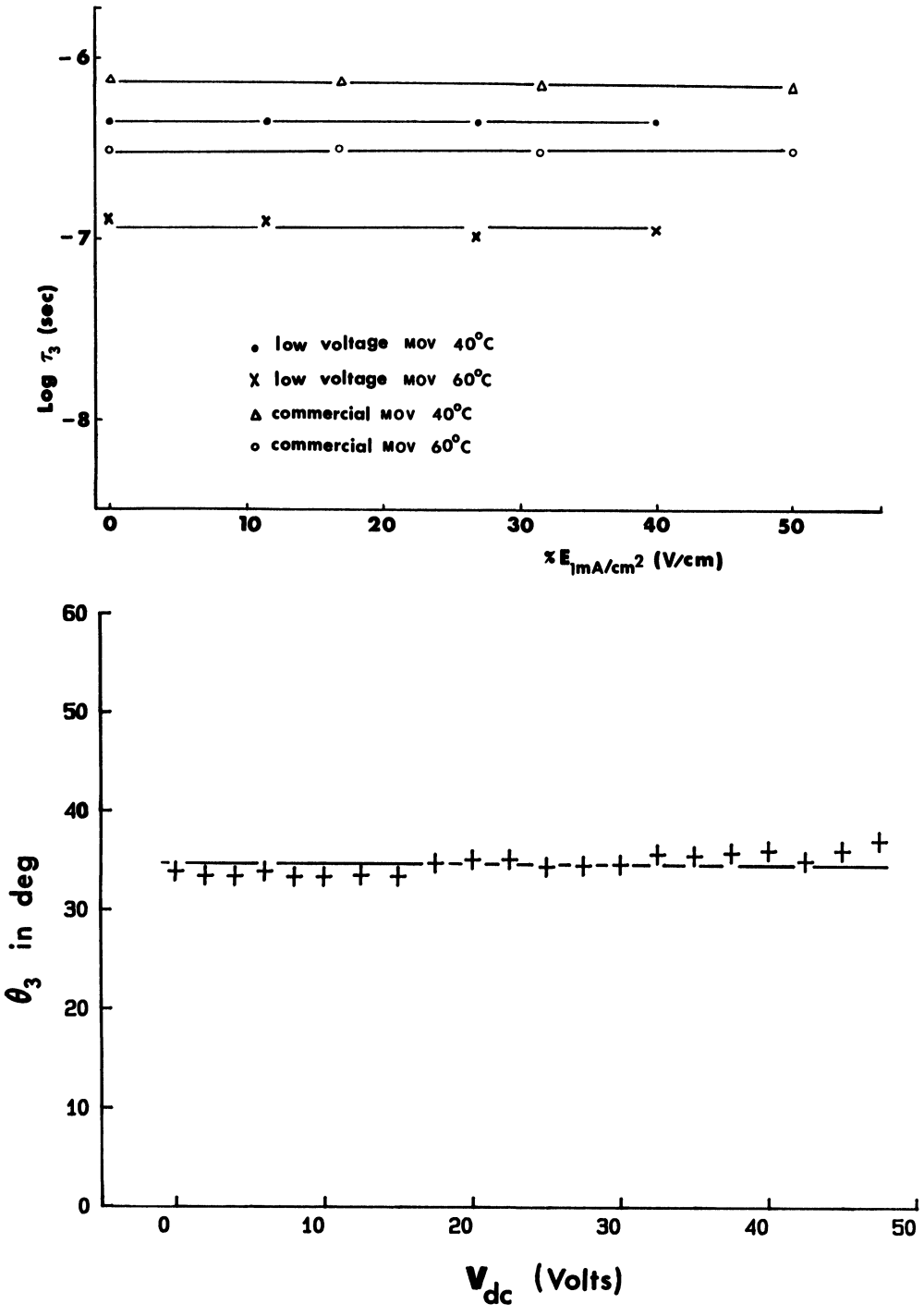

FIGURE 6 (A) Electric Field (dc) dependence of the common trapping relaxation time, τ_3 (E_{1mA/cm^2} is the electric field corresponding to the current density 1mA/cm^2). (B) Voltage (dc) dependence ($0 \leq V_{dc} \leq 80\%V_{1mA/cm^2}$) of the depression angle (θ_3) of the common trapping response at room temperature (V_{1mA/cm^2} corresponds to electric field at E_{1mA/cm^2}).

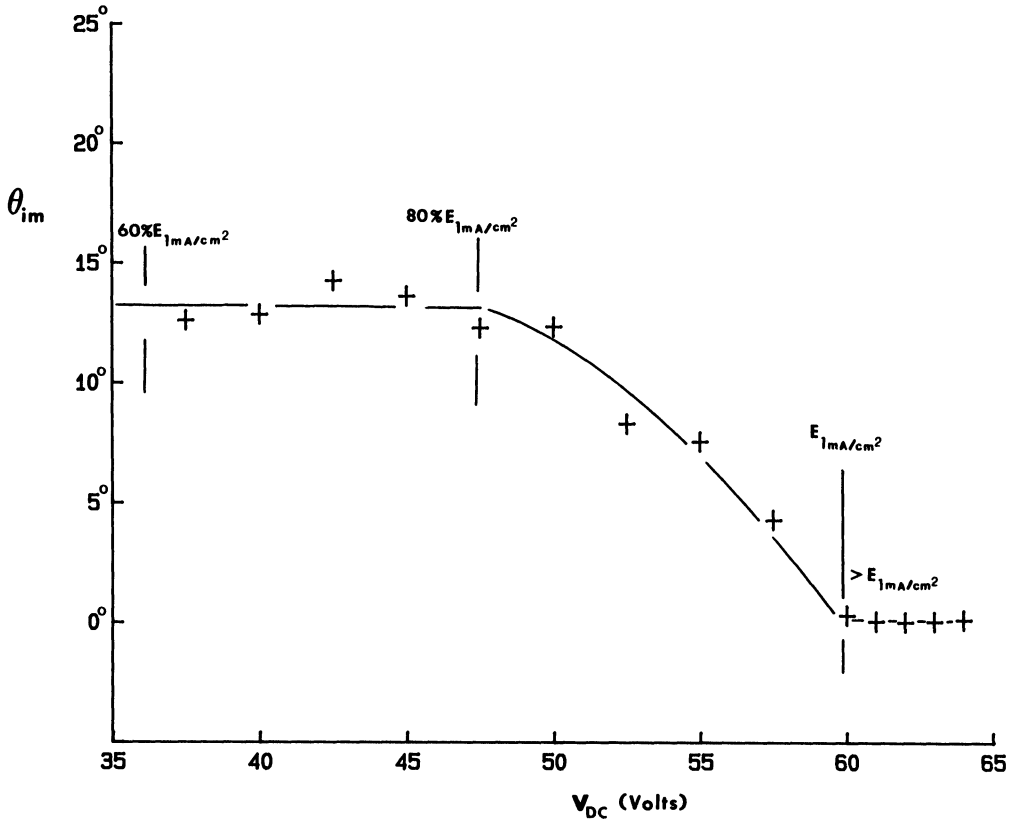

FIGURE 7 Voltage (dc) dependence ($0 \leq V_{dc} \leq \sim V_{1mA/cm^2}$) of the depression angle (θ_{im}) related to the total response of the device.

The summation of these two parameters provides the dc resistance (R_{dc}) of the device. For all practical purposes, the chord can be approximated to the dc resistance as the intercept remains small, which is not often observable in the scaling range of the abcissa parameter (as an example: 10 Ω is too small with respect to $R_{dc} \geq 10^5$ Ω). The intercept is identified as a resistance of the lumped ZnO grains (R_{ZnO}). In the high frequency limit, all relaxations are eliminated and, thus, the barriers become transparent to the ac frequency resulting in lumped grains to constitute a small resistance. It is not unreasonable to assume that the small intercept is associated with the lumped ZnO grains at high frequencies.

INTRINSIC RELAXATION AND OTHER TRAPPING EFFECTS

A remarkable feature of the ZnO-Bi_2O_3 based varistors, based upon observations, is that the lumped trapping capacitance (i.e., $C_1 + C_2 + C_3 + C_4$ or $\Sigma_{i=1}^{4} C_i$ from Figure 1) can be distinguished among the devices. This assumes C_{BL} ($= C_5 + C_6$)

to be nearly constant for all devices regardless of composition recipe and processing variables, implying a demarcation between a good performance and a weak (poor) response of the devices. Often, τ_4 relaxation is not distinct and masked by the emergence of the resonance phenomenon.[6,14] Such devices, though well-formed, yield very little information on the τ_4 relaxation. In the event the τ_4 relaxation is visible, no relationship can be assessed easily between the performance and composition recipe or processing variables. For each set of variables within the well-formed device configuration, the constituting elements possess nearly identical values. The τ_4 relaxation (usually observed $\sim 10^{-8}$ s) as well as its constituting elements have much less impact on the degradation or failure of the devices. This trapping relaxation is somewhat insensitive to the sintering temperature and soak time for the well-formed MOVs. However, these processing parameters are necessary to originate this relaxation. Another perspective of these defects associated with the τ_4 relaxation is that they are likely to occupy permanent sites within the electrical thickness. Thus, either their destruction or alteration of the constituting equivalent circuit elements (using $\tau_4 = R_4C_4$) may not be possible unless a serious change occurs in achieving a well-formed device. This hypothesis implies that the τ_4 relaxation or its constituting elements can be treated as nearly invariant at quasiequilibrium conditions.

The τ_3 relaxation follows a definite pattern for the right composition recipe and processing route with respect to the behavior of τ_2 and τ_1. The foregoing discussion, addressing the dc behavior of the device, may influence the resulting effect of τ_2 and τ_1 relaxations. Thus, the pattern of τ_3 is strongly associated with the τ_2 and τ_1 relaxations if two devices possess non-identical τ_1, τ_2, and τ_3 relaxations satisfying the applications criteria. Extending this concept, further, a method can be developed to judge a better device between two well-formed satisfactory devices. These issues are also important to distinguish a good performance from a poor response and systematically investigated.

A strong sensitivity is observed in the τ_2 relaxation and the shape of the distortion associated with the τ_1 trapping. Typically, the τ_2 relaxation can vary between 10^{-4} s and 10^{-2} s. This range determines the value of R_2 and C_2. In general, C_2 plays the key role in determining the value of C_3 and, thereby, the value of τ_3 for a satisfactory value of R_3. This interrelationship is subject to verification of the device's dielectric behavior at dc condition. This condition presumes $C_1 + C_2 + C_3 + C_4$ ($\Sigma_{i=4}^{4} C_i$) to be small but finite for good devices. Often, τ_2 relaxation is found to be heavily distorted, and becomes difficult to extract its value. In such cases, a wide range in measurement frequencies including the low-frequencies can delineate the total value of capacitance at the dc condition (i.e., $\Sigma_{i=1}^{6} C_i$ as $f \rightarrow 0$ Hz). For this purpose, these data must be analyzed in the Z*-plane to obtain a single depressed semicircular relaxation. The relaxation time (τ_{im}) obtained in this semicircle originates from its chord and the capacitance at the dc condition. An example of the Z*-plane representation is provided in references 5 and 6. Thus, $C_1 + C_2$ can be obtained as a lumped quantity, which dictates the range of τ_3 and the corresponding numerical values of its constituting elements. In the event of a clear detection of C_2, C_1 must be extracted in an identical manner. For this case $C_1 + C_2$ can be also treated as a single lumped quantity.

The element R_2, if possible to determine from the τ_2 semicircular relaxation in the C*-plane, is a controlling parameter for the accelerated life-test, steady nature of the watts-loss at elevated temperatures, and thermal runaway behavior of the device. For an excellent device, both R_2 and R_3 must possess high values. A compromise between them may result in an intermediate or a poor device. In practice, R_2 or R_3 or R_4 is always at least one or several orders less than R_{dc}. Nearly no information can be extracted on the numerical value of the τ_1 relaxation using the LP/CPA technique. However, the value of C_1 can be obtained using combined C*- and Z*-plane plots for the same immittance data, at least when these are acquired in the range $10^{-2} \leqslant f \leqslant 10^9$ Hz. The dc measurement can only complement this information. The presence of C_1 can be verified with the immittance data within $\sim 10^3$ Hz but may not be quantified unless other relaxations are distinguished in the frequency domain.

Since C_1 through C_4 exhibits a strong frequency dependence, it is reasonable to distinguish extreme kinds of devices with respect to their magnitudes. Such a situation leads to two distinct cases, observed for all normalized (i.e., considering geometry or dimension) configuration of the MOV samples at a specific (i.e., arbitrarily chosen) frequency, before approaching resonance phenomena. Thus, the terminal parallel capacitance (C_p) can be distinguished as *large* and *small*. Extending C_p to the dc condition and assuming a nearly constant C_{BL}, this observation provides:

$$\sum_{i=1}^{6} C_i = \textit{large}, \quad \text{and} \quad \sum_{i=1}^{6} C_i = \textit{small}.$$

The terms "*large*" and "*small*" are absolutely dependent on the devices' composition recipe, raw materials' history, and processing variables. Further, these terms are empirical and absolutely dependent on a series of systematic evaluation steps.

In order to distinguish between two unknown MOV samples, the aforementioned situation must be distinguished as a critical demarcation at the dc condition. This critical demarcation implies on both well-formed and weak (poor) devices. Inspecting the values of individual C_i (i = 1 through 6) and a tentative scrutiny procedure may provide a clear distinction among the devices. Ultimately, a demarcation between a good and a poor response is achieved via a thorough evaluation process. Such a decision is based purely on a systematic trend of the electrical response and the dispersion of immittance with ac frequency. Thus, these devices allow a classification in a sequential order with respect to the chemistry or composition/formulation and processing history. The exact reason for the empirical establishment between the nature of the dispersion in terminal immittance as a function of ac frequency and performance characteristics is not known at this time. However, this relation is believed to be attributed to the charge states of the traps originated from the nature of the defect configuration sustaining an electrical barrier across the grain-boundary. These traps have possibly emerged into existence through the influence of the pre-determined processing cycles.

Several summary cases, related to τ_3 or its constituting elements, can reveal

good performance and/or satisfy the requirements for the applications criteria of such a device. These cases are noted below:

1. large C_3 (small R_3) with respect to another device whose C_3 is small and just enough to balance $\Sigma_{i=1}^{6} C_i$ = *small*, possessing identical (or nearly the same) value for τ_3;
2. small C_3 (large R_3) with respect to another device whose C_3 is large and just enough to balance $\Sigma_{i=1}^{6} C_i$ = *small*, possessing identical (or nearly the same) value for τ_3;
3. large C_3 (small R_3) with $C_1 + C_2 + C_4$ = *small* with respect to another device, and also small C_3 (large R_3) with $C_1 + C_2 + C_4$ = *small* with respect to another device;
4. range of *finite* depression angle for the τ_3 semicircular relaxation in the C*-plane: $12 \leqslant \theta_3 \leqslant 36°$, and range of *non-vanishing* (i.e., non-zero or finite) depression angle for the Z*-plane semicircular relaxation: $\theta_{im} \leqslant 18°$;
5. sharp and asymptotic approach to infinity (Figure 1) for the τ_1 relaxation indicating *small* C_1 yielding a distinct dc limit.

Recognizing a poor device is not a very difficult task. Any parameter falling outside the aforementioned limiting range observations will lead to a poor or weak device. Such devices can be eliminated outright after a non-destructive evaluation utilizing the LP/CPA technique. Some rejecting features are summarized below:

1. large C_3 (small or large R_3) with $C_1 + C_2 + C_4$ = *large* (with or without distortion of τ_2 and/or τ_1 relaxations and small R_2); and
2. range of depression angle for the τ_3 semicircular relaxation: usually $\theta_3 \geqslant 36°$.

The proof of the above findings remain empirical, but useful, and the cause to each occurrance is not adequately addressed in the literature. The discussion suggests that a passive relationship exists between τ_3 and τ_2 or combined τ_2 and τ_1. This implies that a large value of R_3 has a tendency to yield a better device. This large value reduces the polarization (or drift) effect observed at low-frequencies (i.e., possibly τ_2 and/or τ_1 related). Such information is believed to have been reported in the recent papers by Modine et al.[23] and Leite et al.[12] The low frequency traps (τ_2 and/or τ_1) are simultaneously affected when the device is subjected to a degradation. Furthermore, this information is likely to have been supported via another representation of the GB barrier (i.e., perhaps similar to the evidence cited by Modine et al. and Leite et al.) via its deformation).

CONCLUSIONS

The evaluation procedure employs the lumped parameter/complex plane analysis technique. This technique reveals several contributions to the terminal immittance including multiple trapping phenomena, barrier layer capacitance, and a resonance

effect. The barrier layer capacitance is presumed to be nearly constant as the carrier and defect concentrations remain identical for all devices investigated.

The role of the τ_3 relaxation and its constituting elements R_3 and C_3 in conjunction with the depression angle θ_3 (or corresponding parameter h_3) are examined considering the nature of other trapping effects (such as: τ_4, τ_2, and τ_1) in the ZnO-Bi_2O_3 based varistors. The depression angles, θ_3 and θ_{im}, of the τ_3 relaxation and Z*-plane single semicircular relaxation, respectively, are also examined below $80\%V_{1mA/cm^2}$. Although the magnitude of the τ_3 relaxation, θ_3 and θ_{im} are not very sensitive to the composition recipe and/or processing variables, the associated constituting parameters of τ_3 are found to be seriously sensitive. This sensitivity ensures device function via the component contributions of other trapping effects (such as: C_4, C_2, C_1, etc.) for applications. The nature of the τ_3 relaxation possibly ensures the characteristics of τ_2 and/or τ_1 (when these two are combined together) via processing variables for a specific composition recipe. Finally, the τ_3 relaxation indicates (and/or possibly dictates) a devices' overall performance for the applications criteria based upon systematic findings.

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