SIMULATION OF CROSSTALK IN HIGH-SPEED MULTI-CHIP MODULES

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Simulation results of the electrical performance at 1 GBits/sec of a number of different off-chip interconnection architectures are presented with emphasis given to the dependence of crosstalk and signal delay on the geometries and dielectric constants of the insulating layers as well as on the widths and separations of the conductors. The results indicate that signal delay and crosstalk may be reduced by using low ϵ_r values for the dielectrics and that crosstalk may be also reduced by reducing the conductor-to-ground wire separation which simultaneously neutralises the role of ϵ_r value on crosstalk and line impedance.

1. INTRODUCTION

As the speed of the logic devices increases, the performance limits of the off-chip electrical interconnections (i.e. multilayer motherboards, multi-chip modules, etc.) become an important matter of concern. Also, maximisation of the density of the interconnect lines may lead to undesirable coupling between adjacent signal paths. Modelling the relationship between the geometry and material properties of the interconnect medium and their electrical characteristics is important so that trade-offs can be made between technology selection and performance.

When rise times decrease below 2 ns, terminated transmission line interconnects between ICs are necessary; otherwise, multiple reflections on unterminated lines can degrade the waveform characteristics throughout the entire clock period. The shorter the off-chip signal rise time, the more necessary and the more difficult it is to establish uniform transmission line behavior of the interconnects. The most commonly employed transmission line values¹ are in the range of 50–75 Ohm. Although higher line impedance values such as 100 ohms are also possible, the line becomes more susceptible to crosstalk when line impedance exceeds 75 ohms, while reflections become more serious².

The advanced developmental work in this field is attempting to develop new methods for creating substrates which can support very dense interconnects (up to 1000 linear cm of interconnect per square cm of substrate real estate), fine line geometries (down to 5 μm in width, and comparable to those on the integrated circuits themselves), and favourable electromagnetic properties, i.e. low waveform degradation and crosstalk.

The very high density of the interconnect structures which will be required in next-generation subsystems will in turn make it difficult to create transmission line paths for the signals while simultaneously minimising wavefront reflections due to transmission line discontinuities and crosstalk between adjacent lines.

The purpose of this work is the extraction of design rules for off-chip interconnections, through simulation, using a software package developed for the electrical modelling of lossy-coupled multilayer off-chip interconnection lines at high bit rates. The formulation of lossy coupled multiconductor interconnection lines, which at high bit rates (1 GBit/sec) must be considered as transmission lines, is obtained using a free-space Green's function in conjunction with total charge on the conductor-to-dielectric interfaces and polarisation charge on the dielectric-to-dielectric interfaces. The solution is derived by applying the method of moments³ and it is based on the TEM/quasi-TEM assumption which has been reported⁴ to be accurate for frequencies up to several gigahertz and for rise times of the order of 50 ps for a typical stripline or microstrip structure.

2. THE ELECTRICAL MODEL

The evaluation of the electrostatic parameters, including capacitance, inductance, conductance and resistance matrices, and attenuation factors as well as propagation constants and characteristic impedance for the given multiconductor geometry, is computed initially. A multiple coupled line model consisting of uncoupled lines and linear dependent current and voltage sources is finally calculated according to the capacitance, inductance, conductance and resistance matrix values computed.

2.1. Capacitance, Inductance, Conductance and Resistance Matrices

The elements of the capacitance matrix are calculated by relating the free charge per unit length of surface on the conductors to the potentials of the conductors.

At any point $\underline{r}$ on the i -th conductor-to-dielectric interface, the potential Φ_i due to the combination of σ_T and the image of σ_T above the lower ground plane is assumed to be constant (first boundary condition), and it is given by the following equation which is derived from the appropriate Green's function applying the method of images³:

$$\frac{1}{2\pi\epsilon_0} \sum_{j=1}^N \int_{S_j} \sigma_T(\underline{r}') \ln \left(\frac{|\underline{r}' - \hat{\underline{r}}'|}{|\underline{r} - \hat{\underline{r}}'|} \right) dS' = \Phi_i \quad (1)$$

where S_j is the boundary of the j -th interface in the xy plane, dS' is the differential element of length at $\underline{r}'$ on S_j , $\hat{\underline{r}}'$ is the image of $\underline{r}'$ about the lower ground plane, and N is the total number of interfaces ($N_c + N_d - 1$).

The second boundary condition refers to the y component of the displacement vector $\underline{D}(\underline{r})$ which is assumed to be continuous across each i -th dielectric-to-dielectric interface, thus:

$$(\epsilon_{i-N_c}) \left. \frac{\partial \Phi(\underline{r})}{\partial y} \right|_+ \underline{u}_y = (\epsilon_{i+1-N_c}) \left. \frac{\partial \Phi(\underline{r})}{\partial y} \right|_- \underline{u}_y \quad (2)$$

$$i = N_c + 1, N_c + 2, \dots, N, \quad \underline{r} \text{ on } S_i$$

where ϵ_{i-N_c} is the permittivity on the upper side of S_i , and $\partial\Phi(\underline{r})/\partial y|_+ \underline{u}_y$ is the normal component of the electric field on the upper side of S_i .

The electric field $\underline{E}(\underline{r})$ when $\underline{r}$ approaches the interface S_i is given by the following equation:

$$\frac{(\epsilon_{i+N_c} + \epsilon_{i+1-N_c})}{2\epsilon\epsilon_0(\epsilon_{i-N_c} - \epsilon_{i+1-N_c})} \sigma_T(\underline{r}) + \frac{1}{2\pi\epsilon_0} \sum_{j=1}^N \int_{S_j} \sigma_T(\underline{r}') \left(\frac{\underline{r} - \underline{\hat{r}}'}{(\underline{r} - \underline{\hat{r}}')^2} - \frac{\underline{r} - \underline{r}'}{(\underline{r} - \underline{r}')^2} \right) \underline{u}_y dS' = 0 \quad (3)$$

Equations (1) and (3) constitute a set of N integral equations for the unknown total charge σ_T per unit area on the interfaces whose contours are S_i . The capacitance coefficients C_{ij} between conductors i and j are³

$$C_{ij} = \int_{S_i} \frac{\epsilon(\underline{r})}{\epsilon_0} \sigma_{T(j)}(\underline{r}) dS_i \quad (4)$$

If an upper ground plane exists, it is considered as an ordinary conductor j ; so that the reduced capacitance matrix $[C]$ is found by deleting the j -th row and column.

For the calculation of the C_{ij} the integral equations (1) and (3) may be solved numerically for σ_T by the method of moments⁵.

It is known that⁶:

$$[L] = \mu_0\epsilon_0[C_0]^{-1} \quad (5)$$

where C_0 is the capacitance matrix which would result if all dielectric layers were replaced by free space. The complex permittivity of the i -th loading layer given by $\epsilon_i = \epsilon'_i - j\epsilon''_i = \epsilon'_i (1 - j \tan \delta_i)$ where, ϵ'_i and ϵ''_i are the real and imaginary parts of ϵ_i and $\tan \delta_i = \epsilon''_i/\epsilon'_i$ is the loss tangent, the so-called dissipation factor, which it represents the losses of the dielectric medium, consequently:

$$j\omega[C'] = [G + j\omega C] \quad (6)$$

The conductance which is the real part of (I.20), is calculated as:

$$[G] = -\text{Im}[\omega C'] \quad (7)$$

The resistance matrix is calculated by applying the perturbation theory⁴ to the loss-free line system which is described by the following eigenvalue equations:

$$[C][L]I_0 = \frac{1}{V_p^2} I_0 \quad (8)$$

$$[L][C]V_0 = \frac{1}{V_p^2} V_0 \quad (9)$$

where the subscripts^o denote unperturbed, and V_p is the phase velocity.

The time-average power transmitted along the line, is $P_T = \text{Re} ((I^T)^* V)$ and thus, the unperturbed power flow is $P_T^0 = I^{T0} V^0$. The power loss per unit length, P_c , of the transmission line can be calculated by the following formula:

$$P_c = \sum_i R_s \int_i J_i^2 \quad (10)$$

where R_s is the surface resistance of the metal, J_i is the current density on the i -th conductor, and the integral is taken over all metal surfaces S_i . Equation (10) is evaluated by using the moment solution. Once P_c is evaluated for a given mode, attenuation due to conductor losses is given by:

$$a_c = \frac{P_c}{2P_0 T} \quad (11)$$

The resistive matrix per unit length $[R]$ can now be evaluated, if $G \ll \omega C$ then

$$(\alpha_c + j\beta)^2 V = [R + j\omega L][j\omega C]V \quad (12)$$

If the losses are low⁷, we can take $V \gg V^0$ to be real, setting $\beta \gg \beta^0$ and using (8), equation (12) reduces to

$$2\alpha_c V^0 \gg [R]I^0 \quad (13)$$

from which $[R]$ can be calculated since α , V^0 , and I^0 are known for each mode.

2.2. Multiport Model

At the second phase, a multiple coupled line model consisting of uncoupled lines and linear dependent current and voltage sources is calculated according to the $[C]$, $[G]$, $[R]$ and $[L]$ matrix values computed. Taking into account that the uniform system under consideration is linear and time invariant, and for $e^{j\omega t - \gamma z}$ variation, we obtain:

$$\frac{d^2 V}{dz^2} = [R + j\omega L][G + j\omega C]V \quad (14)$$

$$\frac{d^2 I}{dz^2} = [G + j\omega C][R + j\omega L]I \quad (15)$$

Let $[M_u]$ be the eigenvector matrix associated with the characteristic matrix $[R + j\omega L][G + j\omega C]$. The voltage and current eigenvectors $e]$ and $j]$, respectively, are the solutions of the decoupled set of equations

$$\frac{de]}{dz} = -\text{diag} \left[\frac{\gamma_k}{y} \right] j] \quad (16)$$

$$\frac{dj}{dz} = -\text{diag} [\gamma_k y_k] e \quad (17)$$

$$\begin{bmatrix} V \\ I \end{bmatrix} = \begin{bmatrix} [M_u] & [0] \\ [0] & [(M_u)^T]^{-1} \end{bmatrix} \begin{bmatrix} e \\ j \end{bmatrix} \quad (18)$$

where γ_k is the propagation constant for the k-th mode and is the square root of the k-th eigenvalue of the $[R + j\omega L][G + j\omega C]$ matrix and y_k is the characteristic admittance of the k-th mode and is the corresponding element of the diagonal matrix $[Y_k]$ which is given by

$$[Y_k] = [M_u]^{-1} [Y_{SH}] [M_u] \quad (19)$$

The previous equations lead to the 2n port circuit model representing n lossy parallel lines as shown in Fig. 1.

3. SIMULATION

Simulation of the electrical performance of a number of different interconnection architectures has been performed with emphasis given to the dependence of cross-talk, signal delay and distortion on the geometries and dielectric constants of the insulating layers as well as on the cross sections and spacings of the conductors.

FIGURE 1 2n Port circuit model.

Architectures that have been adopted⁸ in practice so far may be classified in three categories: a) simple multilayer metallizations, b) active conducting path layers separated by ground planes and c) interconnections separated by ground wires. Calculations carried out assuming as the length of the conductors 1 cm.

3.1. Performance of a Conventional Geometry Structure

Consider the structure shown in Fig. 2(a). The thickness, H , of the substrate with relative dielectric constant 12 is $200\text{ }\mu\text{m}$ and the conductors are embedded in a dielectric medium with relative dielectric constant of 3.9. The height, t , of the conductors is $2\text{ }\mu\text{m}$. The variation of the characteristic impedance for several conductor widths, W , starting from 4 to $16\text{ }\mu\text{m}$ is shown in Fig. 3 as curve #1. It decreases slightly from 100 Ohms to 96 Ohms when the conductor width increases from $4\text{ }\mu\text{m}$ to $16\text{ }\mu\text{m}$ respectively. Assuming the height of the conductors to be $2\text{ }\mu\text{m}$, and the width $8\text{ }\mu\text{m}$, the crosstalk is calculated when the left line is the active one and the right one is passive (off-state of the driving transistor). We assume the output resistance of the driving transistors, either in on- or off-state, to be 15 Ohms . The dependence of crosstalk on conductor spacing is shown in Fig. 4 curve #2. It is shown that increasing the spacing, S , between the conductors from $8\text{ }\mu\text{m}$ to $30\text{ }\mu\text{m}$ crosstalk decreases, from -2.5 dB to only -6 dB .

This is also shown in Fig. 5 where curves #3 and #4 represent the crosstalk curves, (for conductors spacing $8\text{ }\mu\text{m}$ and $30\text{ }\mu\text{m}$ respectively) with curve #7 representing the active conductor input pulse.

FIGURE 2 Investigated architectures (distances in micrometers).

FIGURE 3 Characteristic impedance as a function of conductors width.

3.2. Performance in the Presence of Ground Planes

Addition of a ground plane at a distance H_2 above the substrate, as shown in Fig. 2(b), an architecture which is frequently suggested in the literature, alters the electrical performance of the structure: it reduces the line impedance but it increases

FIGURE 4 Crosstalk as a function of conductors spacing for architectures 2(a), 2(b), 2(c).

FIGURE 5 Crosstalk and input signals for various architectures and spacings.

the crosstalk by about 5%. More specifically the impedance is reduced by about 15% with the addition of the upper ground plane and it may be further reduced by another 15% if the distance of the upper ground plane from the substrate is reduced from $40\text{ }\mu\text{m}$ to $20\text{ }\mu\text{m}$ and the conductors width is increased from $4\text{ }\mu\text{m}$ to $16\text{ }\mu\text{m}$, as shown in Fig. 3 (curves #2, #3, #4 for $40\text{ }\mu\text{m}$, $30\text{ }\mu\text{m}$ and $20\text{ }\mu\text{m}$ respectively). The increase in crosstalk can be seen from Fig. 4 curve #2 in comparison with curve #1 (which represents crosstalk for the conventional geometry structure), but also from Fig. 5, where curves #1 and #2 represent the crosstalk curves, (for conductors spacing $8\text{ }\mu\text{m}$ and $30\text{ }\mu\text{m}$ respectively) with curve #7 representing the active conductor input pulse.

The addition of the upper ground plane deteriorates crosstalk slightly whereas the increase of the conductor separation from $8\text{ }\mu\text{m}$ to $30\text{ }\mu\text{m}$ improves electrical performance by only about 4%.

3.3. Performance in the Presence of Ground Wires

A drastic decrease in both crosstalk and line impedance may be achieved by adopting the interconnection architecture shown in Figs. 2(c) and 2(d), as it is described next. Fig. 3 (curve #5) shows that line impedance is also reduced by about 35% by increasing the width of the conductor from $4\text{ }\mu\text{m}$ to $16\text{ }\mu\text{m}$. Fig. 4 (curve #3) shows that the introduction of a ground wire of a cross section of $2\text{ }\mu\text{m} \times 8\text{ }\mu\text{m}$ between two conducting paths of the same cross section reduces the crosstalk to about -16 dB .

Further decrease of crosstalk may be achieved by reducing the separation between the conductors and the ground wire. Simulation results (Fig. 4 curve #3)

FIGURE 6 Crosstalk pulse for various conductors spacing for the architecture 2(a).

show that when separation reaches $8\text{ }\mu\text{m}$ crosstalk is expected to be reduced to -22 dB . Notice that in Fig. 5 curve #5 (which refers to conductor spacing of $30\text{ }\mu\text{m}$) has bigger absolute values than curve #6 (which refers to conductor spacing of $8\text{ }\mu\text{m}$). This inversion of the crosstalk-spacing curve can be seen more clearly in Figs. 6, 7, 8 (for architectures as shown in figures 2(a), 2(b) and 2(c) respectively),

FIGURE 7 Crosstalk pulse for various conductors spacing for the architecture 2(b).

FIGURE 8 Crosstalk pulse for various conductors spacing for the architecture 2(c).

where curves #1, #2 and #3 refer to conductor spacing of $8\ \mu\text{m}$, $17\ \mu\text{m}$ and $30\ \mu\text{m}$ respectively. Investigation of the effect of conductor separation and the width of the ground wire on crosstalk produced the results shown in Fig. 9. The curves #1, #2 and #3 correspond to ground wire widths of $2\ \mu\text{m}$, $4\ \mu\text{m}$ and $8\ \mu\text{m}$ respectively. It is apparent that reduction of the ground wire width deteriorates the electrical performance even at practically low conductor spacing values. Consequently the simulation results dictate a width for the ground wire at least equal

FIGURE 9 Crosstalk as a function of conductors spacing for several ground wire widths ($2\ \mu\text{m}$, $4\ \mu\text{m}$, $8\ \mu\text{m}$).

FIGURE 10 Crosstalk as a function of conductors spacing for several dielectric constants.

to the width of the conducting lines together with a conductor-to-ground wire separation of less than $10\text{ }\mu\text{m}$. A compromise, however, may be desirable in order to increase interconnection density. For example adoption of a ground wire width of $2\text{ }\mu\text{m}$ with $8\text{ }\mu\text{m}$ conductor separation may deteriorate crosstalk by 4 dB (from -21 dB to -17 dB , Fig. 9), but it is expected to increase interconnection density by approximately 15%.

The effect of the dielectric constant of the insulating layer in the crosstalk has been also investigated (assuming a width of $2\text{ }\mu\text{m}$ for the ground wire and $8\text{ }\mu\text{m}$ for conductor separation) and the results are given in Fig. 10.

As it was expected¹ on MCMs manufactured with today's technology (i.e. conductor spacing of the order of $30\text{ }\mu\text{m}$) the use of low dielectric constant insulating layers is necessary in order to suppress crosstalk. This is shown in Fig. 10 where curves #1, #2, #3, #4 correspond to dielectric constants $\epsilon_r = 6.7, 5.0, 3.5$ and 2.0 , respectively. For a conductor spacing of $30\text{ }\mu\text{m}$ a reduction of dielectric constant from 6.7 (a value which corresponds to Beryllium Oxide) to 2.0 (a value which corresponds to Teflon) suppresses crosstalk by about 3 dB, whereas the reduction of conductor spacing from $30\text{ }\mu\text{m}$ to $10\text{ }\mu\text{m}$ not only suppresses crosstalk by another 3 dB but it also minimises the effect of the dielectric constant on the crosstalk level. One could also notice the difference in Fig. 11 where curves #1, #2, #3 and #4 refer to dielectric constants $\epsilon_r = 6.7, 5.0, 3.5$ and 2.0 , respectively. Furthermore, dimensional scaling down procedure is expected to improve the level of the output signal (reduce signal losses/cm), as shown in Fig. 12. In addition, the adoption of low-dielectric constant materials are expected to minimise the output signal delay on the active line as shown in Fig. 13 with curves #1, #2, #3 and #4 referring to dielectric constant $\epsilon_r = 6.7, 5.0, 3.5$ and 2.0 , respectively. These simulation results show that signal losses per cm in a geometry like the one shown in Fig. 2(c) are reduced considerably (from 4.5 dB to 1.5 dB depending on the dielectric constant value) by reducing the spacing between conductors and ground wire from $30\text{ }\mu\text{m}$

FIGURE 11 Crosstalk pulse for several dielectric constants (spacing = 30 μm).

FIGURE 12 Signal losses on the active conductor as a function of the conductors spacing for several dielectric constants.

FIGURE 13 Output pulse on the active conductor for several dielectric constants.

FIGURE 14 Crosstalk as a function of conductors spacing for two different output impedances of the inactive line driver.

down to $8\ \mu\text{m}$ with a simultaneous neutralisation of the role of the dielectric constant value.

Application of the grounding wire architecture in a multilayer situation as it happens in practice for MCMs, would result in a cross-section geometry like the one shown in Fig. 2(d). The results of the simulation as far as crosstalk is concerned are shown in Fig. 14. Curve #1 shows the simulated crosstalk between lines on different layers when the output impedance of the driver of the inactive line is 15 Ohm whereas curve #2 shows the reduction of crosstalk with decreasing conductor-to-ground wire spacing when the output impedance of the driver of the inactive line is 50 Ohm. It is apparent that in order to minimise crosstalk it is also necessary to terminate the input of the inactive line (while it is inactive) with a 50 Ohm resistor and each output with a resistor equal to its characteristic impedance⁹.

4. CONCLUSIONS

Simulation of the electrical performance of two major MCM architectures, i.e. employing ground planes or ground wires for electrical isolation, has been performed at 1 GBit/sec. Simulation results indicated that the latter architecture is superior as far as crosstalk suppression and signal delay minimization (if low-dielectric constant materials are used) is concerned.

A very interesting conclusion which emerged from the simulation is that in the case of the ground wire architecture a dramatic reduction of crosstalk ($-20\ \text{dB}$) is expected when the conductor-to-ground wire separation decreases below $8\ \mu\text{m}$ independently of the value of the dielectric constant of the insulating layers. This

figure may be further reduced down to -38 dB if care is taken so that the output impedance of the driver of the inactive line is around 50 Ohm.

Finally, scaling down of the conductor-to-ground wire separation to $8\text{ }\mu\text{m}$ is expected to reduce signal losses on the active lines by 4 dB and simultaneously to neutralize the effect of dielectric constant value.

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