

ANALYSIS AND MODELING OF DEPLETION-MODE MOS TRANSISTORS

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Depletion mode MOSFETs are widely used in MOS—LSI/VLSI circuits as load elements. The main advantages offered by these devices are:

- Higher packaging density,
- Improved performance,
- Reduced power consumption, etc.

Masuhara et. al (1972) developed a model for analysis of this device as an enhancement mode MOSFET. The model was adequate for analysis of lightly-doped, shallow-implanted channels. Subsequently, a more rigorous analysis was put forth by HAKEN for larger doping and deep channels. The analysis made by Edward and Marr did not simplify the non-linear relationship between surface depletion region width and gate voltage. The model also did not account for the transconductance of the device in the three operating regimes.

In this paper, the various models are briefly examined, and an attempt has been made for extraction of various parameters for obtaining the DC characteristics of these devices.

INTRODUCTION

MOSFETs are classified as depletion-type MOSFETs or enhancement-type MOSFETs, depending on the operation principles. Buried channel MOSFETs are not new. These are obtained by introducing within the surface region impurities of opposite type to that of the substrate impurities. Thus, a conducting channel between the source and drain contacts exists in a direction parallel to the interface but below it. The width of the neutral channel region is restricted by a surface depletion region and a bulk depletion region. Thus, a junction of depletion regions is formed around the metallurgical junction, whose local width depends on the externally applied voltages. The operation of buried-channel depletion-mode MOS transistors is explained in Fig. 1.

The various modes of operations are:

- (1) Complete enhancement/accumulation mode.
- (2) Depletion/enhancement mode.
- (3) Normal depletion mode and
- (4) Depletion mode with complete/partial surface inversion.

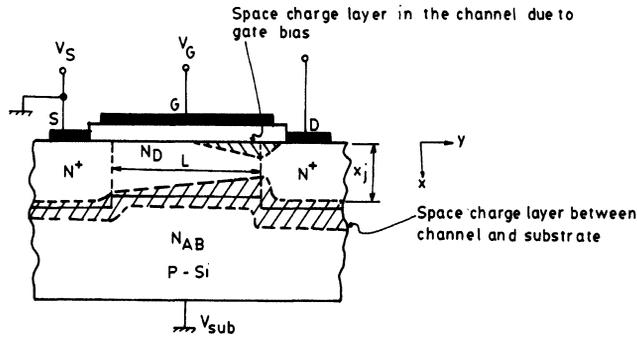


FIGURE 1 Cross-section of a buried N-channel MOS transistor.

OPERATION OF BURIED CHANNEL DEPLETION MOSFETS

In order to describe the different operating modes of a buried-channel depletion-mode MOSFET, the exact profile is approximated by a one step profile with a junction depth “ X_j ” as shown in Fig. 2 such that,

$$N_D = \frac{1}{X_j} \int_0^{X_j} N(x) dx.$$

Complete Enhancement/Accumulation Mode

In this mode, the applied voltage relationship $V_{GS} \geq V_{DS} > 0$ holds good. For large positive values of ‘ V_G ’ in excess of the drain voltage ‘ V_D ’, electrons accumulate near the semiconductor surface over the entire channel length between the source and drain electrodes (Refer Fig. 3(a)).

The local width of the channel is only limited by the depletion region extending around the substrate/channel p-n junction ($X_L \leq X_j \leq X_r$). Due to the accumulation of the carriers on the surface, the channel conductance increases with larger positive values of V_G . The current flowing between the source and drain increases

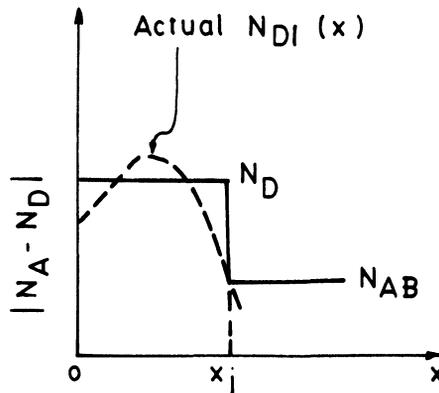


FIGURE 2 Actual profile and one-step approximation.

Buried channel depletion mode MOS transistors

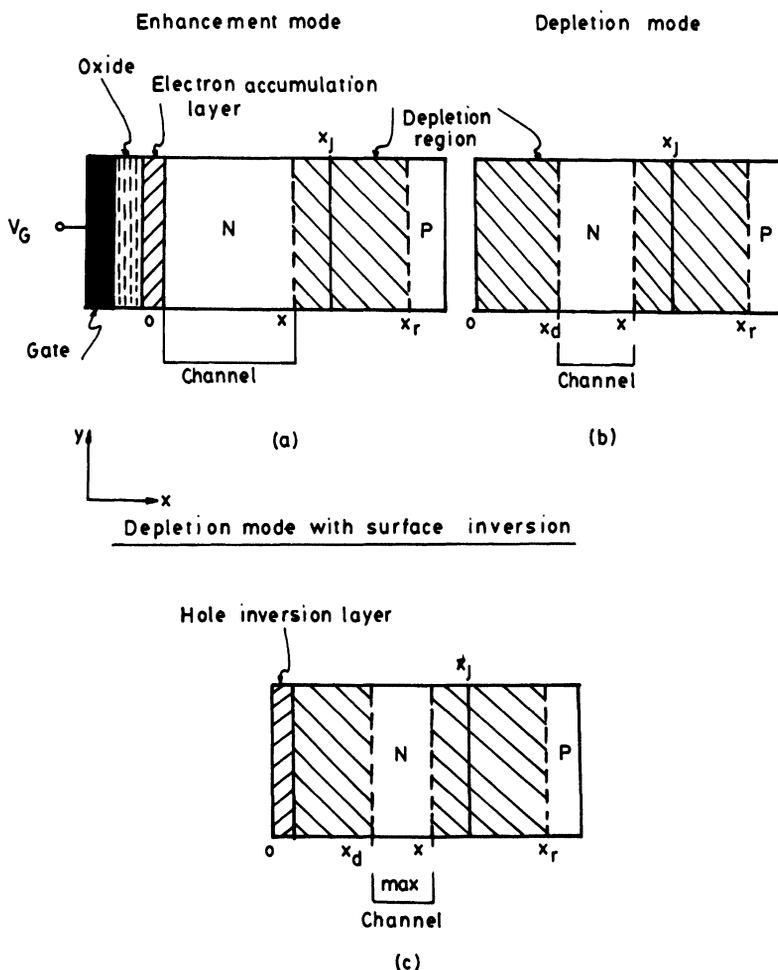


FIGURE 3 Schematic representation of the buried channel structure for the different operation modes.

non-linearly for larger positive values of V_{DS} since the depletion region of the p-n junction becomes larger. A similar effect may result from modifying the substrate polarization. One may expect a lower electron mobility in the surface region than in the buried channel region due to surface scattering.

Depletion/Enhancement Mode

In this mode, ($V_{DS} > V_{GS} > 0$) holds good. For smaller positive values of V_{GS} compared to the previous mode, electron accumulation only occurs between the

source contact ($y = 0$) and some specific point ($y_a < L$) along the channel. The rest of the channel is now depleted. The local width of the buried channel for $y > y_a$ is thus restricted as shown in Fig. 3(b).

Normal Depletion Mode

This mode is valid for the condition $(V_{GS} - V_{FB}) < 0$. Thus, for a negative value of V_{GS} , (more exactly for negative values of $(V_{GS} - V_{FB})$), the surface depletion of the n-region extends over the entire channel length. The width of the buried channel decreases for increasing values of V_{DS} and 'y' due to local potential ' V_y ' along the channel.

Depletion Mode with (Complete/Partial) Surface Inversion

For further increase in negative potential ' V_{GS} ', a partial surface inversion may take place due to the formation of a hole inversion layer between the surfaces of source contact ($y = 0$) and any point ($y_i < L$) along the channel length. The rest of the channel length $y_i < y < L$ is still surface depleted. This is shown in Fig. 3(c).

For still more negative values of ' V_G ', the surface region of the n-surface becomes inverted over the entire channel length and the surface depletion region attains its maximum width. The width of buried channel is no longer a function of the gate potential ' V_G '.

CLASSIFICATION OF BURIED CHANNEL MOSFETS

The depletion-mode buried-channel MOSFETs in general can be placed in to the following two broad categories depending upon the thickness and doping level of the implanted channel.

- Type-A; Complete pinch off devices,
- Type-B; Non-pinch off or deep depletion devices.

Type-A Devices

In these type of devices, the buried channel is shallow implanted and lightly doped. The thickness of the channel (x_j), (Refer Fig 3(a), (b),(c)) is less than the maximum depletion layer width ($X_d \text{ max}$) for inversion at the interface. Assuming the one step profile of the channel, the maximum thickness of the channel for complete pinch off versus the doping for different substrate concentrations are shown in Fig. 4. The allowed pinch-off voltage for various channel doping and substrate bias for various channel thickness and also the limiting thickness of the channel for various substrate doping are shown in Fig. 5, 6. (The parameter calculations are done using depletion approximation and a step junction profile).

These figures are quite informative for selection of required depth, channel implant, and pinch-off voltage for typical depletion-load characteristics.

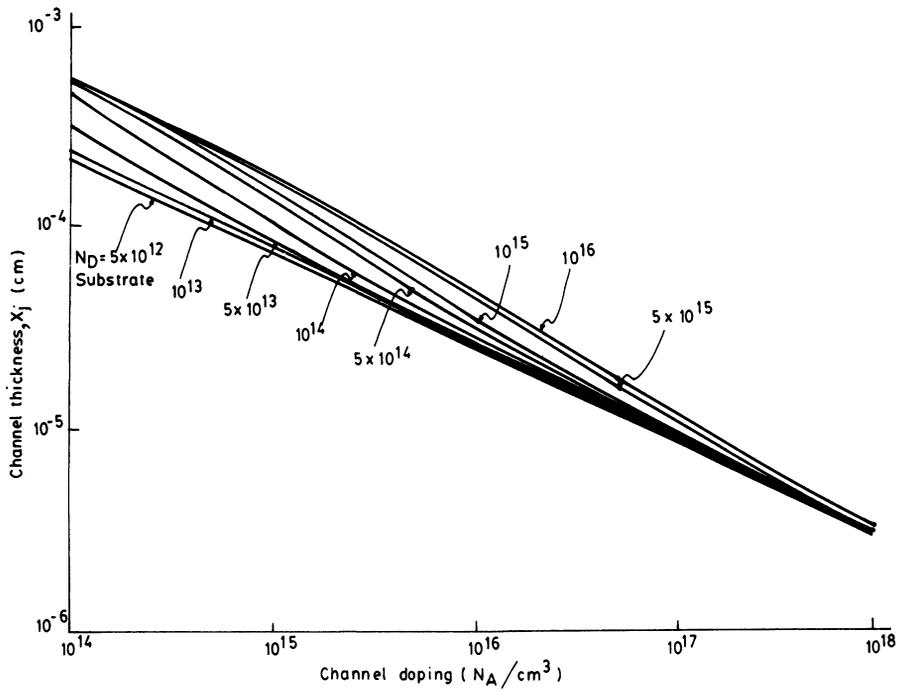


FIGURE 4 Plot of maximum allowed channel thickness vs. channel doping for complete Pinchoff for different substrate dopings.

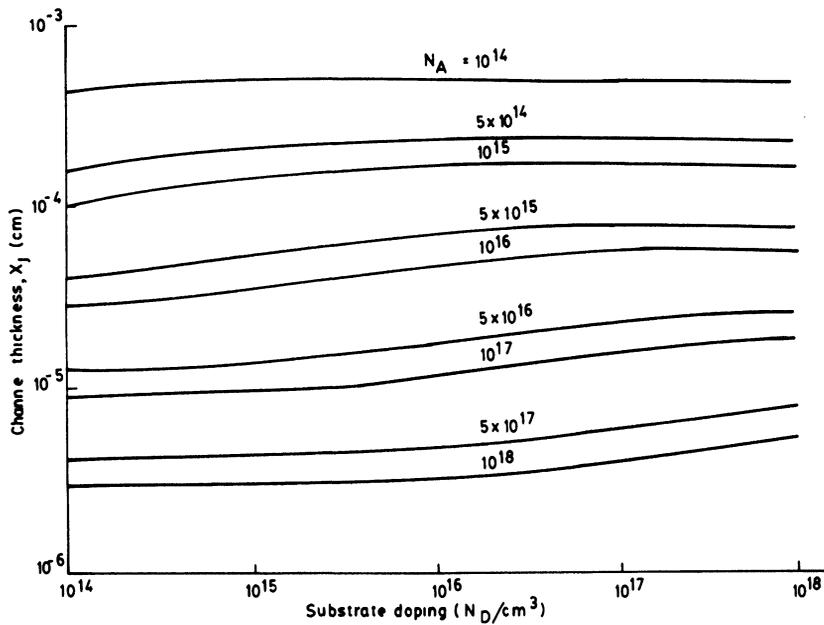


FIGURE 5 Plot of maximum allowed channel thickness vs substrate doping for complete Pinchoff for different channel doping.

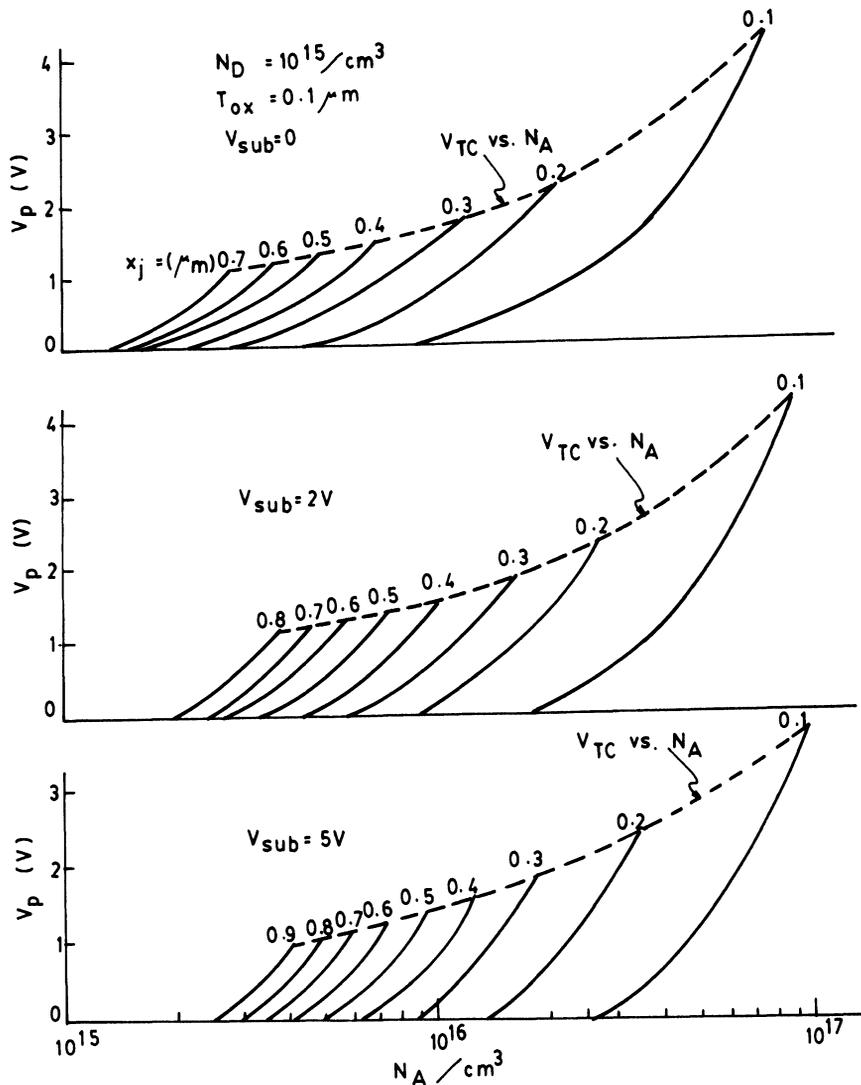


FIGURE 6 Plot of maximum allowed Pinchoff voltage vs. channel doping for different channel thicknesses.

Type-B Devices

These devices are deep implanted and heavily doped such that the thickness of the channel (x_j) is greater than the maximum depletion layer width ($x_d \text{ max}$) (Fig. 3(a), (b), (c)) at the time of inversion at the inversion. This is because of the incomplete pinch off for which the inversion layer is formed at the Si/SiO₂ interface. Inversion layer formed at the interface is floating in nature. Hence, there is very little work done in this aspect and this paper also does not deal with the inversion mode of operation of these devices.

ANALYSIS & MODELLING OF BURIED CHANNEL DEPLETION MOSFETS

In this paper, an analysis has been made for deriving the $I_D \sim V_D$ characteristics for the two types of devices in the selected modes of their operations. To account for the various modes of operation, the basic equations are derived explicitly for the desired conditions. Another important consideration that has been taken into account is the field dependence of the surface mobility irrespective of channel length. The following assumptions are made in the process of analysing the operation of each device in the selected modes.

Assumptions

- The conventional gradual channel approximation is assumed.
- The doping profile of the channel region is assumed to be uniform (box-type).
- The depletion approximation is used to calculate the density of electrons depleted from the channel region.
- All the derivations are based around the grounded source operation for p-channel devices and are equally applicable to n-channel devices with corresponding proper signs.

ANALYSIS OF TYPE-A DEVICES

Fig. 7 shows the charge density and potential drop across the channel in the conduction region of such a device.

Using gradual channel approximations we write for the charge density, which causes conduction in the channel at any point in the x-direction as

$$Q(x) = Q_i + Q_j(x) + Q_D(x) + Q_s(x) \quad (1)$$

Where $Q_i =$ Implanted charge $= q N_A X_j$,

$$Q_j(x) = K_1 [V_{sub} + \phi_B - V(y)]^{1/2}, \quad (2)$$

depletion charge on p-side of the junction.

$$K_1 = (2 \epsilon_s q N_E)^{1/2}$$

$$N_E = N_A N_D / (N_A + N_D)$$

$Q_s(x) =$ surface charge in the Si/SiO₂ interface which depends on the particular mode.

$$\begin{aligned} Q_D(x) &= \text{Surface depletion charge} \\ &= q N_A x_d. \end{aligned}$$

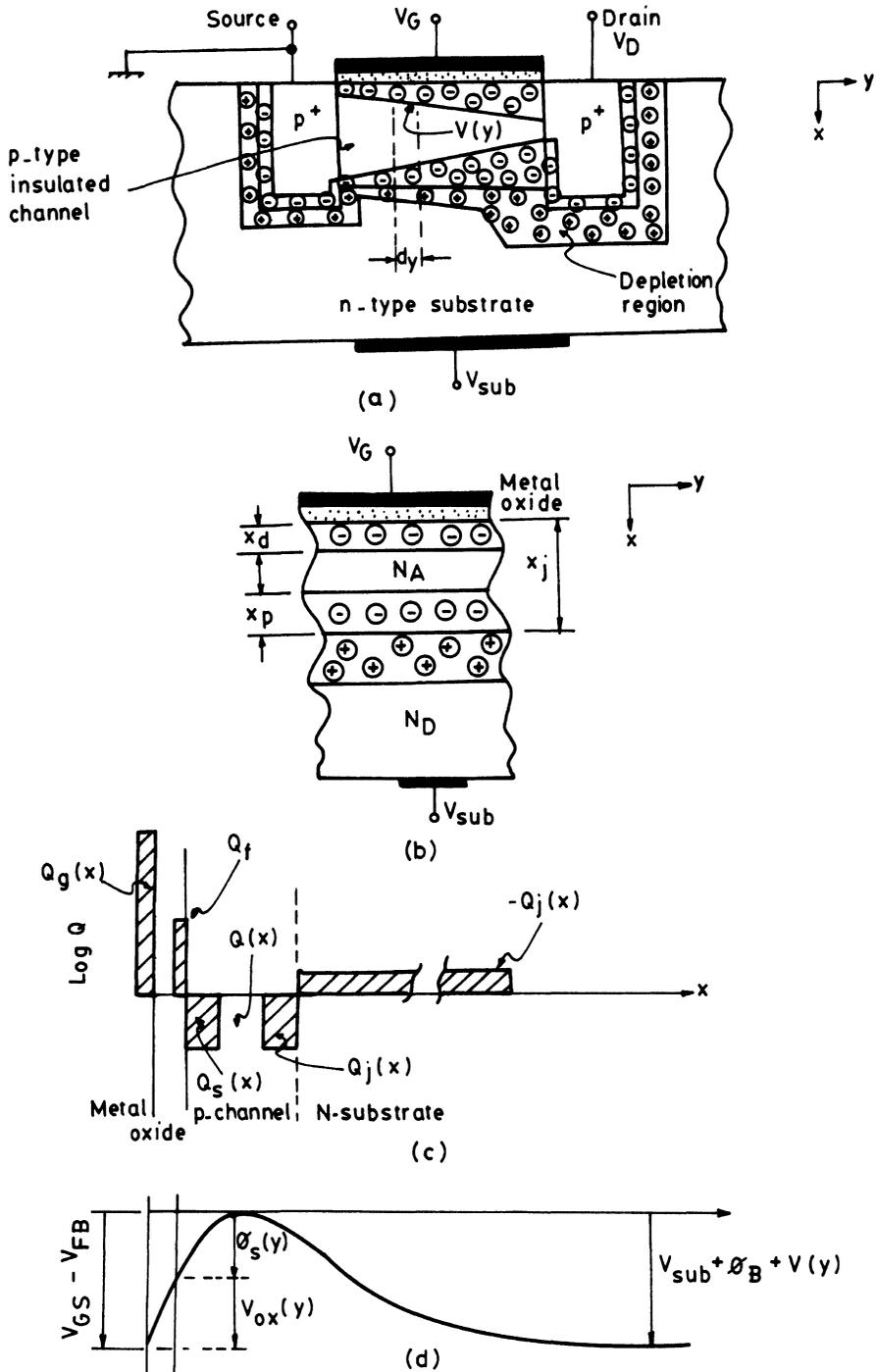


FIGURE 7 (c) Charge density and (d) Potential drop across the channel for BC MOSFET in depletion mode (a) and (b).

The drain current at any point along the y-direction in the channel where the potential $V(y)$ is given by,

$$I_{DS} = + \mu W Q(x) \frac{dV(y)}{dy} \quad (3)$$

Where,

W = Width of the channel,

μ = mobility of carriers.

Equation (3) can be otherwise written as

$$I_{DS} = \frac{\mu W}{L} \int_{V_s}^{V_D} Q(x) dV(y) \quad (4)$$

Type-A Device in Accumulation Mode

For this mode, the surface charge density $Q(x)$ is given by,

$$Q_s(x) = - C_{ox} [V_{GS} - V_{FB} - V(y)] \quad (5)$$

Substitution of this in equation (1) and (4) gives,

$$\begin{aligned} I_{DS} &= \frac{\mu W}{L} \int_0^{V_{DS}} Q(x) dV(y) \\ &= \frac{\mu_b W}{L} \left[Q_i V_{DS} - \frac{2}{3} K_1 \right. \\ &\quad \left. \{ (V_{sub} + \phi_B - V_{DS})^{3/2} - (V_{sub} + \phi_B)^{3/2} \} \right] \\ &\quad + \frac{\bar{\mu}_s W C_{ox}}{L} \left[(V_{GS} - V_{FB}) V_{DS} - \frac{V_{DS}^2}{2} \right] \end{aligned} \quad (6)$$

Where μ_b = bulk mobility,

$\bar{\mu}_s$ - effective surface mobility, depend on gate bias.

The effect of gate field on μ_s is not negligible and the effective mobility is obtained through an averaging procedure. Thus,

$$\bar{\mu}_s = \frac{\mu_{so}}{1 + \theta (V_{GS} - V_{FB} - \frac{V_{DS}}{2})} \quad (7)$$

The value of μ_b can be taken to be fairly constant for a given implant. Using equations (6) and (7), the $I_D \sim V_D$ characteristics for this mode is plotted.

Type-A Device in Accumulation/Depletion Mode

In this mode of operation, the channel is partially accumulated over a distance ' L_1 ' near the source and depleted over a distance ' L_2 ' near the drain such that $(L_1 + L_2) = L$, as shown in Fig. 8.

The $I_D \sim V_D$ characteristic can therefore be modelled as a combination of two devices; one of channel length ' L_1 ' as in the accumulation mode and the other of channel length ' L_2 ' in depletion mode. The surface/channel potential at the transition is given by

$$V_c = V_{GS} - V_{FB} \quad (8)$$

Assuming the charge densities for lengths L_1 and L_2 as

$$Q_s(x) = -C_{ox} [V_{GS} - V_{FB} - V(y)]$$

and

$$Q_D(x) = -q N_A X_d,$$

respectively, we write the equation for current in the two sections as,

$$\begin{aligned} I_{DS} \cdot L_1 &= \mu_b W \left[Q_i V_c - \frac{2}{3} K_1 \{ (V_{sub} + \phi_B - V_c)^{3/2} - (V_{sub} + \phi_B)^{3/2} \} \right] \\ &+ \mu_s C_{ox} W \left[(V_{GS} - V_{FB}) V_c - \frac{V_c^2}{2} \right] \end{aligned} \quad (9)$$

$$\begin{aligned} I_{DS} \cdot L_2 &= V_{DS} \int_{V_c}^{\mu} W [Q_i + Q_j(X) + Q_o - K_2 \{V_{GS} - V_{FB} - V(y) + V_o\}^{1/2}] dv \\ &= \mu_b W [Q_i(V_{DS} - V_c) - \frac{2}{3} K_1 \{ (V_{sub} + \phi_B - V_{DS})^{3/2} - (V_{sub} + \phi_B - V_c)^{3/2} \} \\ &+ Q_o (V_{DS} - V_c) - \frac{2}{3} K_2 \{ (V_{GS} - V_{FB} + V_o - V_{DS})^{3/2} - (V_{GS} - V_{FB} + V_o \\ &- V_c)^{3/2} \}] \end{aligned} \quad (10)$$

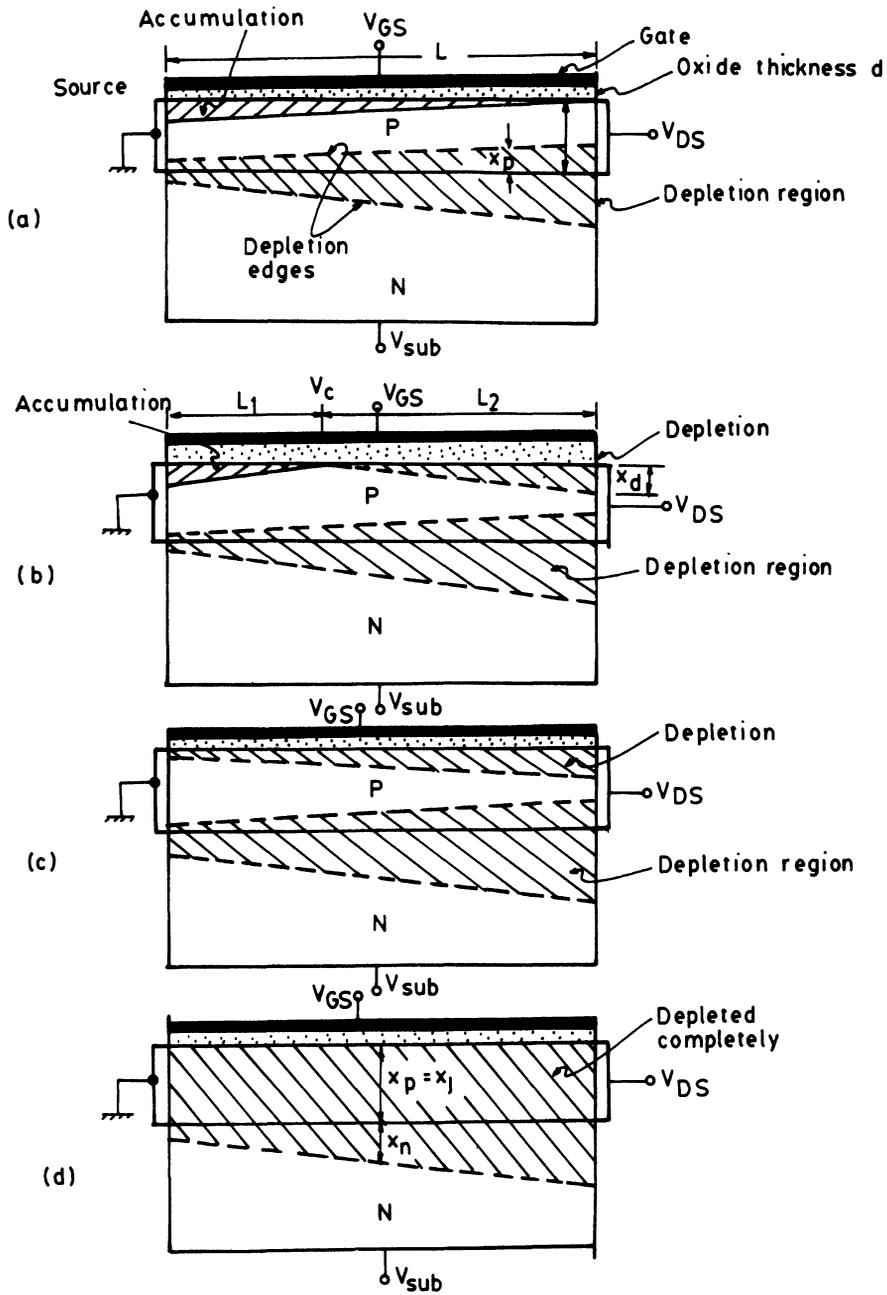


FIGURE 8 Cross-section of a type 'A' BC depletion mode MOSFET in various modes of operation Common nodes (a) Accumulation, (b) Accumulation/Depletion, (c) Depletion, (d) Punch through Accumulation.

Where

$$Q_o = \frac{\epsilon_o q N_A}{C_{ox}}; K_2 = (2\epsilon_s q N_A)^{1/2}, V_o = \frac{Q_o}{2 C_{ox}}$$

Adding equation (9) and (10) we can have

$$\begin{aligned} I_{DS} (L_1 + L_2) &= I_{DS} L \\ &= \mu_b W [Q_i V_{DS} + Q_o \{V_{DS} - (V_{GS} - V_{FB})\} \\ &\quad - \frac{2}{3} K_1 \{(V_{sub} + \phi_B - V_{DS})^{3/2}\} \\ &\quad - \frac{2}{3} K_2 \{(V_{GS} - V_{FB} + V_o - V_{DS})^{3/2} \\ &\quad - (V_{sub} + \phi_B)^{3/2} - V_o^{3/2}\}] \\ &\quad + \bar{\mu}_s W C_{ox} (V_{GS} - V_{FB})^{2/2} \end{aligned} \quad (11)$$

Type-A Devices in Depletion Mode

As the gate voltage is made more positive the complete channel surface region becomes depleted and X_d , which is the surface depletion width together with X_p , which is the depletion width on the channel side of the p-n junction, may become equal to or greater than the channel depth. Thus, for

$$X_j \leq (X_d + X_p),$$

Complete pinch-off is possible and the punch through voltage ' V_T ' is obtained as,

$$\begin{aligned} V_T = V_{FB} + q N_A X_j \left(\frac{1}{2C_j} + \frac{1}{C_{ox}} \right) + \frac{ND}{N_A} + N_D (V_{sub} + \phi_B) \\ - \left(\frac{1}{C_j} + \frac{1}{C_{ox}} \right) K_1 (V_{sub} + \phi_B)^{1/2} \end{aligned} \quad (12)$$

$$\text{Where } C_j = \epsilon_s / X_j$$

Type-B Devices

For these devices, the channel width is large such that $X_j > (X_d + X_p)$. Hence, incomplete pinch-off is observed and ' V_T ' is given by

$$V_T = V_{FB} + \frac{K_2}{C_{ox}} (V_{sub} + \phi_B)^{1/2} + V_{sub} + \phi_B \quad (13)$$

The drain current is obtained as

$$\begin{aligned}
I_{DS} = \frac{\mu_w}{L} \int_{V_D}^{V_i} [Q_i + Q_j(x) + Q_D(x)] dv = \frac{\mu_b W}{L} [(Q_i + Q_o) V_{DS} \\
- \frac{2}{3} K_1 \{(V_{sub} + \phi_B - V_{DS})^{3/2} - (V_{sub} + \phi_B)^{3/2}\} - \frac{2}{3} K_2 \{(V_{GS} - V_{FB} + V_o - V_{DS})^{3/2} \\
- (V_{GS} - V_{FB} + V_o)^{3/2}\}] \quad (14)
\end{aligned}$$

Where

$$Q_D(x) = Q_o - K_2 [V_{GS} - V_{FB} + V_o - V(y)]^{1/2}$$

Equations (6), (11), and (14) give $I_D \sim V_D$ characteristics for the normal modes of operations of both Type-A and Type-B devices usually encountered in applications such as depletion load and RF amplifiers for both P-MOS and N-MOS technologies.

EXTRACTION OF IMPORTANT PARAMETERS FOR THE $I_D \sim V_D$ CHARACTERISTICS

The parameters considered important for the characterization of these devices are

- The flat band voltage, V_{FB} ,
- The average channel doping, N_A ,
- The average channel thickness, X_j ,
- The effective surface mobility of the carriers, $\bar{\mu}_s$ and
- The bulk mobility of carriers, μ_b .

These parameters are usually extracted from the $I \sim V$ measurements of the device around the operating region. Though various methods, viz,

Huang and Taylor's Method,
Haken's Method,
Donald's Method,
White's method

are available, none of them are suitable for online extraction because they require more than one set of measurements for extraction of parameters and also that these methods do not account for the variation of surface mobility with gate field.

The method described here is an accurate and simple method for online extraction purpose. In this method, various parameters are extracted from a single set of $g_{DS} \sim V_{sub}$ plots as shown in Fig. 9.

Since for very low V_{DS} the value of g_{DS} is almost proportional to I_{DS} , the plot is almost the same as $I_{DS} \sim V_{DS}$ plot and hence it can be considered as a D.C. characteristic. In the plot, the three different plots are shown very distinctly. This

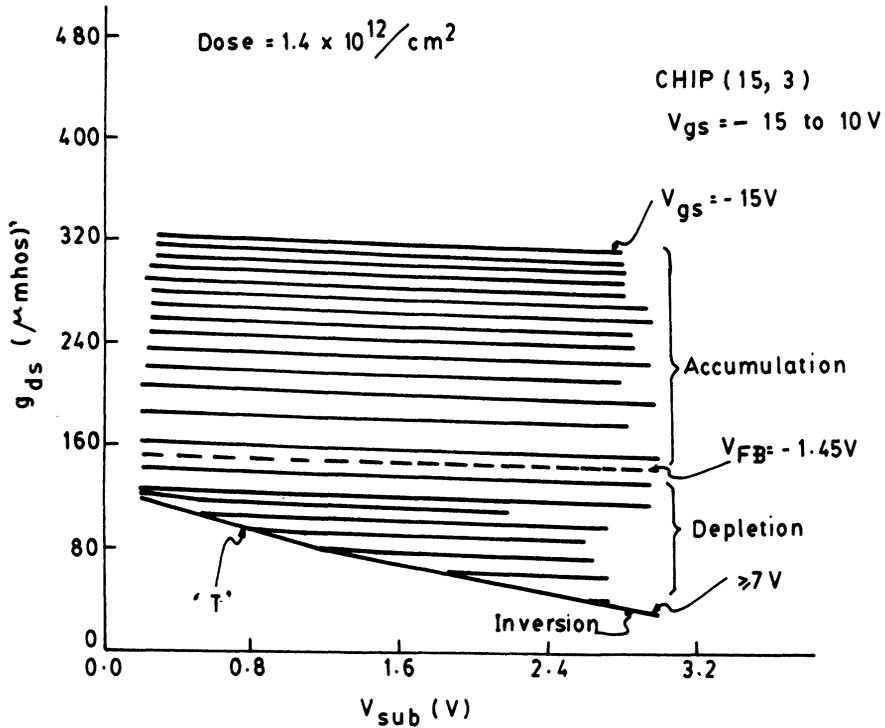


FIGURE 9 Typical $g_{ds} - V_{sub}$ plots of buried channel MOSFET exhibiting various modes $V_{ds} = 0$ (plotted by the data acquisition system).

procedure is fast enough to be coupled to an online Data Acquisition system as it does not require any change in circuit configuration during measurements.

EXTRACTION OF V_{FB}

$$V_{GS} - V_{SI} = V_{FB} + \frac{K_2}{C_{OX}} (V_{SI} + \phi_B)^{1/2} + \phi_B \quad (15)$$

From this equation, a plot of $(V_{GS} - V_{SI}) \sim (V_{SI} + \phi_B)^{1/2}$ is obtained, the intercept of which on the $(V_{GS} - V_{SI})$ axis gives $(V_{FB} + \phi_B)$. Assuming some value for ϕ_B (0.6V), V_{FB} can be calculated. This method has the advantage that the identification of the transition points (T) is more precise than in Haken's method.

EXTRACTION OF N_A, X_j

The value of implanted dose ϕ_{eff} is obtained from $\phi_{eff} = N_A X_j = \frac{Q_i}{q}$

$$= \frac{\mu_{so}}{\mu_b} \times \frac{F(V_T - V_{FB})}{q} \times C_{ox} \quad (16)$$

In order to calculate the value of N_A , inversion and accumulation modes are used together by switching the device. Then the plot of $g_{ds} \sim (V_{sub} + \phi_B)^{1/2}$ is obtained for both modes separately. Then N_A is obtained from the relation,

$$N_A = (\gamma - 1)^2 N_D \quad (17)$$

Where

$$\gamma = \frac{\text{Slope of } g_{ds} \sim (V_{sub} + \phi_B)^{1/2} \text{ in inversion mode}}{\text{Slope of } g_{ds} \sim (V_{sub} + \phi_B)^{1/2} \text{ in accumulation mode}}$$

Substitution of value of N_A in equation (16) gives X_j .

EXTRACTION OF M_B AND M_S :

From the accumulation mode of operation, the drain conductance g_{ds} at $V_{DS} = 0$ can be derived as

$$g_{ds} = \left. \frac{\partial I_{DS}}{\partial V_{DS}} \right|_{V_{DS} = 0} \quad (18)$$

When plotted for $g_{ds} \sim (V_{sub} + \phi_B)^{1/2}$ this equation gives the slope as,

$$\text{Slope}_1 = - \frac{\mu_b W}{L} K_1 \quad (19)$$

Where $K_1 = (2\epsilon_s q N_D)^{1/2}$

From equation (19), the value of μ_b can be calculated for a known slope₁. μ_{so} can be obtained from the intercepts of the $g_{ds} \sim (V_{sub} + \phi_B)^{1/2}$ plot on the g_{ds} axis. This gives

$$\beta_o = \frac{\mu_{so} W}{L} C_{ox} \quad (20)$$

From eqn. (20), the value of μ_{so} can be obtained.

MEASUREMENT SET UP

To compute the best values of the plots as discussed above, an averaging procedure is used by choosing many gate voltages for a wide range of substrate biases. The measurements are done from the g_{ds} and g_m plots using lock-in amplifier techniques. Fig. 10 shows the measurement setup used for extraction of parameters on an online basis. An HP-9825 A computer controls the measurement process

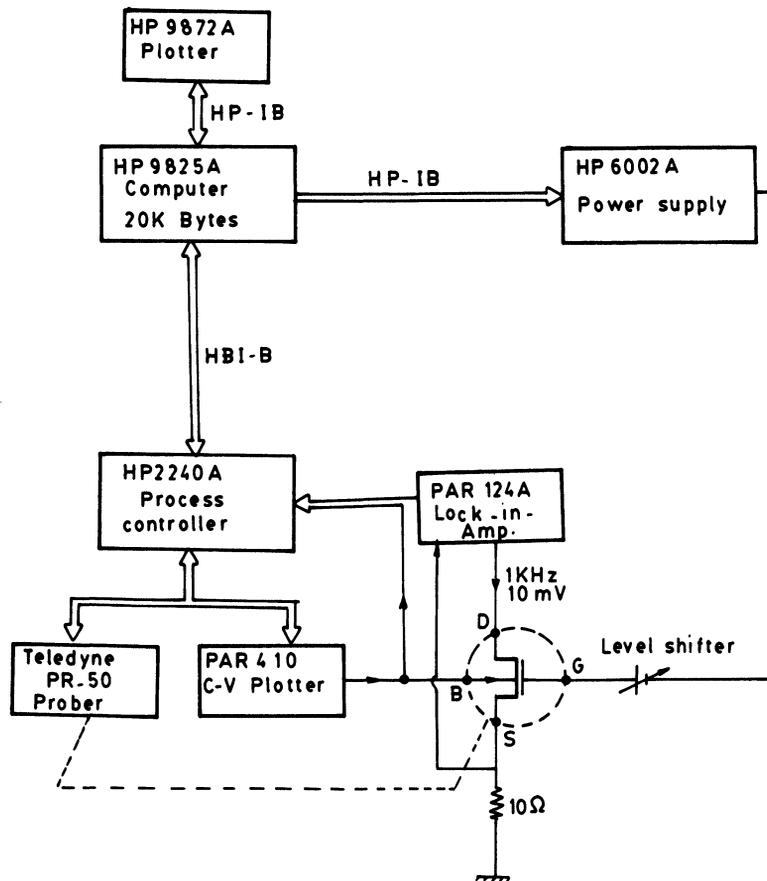


FIGURE 10 Proposed data acquisition system for fast On-line parameter measurements.

controller (HP 2240 A). The process controller measures g_{ds} and V_{sub} by triggering a ramp generator. The gate voltage is changed by a programmable power supply (e.g., HP 6002 A) after every ramp. The output of the lock-in amplifier and that of the ramp appearing at the substrate are fed to the process controller. Once the measurement is complete on one device, the prober is automatically stepped up by the computer through the HP 2240 A.

CONCLUSION

A detailed analysis has been offered about the type, mode of operation, measurement set up and, parameter extraction principles for the buried-channel depletion-mode MOSFETs. Their use as the load transistor to replace the conventional enhancement-mode MOSFET in an inverter for obtaining improved performance with added features like larger power handling ability, faster response, smaller die area, low power loss, etc., are noteworthy.

Basic equations for drain current have been deduced for every mode of operation. A simple averaging procedure for deriving surface mobility of carriers from the considerations of gate field effect on long channel devices is incorporated.

Finally, a very comprehensive study has been made of various parameters to be extracted and a compact, simple, fast acting, and on-line extraction method has been proposed.

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