

## ANALYSIS OF HOT-CARRIER DEGRADATION IN SMALL AND LARGE $W/L$ $n$ -CHANNEL TRANSISTORS

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Device degradation due to hot-carrier in  $n$ -channel HEXFETs is shown to be related to the device geometrical structure. The form of  $I-V$  characteristics of the body-drain junction is found dependent of the hot-carrier stressing and of the layer dimensions. A large increases of the ideality factor, of the reverse recombination current, and of the series resistance are shown to be more significant for small values of  $L$  and  $W$ . It is demonstrated that the degradation of parameters is mainly caused by the generation of interface traps.

*Keywords:* Hot-carrier degradation; MOSFET; gate geometry

### INTRODUCTION

With the reduction of gate sizes to micrometer and submicrometer dimensions in recent years, the problem of the quality of the gate oxide and its interface with the silicon has once again become of concern in the fabrication of MOS devices. This is due to what is called the hot-carrier effect [1, 2]. The hot-carrier effect results from the high fields in the drain region of the transistor due to applied voltages and leads to a degradation in the transconductance (and/or a shift in the threshold voltage) and a decrease in the post-threshold drain current. Published

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works [3–5] have discussed this degradation in terms of interface-states and/or of oxide trapping sites. They are based on the presence of very high field in micronic MOS structures which increase carrier injection into the thermally grown silicon dioxide layer ( $\text{SiO}_2$ ) used as gate insulator.

This study shows that other parameters might be of importance to qualify commercial microelectronic devices for use in space applications. These are the junction body-drain parameters which are shown to be monitors of hot-carrier degradation.

The aim of this work is to show modifications of the electrical properties of the devices stressed for 4 hours at  $V_G = V_D/2$ , which are enhanced by the decrease of its sizes. The hot-carrier stressing dependent large increases of the electrical parameters of the body-drain junction of HEXFET are obtained and found to be related to the layer dimensions.

## METHOD

This study has been performed with  $n$ -channel Hexagonal field effect transistors (HEXFET, IRF 530) before and after stress at  $V_G = V_D/2 = 3,5$  volts. This stress are related to transistors with a gate geometry:  $W/L = 1.4/0.5, 10/0.5, 1.4/6$ .

Static current-voltage measurements were obtained from the gate-controlled HEXFETS integral “body-drain” diode. A schematic representation of the experimental set up is shown in Figure 1 for  $n$ -channel MOSFETS with positive threshold voltage. Current and voltage values are computer driven and stored for further analysis. This body-drain junction is a conventional p-n junction device. It is a feature of the HEXFET (actually, of all power MOSFETS) and the full electrical symbol for the power MOSFET includes the reverse parallel rectifier shown in Figure 1 between source an drain. It can be put into use as a circuit component, providing, for example, the “freewheeling” and “flyback” functions for the “motoring” and “regenerating” modes in a motor speed control circuit [6].

The HEXFET design (Fig. 2) is based upon vertical D-MOS technology. The closed hexagonal cellular structure with the buried silicon gate allows for optimum utilization of silicon. When a positive

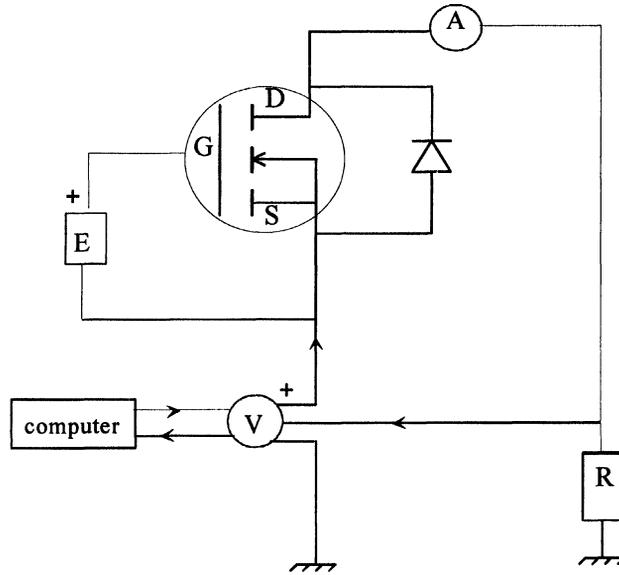


FIGURE 1 Experimental set-up for static measurements of the forward  $I-V$  characteristic of the body-drain diode of a  $n$  channel HEXFET. The gate voltage is used to control the body-drain diodes through reduction of the effective diode area.

voltage is applied on the gate, the source being connected to the ground, an electric field is set up within the HEXFET. This field modulates the resistance between the drain and source terminals, and allows a current to flow in or out of the drain in response to the applied drain circuit voltage. For a direct biased transistor, the body-drain diode is reverse biased and the thermally dependent saturation current flows through it. The main transistor current flows from the drain region vertically through the body of the device, then horizontally through the channel region, and vertically out through the source. This current is made up by electrons and minority carriers, running the other way.

In our experiment the transistor is reversed biased and the body-drain diode is forward biased, *i.e.*, the source terminal is made positive with respect to the drain so the diode is forward biased. Due to the HEXFET design, the current can flow through the source cell, across the forward biased p-n junction (Fig. 2a). Conduction of the body-drain diode results in minority carrier injection into the drain region of

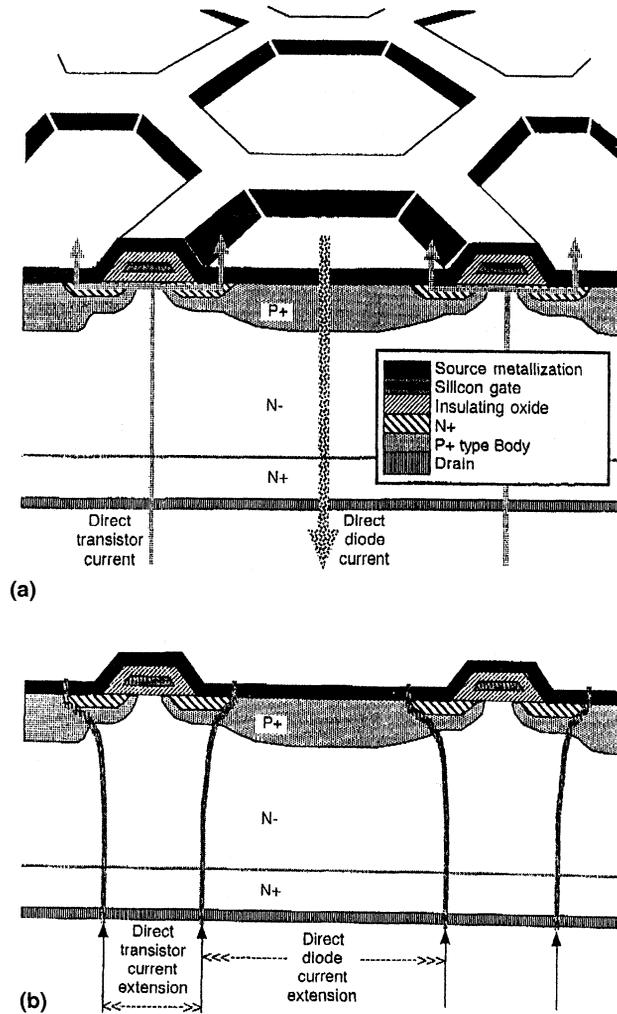


FIGURE 2 Top and cross-section views of a HEXFET power MOSFET (not to scale) showing (a) direct biased transistor current main path. The direct biased diode current flows as shown for a negatively biased drain and null gate voltage. Current lines extend (b) more or less accordingly to bias values.

the MOSFET. The voltage-gate controlled transistor current also flows from source to drain, is made up by electrons as minority carriers, along the same channel path. The reverse transistor current is the counterpart of the direct transistor current. Current lines can

extend around these main lines, more or less, according to the bias values as shown schematically in Figure 2b.

Mathematical models for diodes based on the principles of solid-state physics are reasonably well developed. The  $I-V$  characteristics of silicon p-n junctions can be described by implicit equations [7]:

$$I = \frac{V + R_s I}{R_{sh}} + I_{od} [e^{(q/kT)(V+R_s I)} - 1] + I_{or} [e^{(q/nkT)(V+R_s I)} - 1]$$

The model introduce the classical parameters, series ( $R_s$ ) and shunt ( $R_{sh}$ ) resistances, and ideality factor ( $n$ ). It separate electronic diffusion phenomena in the quasi-neutral regions of the junction (reverse current  $I_{od}$ ) from the surface and space-charge region recombination current (reverse current  $I_{or}$ ). This practice is acknowledged for through its implantation in the SPICE model of the diode. A specifically conceived software [8], extracts the values  $I_{od}$ ,  $I_{or}$ ,  $n$ ,  $R_s$  and  $R_{sh}$  from the experimental  $I-V$  diode measurements. This procedure has been used [9] to study radiation induced defects in field effect transistors.

Using the classical method with normally operating transistor and keeping the HEXFET in saturation, the threshold voltage is obtained from the intercept of the extrapolated square-root drain-current to gate-voltage curve with the voltage axis. The oxide trapped charge ( $\Delta N_{ox}$ ) and the interface trapped charge ( $\Delta N_{ss}$ ), were determined using the subthreshold charge separation technique of McWhorter and Winokur [10].

## RESULTS AND DISCUSSION

Figure 3 shows the characteristics ( $I-V$ ) of the body-drain junction for transistors stressed at  $V_G = V_D/2 = 3.5$  volts during 4 hours, with different structures where the  $W/L$  is indicated. These curves do not deduce of each other by a simple translation, what shows a modification of the junction to the reduction of sizes and to the hot-carrier stressing. For small values of  $W$  ( $1.4 \mu\text{m}$ ) and  $L$  ( $0.5 \mu\text{m}$ ) the modification of characteristics ( $I-V$ ) after stress is much significant that for larger values of  $W$  ( $10 \mu\text{m}$ ) and  $L$  ( $6 \mu\text{m}$ ). Same modification is observed with the extracted physical parameters ( $n$ ,  $I_{or}$ ,  $R_s$ ) with our software [8] from the experimental ( $I-V$ ) diode measurements.

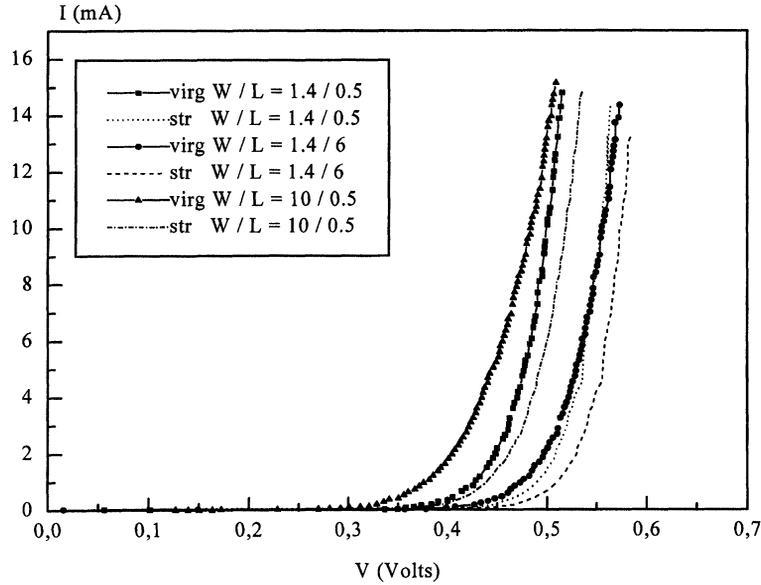
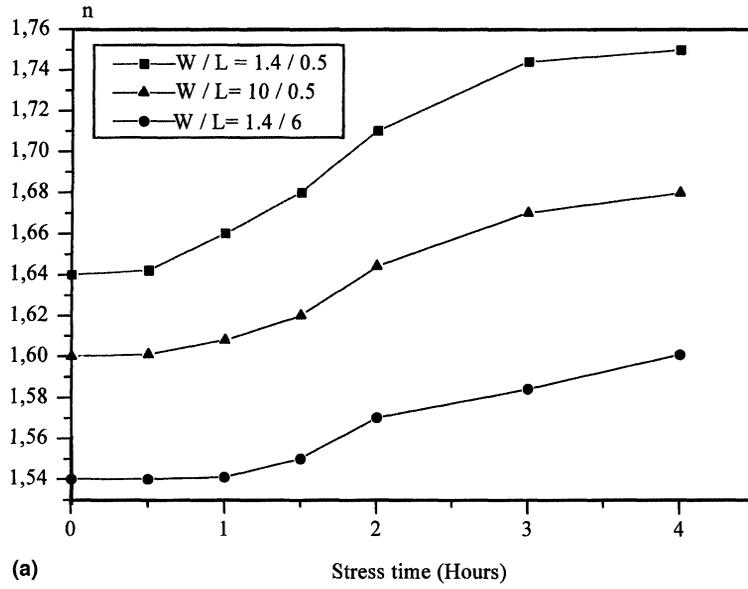


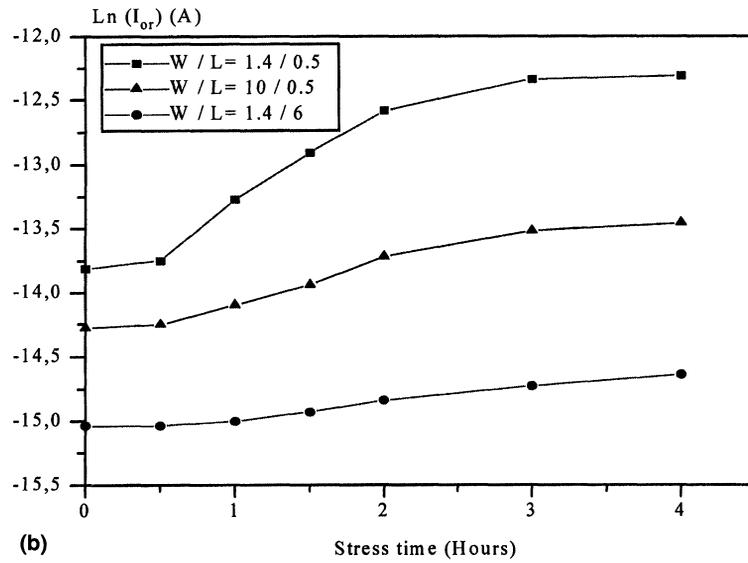
FIGURE 3  $I-V$  Characteristics of the body-drain junction for different gate lengths ( $L$ ) and widths ( $W$ ), during stress at  $V_G = V_D/2$ .

Figure 4 (a,b,c) points out an increase of the parameters ( $n$ ,  $I_{or}$ ,  $R_s$ ) of the stressed device compared to the virgin device that reflects the hot-carrier damage in the transient region of the junction at the oxide semiconductor interface near the junction. The hot carrier effects in MOS devices are due to high lateral electric field  $E_m$  in saturation regime. The maximum lateral electric field is given by:  $E_m = (V_d - V_{dsat})/l$  [11] where  $l$  is the length of the velocity-saturation region and  $V_{dsat}$  is the saturation voltage.  $V_{dsat}$  is a function of the device length  $L$  and of the transverse electric field [12]. Thus, as device length  $L$  shrink contribute to increasing  $E_m$  and consequently the hot-carrier damage became more significant.

Figure 4 clearly demonstrates that the physical parameters ( $n$ ,  $I_{or}$ ,  $R_s$ ) increases when the gate length  $L$  decreases from  $6\ \mu\text{m}$  to  $0.5\ \mu\text{m}$ . A comparative lower influence of  $W$  values is again observed. This fact is intuitive since the length of the channel is related to the modification of the depleted part of the body-drain junction and since  $W$  affects the spatial extension of the junction. This increase of the ideality factor



(a)



(b)

FIGURE 4 The body-drain junction ideality factor (a) reverse recombination current (b) and series resistance (c) for different gate lengths ( $L$ ) and widths ( $W$ ), during stress at  $V_G = V_D/2$ .

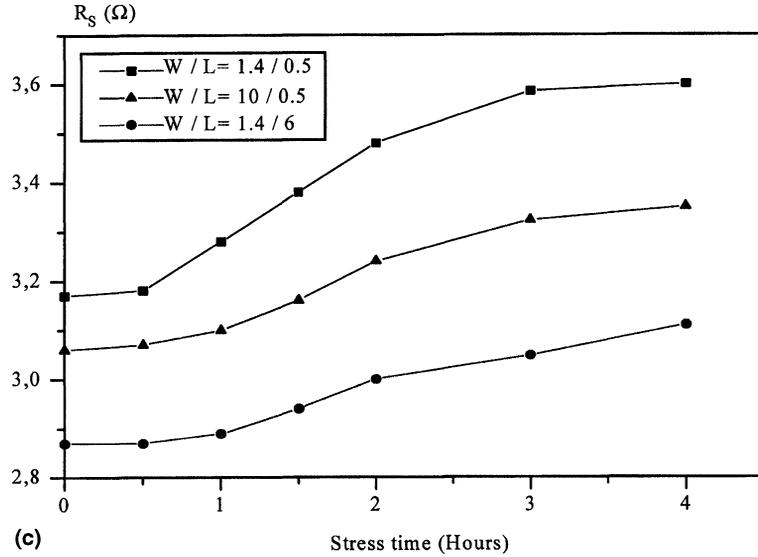


FIGURE 4 (Continued).

(Fig. 4a) reflects an increase of carrier recombination in the diode space charge region and the oxide-semiconductor interface [9]. For very small surfaces, the technological doping process leads to less uniform levels than for larger surfaces, and the edge effects, which are related to high default (broken bonds) concentrations, are more sensitive for the former than for the latter. These effects lead to a high contribution of the recombination current to the reverse diode current. This is confirmed by an increase of  $I_{or}$  reverse current. The electrical field has an influence on recombination process since high electrical field values in the oxide layer make the oxide traps move and exchange charges with the silicon.

During stress, the increase of ( $n$ ,  $I_{or}$ ,  $R_s$ ) is consistent with the carrier mobility reduction [13] and may be related to the increase of induced trapped charge density (Fig. 5). In Figures 4 and 5, it has been seen that the variation of the parameters ( $n$ ,  $I_{or}$ ,  $R_s$ ) is mainly due to an increase of interface traps ( $\Delta N_{ss}$ ).

As clearly shown on Figure 5, there is a modest increase in the number of oxide trapped charge ( $\Delta N_{ox}$ ) during stress. These results shows that the parameters as well as the trapped ( $\Delta N_{ss}$ ) increase with

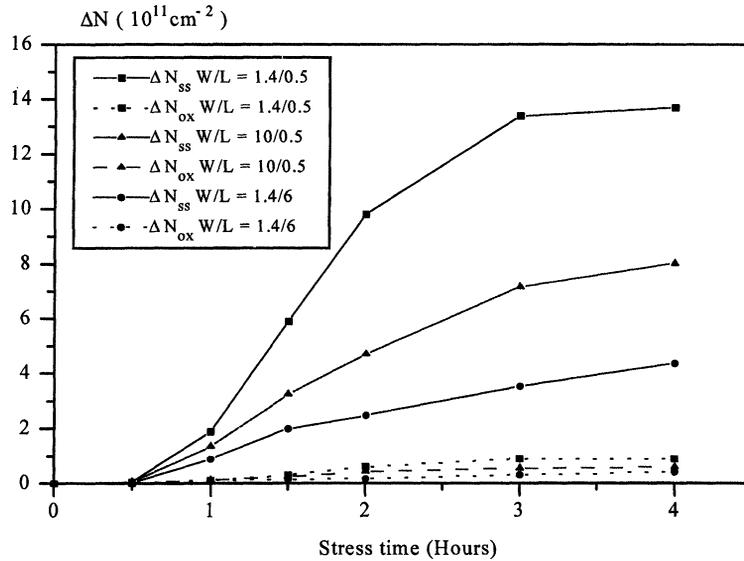


FIGURE 5 Density of oxide trapped charge ( $\Delta N_{ox}$ ) and interface trapped charge ( $\Delta N_{ss}$ ) for different gate lengths ( $L$ ) and widths ( $W$ ), during stress at  $V_G = V_D/2$ .

time during stress, and this increase is significant for small values of  $W$  and  $L$ . A saturation effect of parameters and densities is observed after a time of 3 hours for  $W/L = 1.4/0.5$ , however for  $W/L = 1.4/6$  and  $10/0.5$  the values of  $n$ ,  $I_{or}$ ,  $R_s$  and  $\Delta N_{ss}$  continues always to increase. This result confirms again that the degradation of physical parameters transistors caused by the hot-carrier depends on the two geometrical parameters ( $W$ ,  $L$ ).

### CONCLUSION

An experimental method for studies of HEXFETs junction has been described. The effect, on the body-drain junction parameters, of a decrease of both the channel length and the channel width for micronic devices, has been pointed out. It is shown that, stress time results in large increase of ( $n$ ,  $I_{or}$ ,  $R_s$ ) and the hot-carrier damage is significant for small values of  $W$  and  $L$ . It has been demonstrated that the degradation of physical parameters is mainly due to an increase of trapped interface charges density.

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