A SIMPLIFIED SPICE MODEL FOR IGBT

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A simplified IGBT (Insulated Gate Bipolar Transistor) SPICE macromodel, based on its equivalent circuit, is proposed. This macromodel is provided to simulate various mechanisms governing the behavior of the IGBT, and it takes into account specific phenomena limiting its SOA (Safe Operating Area), such as forward and reverse biased SOA, as well as latch-up. The validity of this model is confirmed by comparison between simulation and experimental results as well as the data sheets. This comparison is tested for two IGBT devices showing two different powers and switching speeds, and a good agreement is recorded for both IGBT devices.

Keywords: Insulated gate bipolar transistor; simulation; spice

I. INTRODUCTION

The Insulated Gate Bipolar Transistor (IGBT) was added to the family of power devices to overcome the high on-state loss of power MOSFETs. The IGBT is an hybrid device that combines the advantages of a MOSFET (high switching speed and low power drive requirement) and of a bipolar junction transistor (BJT) (low conduction losses) [1].

The combined top perspective and cross-sectional views, not to scale, of one from the thousands of cells the IGBT comprises are shown in Figure 1. Its structure is similar to that of a Vertical Double diffused MOSFET (VDMOSFET) with the exception that a p-type,

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heavily doped substrate, replaces the n-type drain contact of the conventional VDMOSFET.

Analytical models exist already [2]. Their implementation sets many problems due to the complexity of the equations used for calculating the current and charges of the IGBT. Some authors [3] proposed simplified equations, but the simulation results show inaccurate results near limit or non standard operating conditions. Another solution is to translate the physical equations into electrical circuits with original solutions to replace the derivative functions and other operators [4–7], but this solution requires a specific SPICE version like IG-SPICE (Interactive Graphics SPICE).

In this work we present another approach which consists in defining the IGBT as a simple macromodel based on its equivalent circuit. The validity of this model is confirmed by comparison between simulation and experimental results as well as the manufacturer's data. Two IGBT devices from International Rectifier, IRGBC20S and IRGBC40F, showing different powers and switching speeds, are modelled and tested.
II. CIRCUIT MODEL

The complete macromodel of IGBT that we suggest is given in Figure 2. The core of this macromodel is the IGBT equivalent circuit marked with bold typeface, i.e., a p–n–p bipolar transistor driven by a n-channel MOSFET in a pseudo-Darlington configuration [8]. This core has been completed with some components to help simulate various mechanisms governing the behavior of the IGBT, such as forward and reverse biased SOA, latch-up, switching parameters, etc.

II.1. DC Model of IGBT

The transfer characteristics of an IGBT and a power MOSFET are similar apart from a shift due to the built-in potential of the base-emitter junction of the p–n–p bipolar transistor. Indeed, the IGBT current is equal to the MOSFET one multiplied by the current gain of the p–n–p bipolar transistor. Therefore, several static parameters of the IGBT depend on the SPICE parameters of the MOSFET.

In our study, the SPICE models used for the BJT and the MOSFET are the Gummel Poon and the Shishman Hodges models respectively.

FIGURE 2 Macromodel, based on the equivalent circuit of the IGBT, used for modelization.
The SPICE parameters which provide for adjustment of saturation current, conductivity, and static saturation voltage of the IGBT are: \( K_p \) (Transconductance coefficient), \( W \) and \( L \) (channel width and length respectively), \( \text{GAMMA} \) (bulk threshold parameter), \( \text{PHI} \) (surface potential), and \( \text{LAMBDA} \) (channel-length modulation) for the MOSFET element, and the current gain for the BJT.

II.2. Dynamic Model of IGBT

After calibration of the static parameters, one can proceed with the dynamic model. Two branches, with components names indicated GD and DG in the sub-circuit, between the gate and drain of the MOSFET, are used to simulate the dynamic parameters [9]. Typical dynamic parameters, used to characterize the IGBT, are the switching characteristics times: rise time \((t_r)\), fall time \((t_f)\), turn-on delay time \((t_{don})\), turn-off delay time \((t_{doff})\), turn-on time \((t_{on})\), and turn-off time \((t_{off})\), with:

\[
t_{on} = t_r + t_{don} \quad \text{and} \quad t_{off} = t_f + t_{doff}.
\]

Fall Time Calibration

The biggest limitation to the turn-off speed of an IGBT is the lifetime of the minority carriers in the \( n^- \) epi. layer, i.e., the base of the \( p-n-p \) bipolar transistor. The charges stored in the base produce a characteristic “tail” in the current waveform of an IGBT at turn-off. When the MOSFET’s channel turns off, electron current decreases and the IGBT current drops rapidly to the level of the hole recombination current at the inception of the tail. Since the base current of the \( p-n-p \) bipolar transistor corresponds to the MOSFET drain current, the current gain of the \( p-n-p \) transistor is then, given by [1]:

\[
\beta(Q1) = \frac{I_c}{I_{MOS}}.
\]

This current gain, \( BF \) parameter in SPICE, allows to adjust the abrupt fall amplitude and implicitly the fall time value, this can be also adjusted directly by the ideal forward transit time of the parasitic \( n-p-n \) transistor (parameter \( TF \) in SPICE).
**Turn-off Delay Time Calibration**

Because of the particular structure of the IGBT where the gate metalization covers a big part of the MOSFET’s drain ($n^-$ layer), the gate-drain capacitance $C_{GD}$ is the main cause of the turn-off delay time [10]. In addition, $C_{GD}$ is the capacitance of a MOS structure, its value is function of the gate voltage. This capacitance is the equivalent capacitance of the oxide capacitance $C_{ox}$ and of the depletion drain capacitance $C_{GDd}$. The equivalent sub-circuit used here is a fixed capacitance $C_{GD\text{max}}$ representing $C_{ox}$ and a diode $D_{DG}$ used because the diode transit capacitance has the same behavior as $C_{GDd}$. Two MOSFET transistors, $M_{GD}$ and $M_{DG}$, controlled respectively by gate-drain voltage $E_{GD}$ and $E_{DG}$ can switch alternatively to $C_{GD\text{max}}$ or $C_{GDd}$. The SPICE parameters of $M_{GD}$ and $M_{DG}$ are chosen to be that of an ideal MOSFETs in order not to disturb the sub-circuit working. Therefore, the turn-off delay time, $t_{\text{doff}}$, can be adjusted by the value of $C_{GD\text{max}}$ and the SPICE parameters of the diode $D_{DG}$.

**Turn-on Delay Time Calibration**

The turn-on delay time fitting can be obtained by adjusting the SPICE parameters of the MOSFET. These parameters are the capacitances $C_{GBO}$ (gate-bulk overlap capacitance per channel length) and $C_{GSO}$ (gate-source overlap capacitance per channel width). The turn-on delay time $t_{\text{don}}$ increases as these capacitance values increase.

**Rise Time Calibration**

Parameters of the sub-circuit allowing to adjust the rise time are, mainly, $K_p$ (transconductance coefficient) and $I_s$ (bulk p–n saturation current). Since $K_p$ is used to regulate the static characteristics, we use especially $I_s$ to regulate $t_r$.

**II.3. Parameters Limiting the SOA**

Safe Operating Area (SOA) is very important in power electronics. Its determination allows one to know the limits of the normal device operating condition. In the IGBT case, the most interesting
parameters, limiting the SOA, are the forward and reverse biased SOA voltages and latch-up current.

**Forward Biased SOA**

The breakdown voltage is not forecasted by the bipolar transistor model included in standard SPICE library. This is why an appropriate breakdown voltage value is chosen for the $D_{DS}$ diode to model this behavior. This additional diode is connected between the MOSFET’s drain and source. When the anode bias voltage is positive (i.e., $V_{AK} \geq 0$) and the MOSFET’s n-channel turns off (when $V_{GK} \leq 0$), the p–n–p bipolar transistor is not conducting. The anode voltage is, therefore, given as:

$$V_{AK} = V_{EB}(Q1) + V_{D_{DS}},$$

where $V_{EB}(Q1) \approx 0.7$ V.

By using the SPICE parameter BV (reverse Breakdown Voltage of the diode $D_{DS}$), the equation can be rewritten as:

$$BV = V_{BV} - 0.7 (V).$$

$V_{BV}$ is the forward biased SOA voltage value of the IGBT. So this value is fixed by adjusting the BV parameter.

**Reverse Biased SOA**

This phenomenon is represented by the $D_{EC}$ and $D_{DS}$ diodes conduction states for some negative values of anode bias voltage $V_{AK}$. $V_{AK} = V_{EB} + V_{BC} - V_{EC}$. In operating conditions such as: $V_{EB} \leq -0.7$ V and $V_{BC} \leq -0.7$ V, the negative current is the current flowing from the cathode through both diodes and the supply voltage $V_{EC}$ to the anode of the IGBT when: $V_{AK} \leq -1.4 - V_{EC}(V)$. The reverse biased SOA voltage of the IGBT is, therefore, adjusted by the supply voltage $V_{EC}$ value. This value will be determinated as function of the IGBT’s reverse biased SOA voltage measured or given in the data sheets.

**Static Latch-up Modelling**

When an IGBT goes into latch-up, the parasitic n–p–n transistor of the device starts to conduct. This behavior can be modelled by
introducing a n–p–n bipolar transistor between the MOSFET's drain and source, which is controlled by the series resistance $R_p$ of the p-well. Latch-up occurs when the voltage drop over this resistor is large enough to turn on the parasitic n–p–n transistor, i.e., when:

$$R_p \times I_c(Q1) > V_{EB}(Q2).$$

Where $V_{EB}$ is the built-in potential of the n–p–n transistor Base-Emitter junction.

The value of the resistor $R_p$ can be expressed using the IGBT's current $I_{AKlup}$ (measured or given in the data sheets) causing the latch-up and the current gain of the bipolar transistor $\beta(Q1)$:

$$R_p = \frac{V_{EB}(Q2)}{I_c(Q1)} = \frac{V_{EB}(Q2)}{I_{AKlup}} \times \frac{\beta(Q1) + 1}{\beta(Q1)}.$$

Although this latch-up model is simple, it allows for modelling the static latch-up in circuit simulation.

III. RESULTS

We have adjusted our model to simulate two IGBT devices from International Rectifier (IR): IRGBC20S and IRGBC40F with various powers and switching speeds. The first one is a standard type 600 V–20 A, and the second one is a fast type 600 V–40 A.

The SPICE parameters of the models corresponding to the two IGBT devices are determined so as to fit the data sheet static and dynamic electrical characteristics.

Figures 3 and 4 show the I–V characteristics, simulated (a) and given in the manufacturer's data book (b), for an IRGBC20S and an IRGBC40F samples respectively. A good agreement is recorded for both IGBT devices.

Concerning the switching parameters, only the switching time values are given in the data sheets. These values are compared in Table I with those obtained by our model.

The data sheets correspond generally to typical value or to average values obtained from several samples. To verify the accuracy of our
model, we have compared its results with experimental ones performed on a given IGBT sample. The results of this comparison are shown in Figures 5 and 6, for static and dynamic characteristics, respectively. The simulation fits very well the experimental characteristics.
The forward biased SOA voltage value measured for an IRGBC20S sample is $\approx 815$ V, therefore, the BV parameter value is fixed in the SPICE program as $815.7$ V. Figure 7 shows the $I-V$ characteristics


### TABLE I  
Comparison of the switching times simulated and given in the data sheets for two IGBT devices: IRGBC20S and IRGBC40F

<table>
<thead>
<tr>
<th></th>
<th>IRGBC20S Data sheets</th>
<th>IRGBC40F Data sheets</th>
<th>IRGBC20S Model</th>
<th>IRGBC40F Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fall time $t_f$ (ns)</td>
<td>1600</td>
<td>420</td>
<td>1425</td>
<td>414</td>
</tr>
<tr>
<td>Turn-off delay time $t_{doff}$ (ns)</td>
<td>1200</td>
<td>410</td>
<td>1147</td>
<td>408</td>
</tr>
<tr>
<td>Turn-on delay time $t_{don}$ (ns)</td>
<td>24</td>
<td>26</td>
<td>23</td>
<td>26</td>
</tr>
<tr>
<td>Rise time $t_r$ (ns)</td>
<td>23</td>
<td>37</td>
<td>26</td>
<td>32</td>
</tr>
</tbody>
</table>

**FIGURE 5**  
I–V characteristics obtained by simulation and by measurements for an IRGBC20S sample.
simulated and measured showing the forward biased SOA of an IGBT.

For the same sample, the IGBT reverse biased SOA voltage value measured is \( \approx 22 \) V, with a fixed supply voltage value \( V_{EC} \) as 20.6 V. The anode current versus anode–cathode voltage characteristics simulated and measured are shown in Figure 7. This is to demonstrate the ability of our model to simulate the reverse biased SOA of an IGBT.

Latch-up occurs when the voltage drop over the \( R_p \) resistor is larger than the built-in potential of the Base-Emitter junction of the parasitic n–p–n transistor. To illustrate the ability of our circuit model to simulate latch-up phenomena, arbitrarily values \( I_{AK_{lup}} \) of the anode current have chosen as \( I_{AK_{lup}} = 19 \) A and 35 A for IRGBC20S and IRGBC40F respectively. The value of the \( R_p \) resistor is then adjusted so as to obtain a current latch-up value greater than or equal to \( I_{AK_{lup}} \). Figure 8 shows the simulated I–V characteristics for the two devices.
and the beginning of the latch-up. The $R_p$ value is not used in Figures 3 and 4 simulations, these IR devices being latch-proof.

IV. CONCLUSION

In this paper, a simplified IGBT SPICE model has been described. This model is built from consideration of static and dynamic operating conditions. Although this model is simple, it is capable to simulate the operation of the IGBT and its different behaviors. This model presents two main advantages:

- an easier adaptation to any IGBT type, such as vertical or lateral, high or low power range. The model fitting is done by adjustment
The simulation results are confirmed by comparison with the experimental results and with manufacturer’s data. The results are in perfect agreement.

References


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