A COMPLICATION OF NEGATIVE RESISTANCE CIRCUITS GENERATED BY TWO NOVEL ALGORITHMS

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There are two algorithms to generate a negative-resistance device which exhibits either a type-N shaped V-I characteristic similar to a tunnel diode, or a type-S shaped V-I characteristic similar to a four layered pnpn diode.

We present here a selection of these circuits using bipolar, JFET or MOSFET or their combinations.

INTRODUCTION

Solid-state devices possessing differential negative resistance are very useful for a wide range of applications involving oscillation, amplification and logic operations. A novel approach for inventing new solid state negative resistance devices is to combine two or more Bipolar – JFET – MOSFET transistors with resistors. They can be easily fabricated and mass produced as integrated circuits.

GENERATION OF TYPE-N (VOLTAGE CONTROLLED) DEVICES

We have generated some devices using Type-N algorithm and we can arrange them in the order of $n = 0, 1, 2, \dots$

A type-N device is called intrinsic if $n = 0$ or no resistors.

We have compiled 3 such circuits as in Figure 1. Figure 1(a) is made of 2 complementary MOSFETs; Figure 1(b) is made of 2 complementary JFETs and Figure 1(c) is made of a n JFET and a PMOSFET. For $n = 1$, similarly, 3 circuits are shown in Figure 2. For $n = 2$, 2 circuits are given in Figure 3 and for $n > 2$, one circuit is depicted in Figure 4.

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FIGURE 1

FIGURE 2

FIGURE 3

FIGURE 4

FIGURE 5

GENERATION OF TYPE-S (CURRENT CONTROLLED DEVICES)

Figures 5, 6 and 7 similarly delineate the Type-S negative resistance circuits generated as a dual of above for $n - 1, 2$ or >2 respectively.

CONCLUSIONS

A compilation of Type-N and Type-S negative resistance circuits is briefly presented herein. The two algorithms can be implemented by using computer graphics and advanced data structure to generate more such devices and in lesser time.

FIGURE 6

FIGURE 7

References

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