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# DESIGN AND DEVELOPMENT OF MONOLITHIC MICROWAVE INTEGRATED AMPLIFIERS AND COUPLING CIRCUITS FOR TELECOMMUNICATION SYSTEMS APPLICATIONS

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Recent advances in printed circuit and packaging technology of microwave and millimeter wave circuits result to the increasing use of MMICs in telecommunication systems. At Microwave and Fiber Optics Lab of NTUA several designs of various MMICs were conducted using the HP Eesof CAD Tool and FET and HEMT models of F20 and H40 GaAs foundry process of GEC Marconi. The designed MMICs are constructed in Europractice Organization while on-wafer probe measurements are performed in the Lab. In that framework, MMIC technologies are employed in the design of power and low noise amplifiers and couplers to be used for mobile and wireless communications as well as remote sensing and radar applications. A medium power linear FET amplifier has been designed with combining techniques on a single chip. The circuit operates at 14.4–15.2 GHz with an input power of −15 dB m, a 36 dB total gain, while the input and output VSWR is less than 1.6. Due to high cost of MMIC fabrication only the first subunit was manufactured and tests verified the simulation results. Additionally, novel techniques have been used for the design of two coupling networks at 10 GHz in order to minimize the area occupied. A meander-kind design as well as shunt capacitors were implemented for a 90° quadrature coupler and a Wilkinson one in order to reduce size. Finally, a two stages low noise amplifier was designed with the use of H40 GaAs process in order the differences between the relevant designs to be explored. The key specifications for this MMIC LNA include operation at 10 GHz with a total gain of 17 dB while the noise figure is less than 1.5 dB.

## 1 INTRODUCTION

Recent advances in printed circuit technology and especially in packaging technology emerged a continuously increasing use of Monolithic Microwave Integrated Circuits (MMICs) in telecommunication systems. MMICs consist of various elements, FETs and transmission lines all in a single chip, especially in a GaAs substrate. A variety of microwave circuits such as amplifiers, mixers, couplers, phase shifters and others can be integrated while the use of MMIC is expanded in several different applications [1–3]. Due to the tenuous efforts for large-scale integration, significantly reduced size of structures can be fabricated in vast quantities, while more stages and components are implemented. The

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result is the construction of chips with reduced power consumption and improved reliability performance.

The fabrication's yield and repeatability have an important role in MMIC technology. That imposes the capabilities of relevant foundries to produce chips with the same performance characteristics. The MMIC design with CAD tools is of major importance due to the performance simulation and parameter optimization capabilities that provides. Thus, the designer is able to define almost in detail the final operation of the circuit under consideration. In the following three MMIC circuits designs will be presented. The circuits include a medium power amplifier chip, MMIC coupling circuits and a Low Noise amplifier design.

## 2 MEDIUM POWER AMPLIFIER

A medium power linear FET amplifier design on a single chip has been developed at the Microwave and Fiber Optics Lab of N.T.U.A. using the Libra Touchstone CAD Tool of HP Eesof [4]. The circuit is based on different types of non-linear FET models of GEC-Marconi's F20 process library [5]. This amplifier is a part of a full duplex sub-SDH (51.84 Mbit/s) wireless digital telecommunication system, which operates in the 14.5–15.2 GHz frequency band, while the carrier frequency is 32-QAM modulated. The medium power amplifier is placed before the final transmitting power amplifier and provides an output power of 21–22 dB m. The medium amplifier's key specifications are given in the following:

### 2.1 Specifications

| | |
|---|---|
| Bandwidth | 14.4–15.2 GHz |
| Input power | −15 dB m |
| Total gain | 37 dB |
| Noise figure | <8 dB |
| $VSWR_{in,out}$ | <1.6 |
| Output power | >21 dB m |
| Spurious | −90 dB c |

### 2.2 Design Concepts and Techniques

The main concept of the design is the implementation of combining techniques which consist of the use of 3 dB branch line hybrid couplers as power spliters and combiners [6–9]. Due to the fact that in any case, no more than 7–8 dB gain per amplifying stage could be achieved, it is obvious that in order to accomplish the 22 dB total gain, about 6–7 stages should be designed. The schematic block diagram of the medium power amplifier in Figure 1.

The input signal is amplified by the first cascade stages and then the signal is divided equally by the coupler who serves as splitter. Each branch consists of identical amplifying stages. Then a second coupler combines the signal of each branch and thus the output power is twice that obtained from the single individual stage. Furthermore, the amplifier's linearity should be taken under serious consideration. The used modulation scheme of the whole tranceiver system being a 32-QAM imposes a strict linear response. Significant FET non-linearities must be taken into account since they can result in distortion of the digital signal and subsequently in increasing BER. The latter automatically limitates

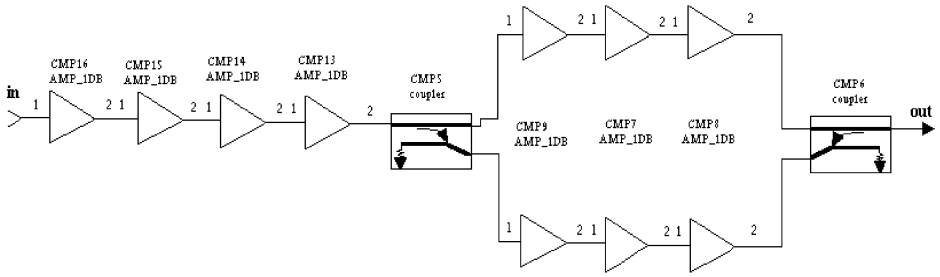



FIGURE 1

the selection of the FETs and thus the maximum output power that these can provide. The GEC Marconi's FET library used is based on an advanced GaAs F20 process with 0.5 μm gate length and $F_t = 24$ GHz.

Various FET models are concerned reference to their gate length [4, 5]. As the FET's gate length increases, the 1 dB compression point increases too, resulting in higher obtained output power. Despites this, a large gate length has an opposite effect on the FET's transducer gain imposing a trade-off between total gain and output power. In other words, a large gate length FET can provide a 3–4 dB total power gain while its output power is respectively large, 23 dB m. Apart from that GEC Marconi's library provides several non-linear as much as linear models. Non-linear models are basically used in the present work since they provide a more realistic performance due to the fact that their electrical characteristics have been defined through measurements by GEC Marconi's foundry. Thus, the basic principle of the design is, since the input power is low enough, to start with FETs with small gate lengths which can provide much gain. Then the design proceeds eventually to the use of FETs with larger gate length which compensate their low gain with the ability to provide higher output power.

Two kinds of analysis were implemented: linear and non-linear. Linear analysis includes *S*-parameter analysis and gain as well as stability factor *K* and matching. Non-linear analysis in Libra Touchstone HP Eesof Software includes DC analysis (curve tracer and bias) and harmonic balance analysis where the 1 dB compression point, the 3rd order intercept point and the frequency spectrum are determined, extracting the amplifier's intermodulation products. Several simulations and optimizations are encountered in order to anticipate losses in distributed transmission lines, parasitic inductances and susceptances as well as in lumped elements.

### 2.3 Fet Models

Following the design concepts, 4 kinds of FETs were examined regarding their bias and their scattering and electrical characteristics: $4 \times 75$ μm, $6 \times 125$ μm, $6 \times 150$ μm, $6 \times 175$ μm. As it is mentioned previously the first design steps include small gate length FETs, that is, $4 \times 75$ μm and $6 \times 125$ μm. At the end, FETs with eventually larger gate length, ($6 \times 150$ μm and $6 \times 175$ μm) were used in order to produce higher output power at the coupler branches.

The $4 \times 75$ μm FET can produce large gain and thus is used into the first 3 cascade amplifying stages until the point where the imposed non-linearities could not severely effect the output signal. Then, due to the fact that the 1 dB compression point of that FET is rather small, a larger gate length FET $6 \times 125$ μm is being used. The whole branch is given in

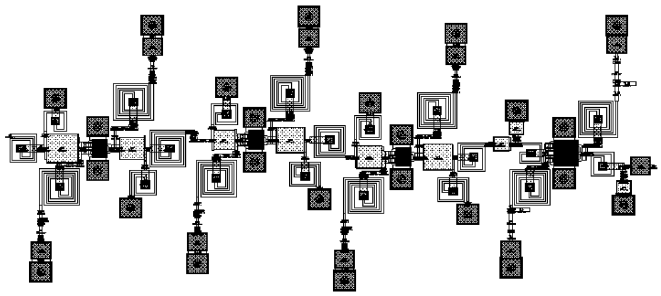


FIGURE 2

Figure 2. After that, higher compression–less gain FETs are used with the implementation of the 3 dB hybrid couplers. Every coupler branch consists of 2 FETs $6 \times 150\,\mu m$ and one $6 \times 175\,\mu m$. Finally, at the combiner coupler's output the desirable signal is produced.

### 2.4 3 dB Hybrid Coupler

In the following a more detailed presentation for the hybrid couplers is presented.

The combining technique used in the design under consideration, with the implementation of the two hybrid couplers, finds several applications in power splitters or power combiners in various microwave circuits such as power amplifiers or mixers. Couplers are widely used in designing especially power amplifiers because they present the following advantages [6]:

- high degree of stability and low VSWR,
- if one amplifier fails the other will still operate with reduced gain
- the stage isolation leads to cascade with other units.

The coupled $l_g/4$ length lines ($l_g$ being the signal wavelength at the specific transmission line) are usually too large for MMIC applications and they occupy large area on the chip lay-out which coscequently results to high construction cost. For that reason, the reduced size branch line technique with the use of external capacitors is being implemented [10]. This technique imposes transmission lines with smaller length but with higher characteristic impedance as well as external shunt capacitors as it is shown in Figure 3.

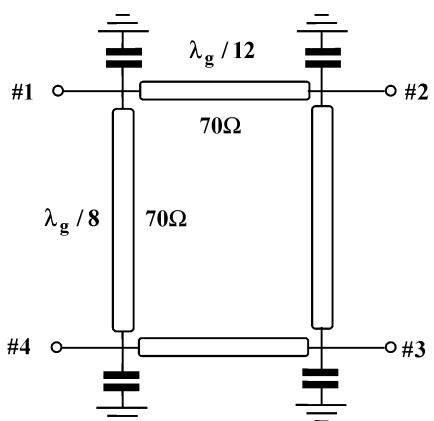



FIGURE 3

Thus, a 3 dB branch line coupler is designed with lengths $l_g/8$ and $l_g/12$ of wavelength and the final area occupied can be reduced significantly, up to 80%. The coupler, as a passive circuit, is also examined by the CAD Tool's electromagnetic simulator (based on the Method of Moments technique) called Momentum. This proved to be an excellent verification for the correct coupler design. The final coupler performance for a band of frequencies between 10 GHz and 20 GHz is shown in the diagram of Figure 4 while the layout diagram is given in Figure 5.

From Figure 4 is derived that, despite the fact that the optimisation goals for the scattering parameters have been accomplished, the insertion loss of the coupler is 4.75 dB. This implies that the models used introduce 1.56 dB losses in the transmission lines as well as to the shunt capacitors due to paracitic phenomena. Finally, the total area occupied by the coupler, including the capacitors, is approximately 0.64 $mm^2$, since the length of the transmission lines is approximately 750–800 μm. In comparison to the relevant occupied area of the common hybrid coupler for the same wavelength (approximately 2 $mm^2$), a reduction of a 68% has been achieved.

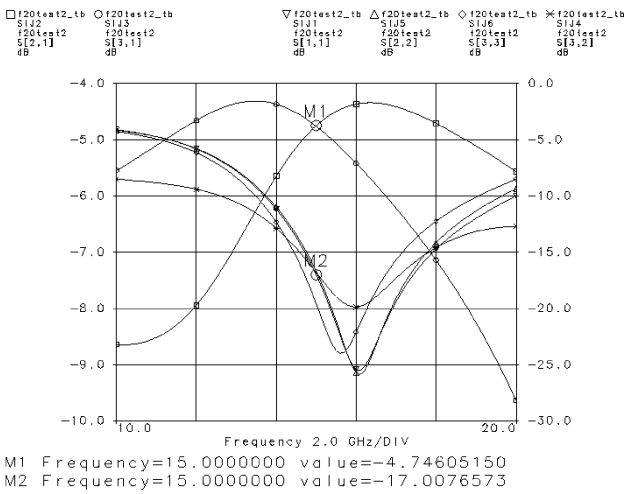



FIGURE 4

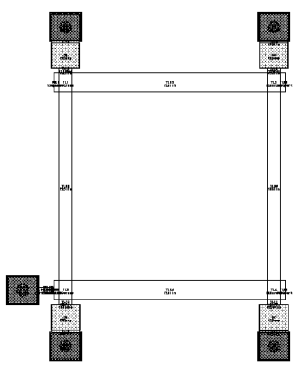


FIGURE 5

## 2.5 Results

Following continouous attempts simulating, optimizing and taking under consideration the layout rules imposed by the CAD tool, the final performance results of the total medium power amplifier are extracted. These are shown in the following table:

| | |
|---|---|
| Bandwidth | 14515–15103 MHz |
| Input power | −15 dB m |
| Total gain | 35.8 dB |
| Noise figure | <5 dB |
| $VSWR_{in,out}$ | <1.6 |
| Output power | 21 dB m |

The performance of the whole amplifier unit due to simulation is given in the diagrams of Figures 6 and 7. From these figures it is derived that the total gain of the circuit is

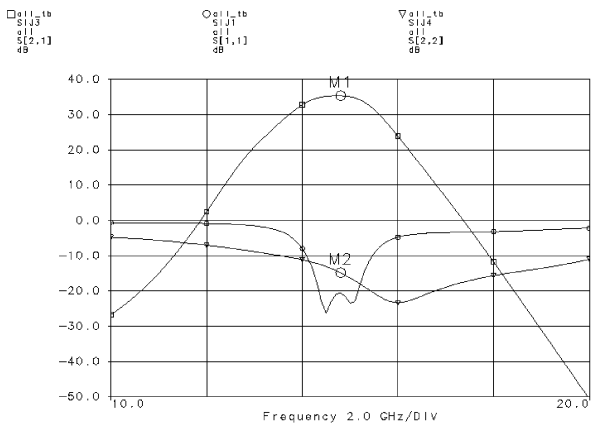



FIGURE 6

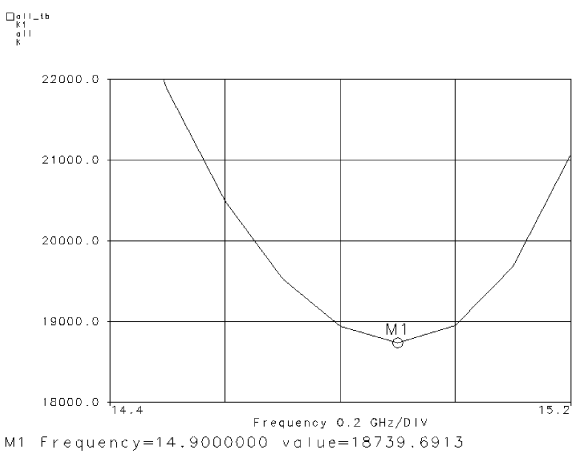



FIGURE 7

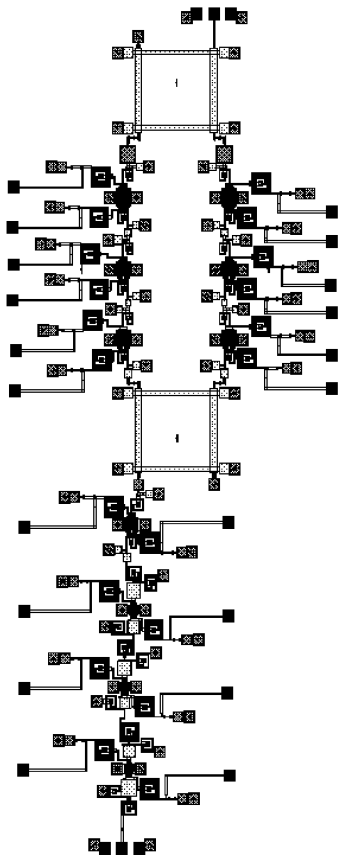


FIGURE 8

approximately 36 dB while a very good degree of stability is obtained as well as a noise figure of 5 dB at the bandwidth of consideration. The layout diagram is shown in Figure 8.

## 3 MMIC FABRICATION

The total area occupied is rather large (36 $mm^2$) due to the large dimensions of the FETs used. As it is already described, the circuit in its final form includes 10 FET units with an output power of approximately 22 dB m. The whole design corresponds to a high construction and fabrication cost due to the fact that the cost depends on the area occupied in $mm^2$. Due to this fact, only the first one subunit was fabricated by EUROPRACTICE Organization. In any case, the proper operation of even this one subunit can provide information regarding the design and simulation qualification. In other words, the correct operation of this small unit is a good indication of the proper performance of the whole circuitry in a high degree.

From EUROPRACTICE organization and GEC Marconi's foundry 10 naked chips and 33 free naked extra dies were received while the chips were tested for good performance with the use of a HP 8510C Vector Network Analyzer (45 MHz–40 GHz) and a Carl Suss Probe Station for on wafer measurements [11]. This first subunit was designed with the use of the linear FET model $4 \times 75$ while its layout diagram is following in Figure 9.

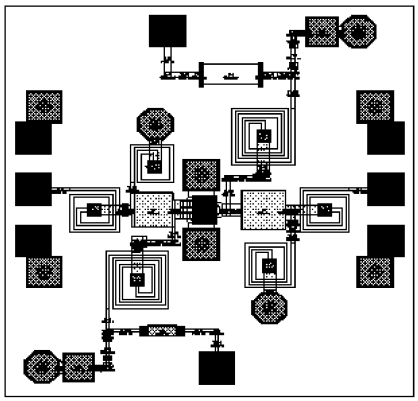


FIGURE 9

The operational characteristics are being presented below:

$$\mathrm{GTU_{max}} = 12\,\mathrm{dB\,m},\ \text{Bias: } 0.81I_{\mathrm{DSS}} = 38\,\mathrm{mA},\ V_{\mathrm{DS}} = 5\,\mathrm{V},\ V_{\mathrm{GS}} = -0.22\,\mathrm{V}$$

The relevant bias resistance for $V_{\mathrm{supply}} = 10\,\mathrm{V}$ is $R_P = 131\,\Omega$.

From the simulation procedure which is also the expected performance, becomes that the input and output reflection coefficients $S_{11}$ and $S_{22}$ are below $-15$ dB for the frequency bandwidth of interest (14.4 GHz–15.2 GHz). In other words, the input and output VSWR are below 1.5 in almost the entire frequency band of interest. By that way, the amplifying unit achieves a 7.5 dB gain approximately with ripple less than 0.5 dB in the specific band. Finally the parameter $S_{12}$ is much lower than $-16$ dB. All expressions show the satisfactory performance of the circuit in terms of scattering parameters. So, it is foreseen that with an input power of $-15$ dBm the output power of the unit is $-7.5$ dBm. All the expected results are shown in the following diagrams of Figures 10 and 11, which are derived from the HP Eesof simulation procedure.

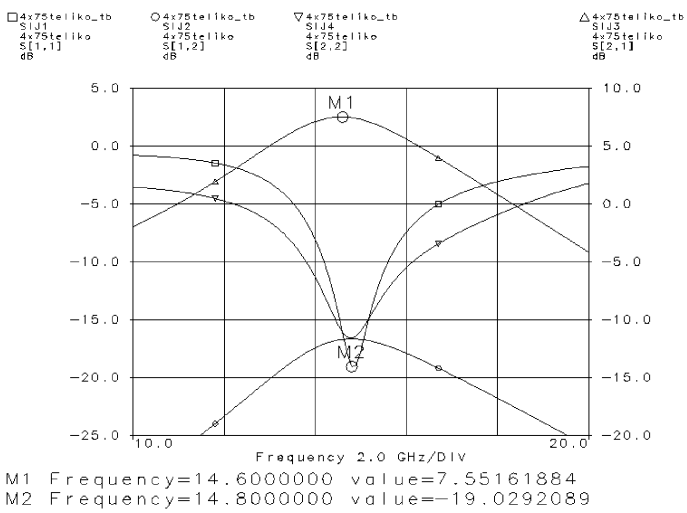



FIGURE 10

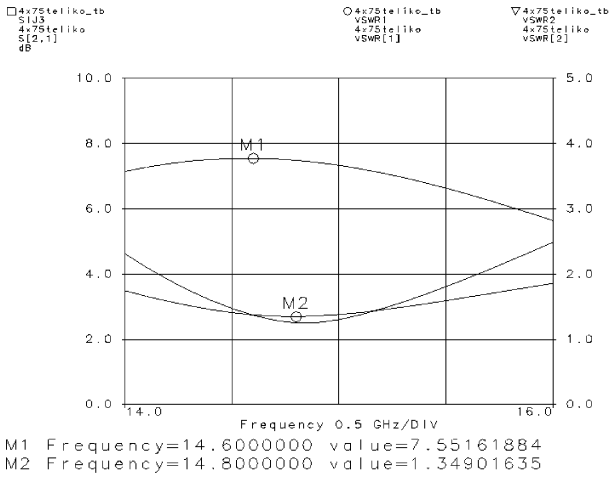



FIGURE 11

In Figure 10 the scattering parameters are shown for the 10 GHz to 20 GHz bandwidth where marker M1 corresponds to the maximum gain 7.55 dB and marker M2 represents the reflection coefficient $S_{11}$. It is obvious that the input and output reflection coefficients are below $-15$ dB in the frequency bandwidth of interest. In Figure 11 the expected subunit gain is drawn inside the frequency band of operation where the low in band ripple is also shown. Additionally the input and output VSWRs are drawn and are below 1.6 in the band of 14.8 GHz–15.2 GHz.

Regarding the testing procedure the following was realized. The Probe Station is connected to the Network Analyzer with two input and output heads while two others were used for the positive and negative voltage supply of drain and source. On wafer standard loads were used for the calibration of the Vector Network Analyzer and 3 samples from the received chips were actually tested in order the foundry's yield and repeatability to be

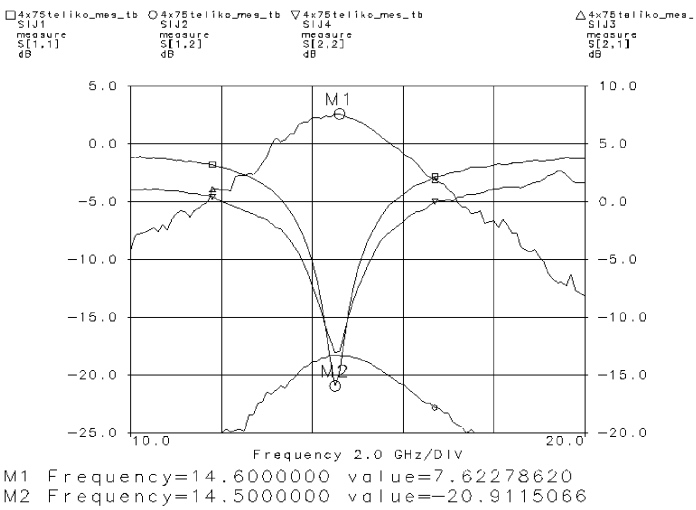



FIGURE 12

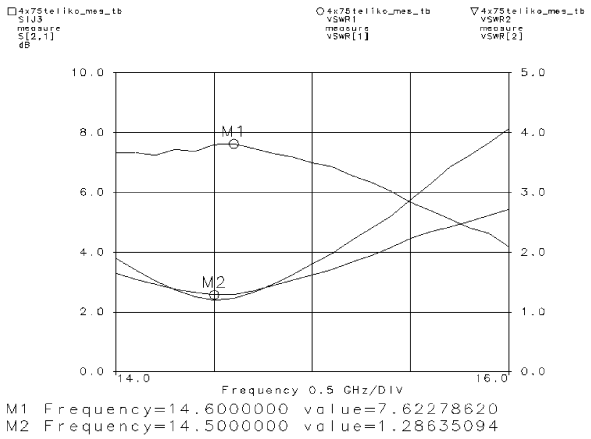



FIGURE 13

confirmed. The test results and thus the real final results are shown in the following diagrams of Figures 12 and 13.

In Figure 12 the scattering parameters are drawn for the same bandwidth used in the expected results figures. Marker M1 corresponds to a maximum gain of 7.62 dB while marker M2 to reflection coefficient, the value of which is in fully accordance with the simulation results. The same compliance between simulated and tested results is obtained and through a comparison of Figure 13. It is obvious that there is full accordance between expected and actual results while in some cases slightly better characteristics were achieved. Since it was certified in all 3 samples that were tested the chips repeatability is very satisfactory.

In general it must be noticed that despite the fact that it was not possible to construct and fabricate the whole amplifier unit, the results derived from one constructed subunit are very satisfactory and the relation between design simulation and construction is successful [11].

## 4 QUADRATURE AND WILKINSON COUPLERS

In addition to the medium amplifier as an active MMIC circuit, which was described in the previous paragraphs, the design of passive components is given in the following. These passive circuits are a quadrature and a Wilkinson coupler. By that way, the most important technologies used, along with the relevant design concepts are presented. These two kinds of couplers were used for the development of a conformal array system placed on a cylindrical surface [12]. The system operates at X-band and can be used in mobile telecommunications applications or radar and remote sensing ones. The 10 GHz carrier frequency is QPSK modulated while for the relevant MMICs the GaAs F20 process of GEC-Marconi is being implemented also.

In order to complete the QPSK modulator two kind of couplers were used. The quadrature coupler is used for the synthesis of the QPSK modulated carrier of 10 GHz (which is provided by a Local Oscillator) and is being divided. This quadrature coupler provides the necessary 90° phase shift between its two outputs which are then being lead to the mixers for the completion of the I and Q channels (200 MHz bandwidth) modulation. In order to reduce the size of the coupler, a meander kind design of the transmission lines was implemented as well as shunt capacitors according to [10]. The quadrature coupler performs

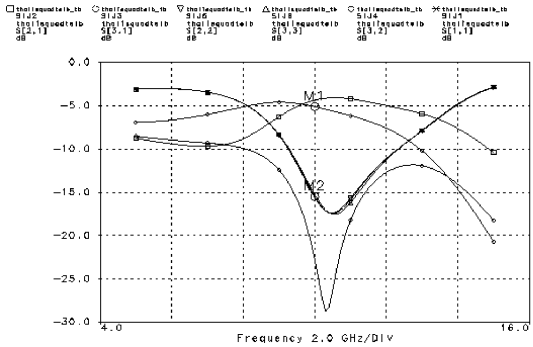



FIGURE 14

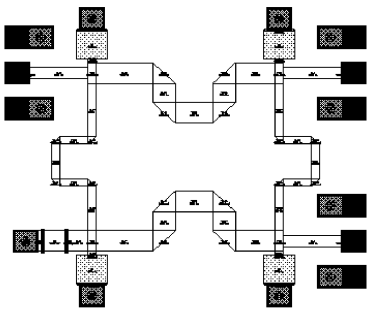


FIGURE 15

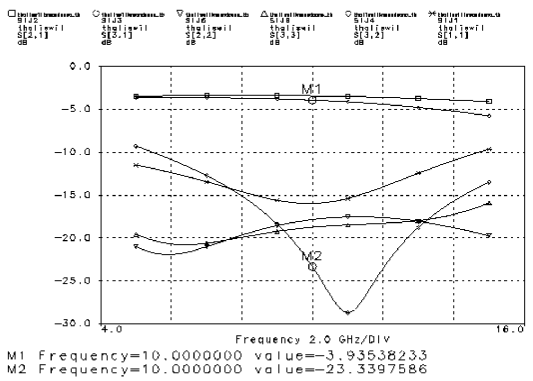



FIGURE 16

approximately 2 dB losses due to the GEC Marconi's foundry models used while the isolation between the output ports was approximately 24 dB [6]. In the following Figures 14 and 15 the *S*-parameter results as well as the layout diagram of the MMIC quadrature coupler are shown.

The same reduced size technique was implemented to the wilkinson coupler that is used to combine the two outputs of the mixers so that the QPSK signal is obtained. The wilkinson coupler performs the desired behavior with an isolation of approximately 23 dB between the

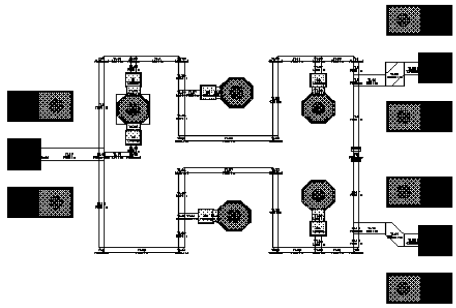


FIGURE 17

two output ports. In Figures 16 and 17 the simulation results and the layout diagram of the Wilkinson coupler is presented as well.

## 5 LOW NOISE AMPLIFIER

Following the design and the development of the power amplifier a presentation of a two-stage low noise amplifier (LNA), which was designed with the use of the HP Eesof design software, will be made [4]. The most interesting point of this design, apart from the amplifier's performance, will be to evaluate the models used for the development of the LNA. As it has already been mentioned the power amplifier was designed with use of the GEC-Marconi F20 library. The proposed LNA will be developed with the use of the H40 GEC-Marconi library [13]. This library which was released some years after the F20 [2, 5] uses HEMT models with an $f_T = 40\,\text{GHz}$ (in F20, $f_T = 24\,\text{GHz}$) and has improved characteristics compared with the F20 (*e.g.* increased gain, decreased noise figure for transistor models with the same occupied area).

So apart from the design concept of the LNA which presents great interest, an evaluation of the H40 library will be attempted and also a comparison between H40 and F20 based on the results obtained and described in the previous paragraphs. The basic specifications of the LNA are the following:

1. Operation frequency: 10 GHz
2. Bandwidth: 500 MHz (9.75–10.25 GHz)
3. Noise figure, NF $< 1.5$
4. $S_{11}$, $S_{22} < -15\,\text{dB}$ which is equivalent to $VSWR_{\text{in}}$, $VSWR_{\text{out}} < 1.5$
5. $S_{12} \leq -25\,\text{dB}$
6. Total gain for both stages $18 \pm 1\,\text{dB}$ ripple
7. Total occupied area for the whole MMIC design $< 3\,\text{mm}^2$

The last specification is not a technical one but it is directly connected to the manufacturing cost of the MMIC. Since this cost is relatively high, it must be taken under consideration and thus the specifications of the LNA should include this aspect. Following the introduction of the LNA an analysis of the designed steps will be presented in the next paragraphs [3].

### 5.1 Selection of HEMTS

There are two different categories of HEMTS among which a designer must make a selection: linear and the non-linear models [13]. In the linear models the output power

increases unlimited as the input power increases. There is no information about the characteristic of the HEMT and its compression point. Additionally the bias condition is set directly as a portion of the maximum drain current $I_{DSS}$. These linear models are actually scalable models where the number and the width of their fingers are set freely by the designer. The non-linear HEMT models are completely different. The function of the output power versus the input power is a real non-linear characteristic based on accurate measurements conducted on the HEMT model. The bias conditions are set through the drain–source and gate–source voltages ($V_{DS}$, $V_{GS}$) and thus the operation point can be determined and checked for its accuracy. Finally by using this model all kinds of non-linear analysis could be carried out.

Based on the previous information presented a $2 \times 60$ linear model [13] had been finally selected for the design of both stages. The $2 \times 60$ model is a medium size HEMT with relatively small noise figure and relatively high gain. Despite the fact that the non-linear models seem to have more advantages than the linear ones, the selection of this particular model was based on two different reasons. The most important one was that after conducting several simulations with the linear and non-linear $2 \times 60$ model, we came to the conclusion that the validity of the noise data of the non-linear model was questionable. Since the primary goal was the design of a low noise amplifier, this observation was the main reason for rejecting the use of the non-linear model. From the other hand the advantages of the non-linear model are mainly focused in the existence of the non-linear data that permit the performance of the relevant non-linear analysis. In the case of a low noise amplifier with a relatively small output power the existence of these data is not crucial for the design.

### 5.2 Setting the Operation Point

For determining the operation point the non-linear model will be used since, as it has already been mentioned, the bias conditions can be set with a better accuracy through the non-linear model. So for the first stage of the amplifier, which is the most crucial for the overall noise performance, a relatively small drain current ($I_{DS} = 0.25 I_{DSS}$) was selected. In the second stage the main goal was to achieve higher gain and thus the drain current can be set as a higher portion of the maximum drain current ($I_{DS} = 0.8 I_{DSS}$). Using now the non-linear model a dc analysis was performed with the use of Eesof. In Figure 18 the variation of the bias current $I_{DS}$ versus the bias voltages $V_{DS}$, $V_{GS}$ is shown. Referring to the manual of the H40 library [13] the maximum current $I_{DSS}$ is derived for $V_{GS} = 0\,\text{V}$ and $V_{DS} = 2\,\text{V}$ (marker M1 of Fig. 18). Thus for a $I_{DSS} = 42.38\,\text{mA}$ the bias conditions for both stages can be summarized as follows:

1st stage: $V_{GS} = -0.71\,\text{V}$, $V_{DS} = 2.5\,\text{V}$ and $I_{DSS} = 0.25 I_{DS} = 10.6\,\text{mA}$ (marker M2, Fig. 18)
2nd stage: $V_{GS} = -0.20\,\text{V}$, $V_{DS} = 2.5\,\text{V}$ and $I_{DSS} = 0.80 I_{DS} = 34.2\,\text{mA}$ (marker M3, Fig. 18)

Based on the above selected operation points the bias resistors are the following:

$$\text{1st stage:}\quad R\pi = \frac{V_{DD} - V_{DS}}{I_{DS}} = \frac{3.5\,\text{V} - 2.5\,\text{V}}{10.62\,\text{mA}} \approx 95\,\Omega$$

$$\text{2nd stage:}\quad R\pi = \frac{V_{DD} - V_{DS}}{I_{DS}} = \frac{3.5\,\text{V} - 2.5\,\text{V}}{34.2\,\text{mA}} \approx 30\,\Omega$$

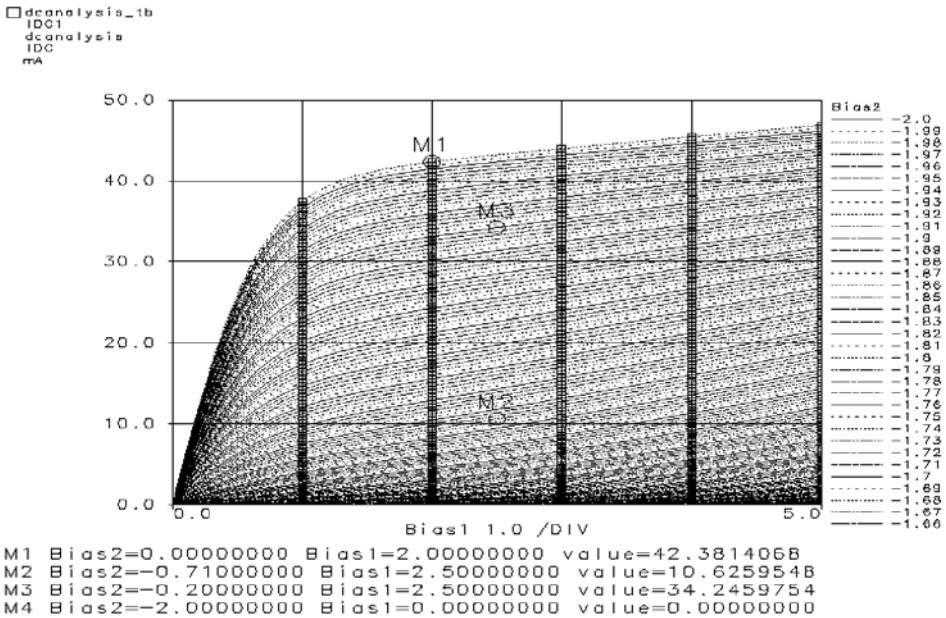



FIGURE 18

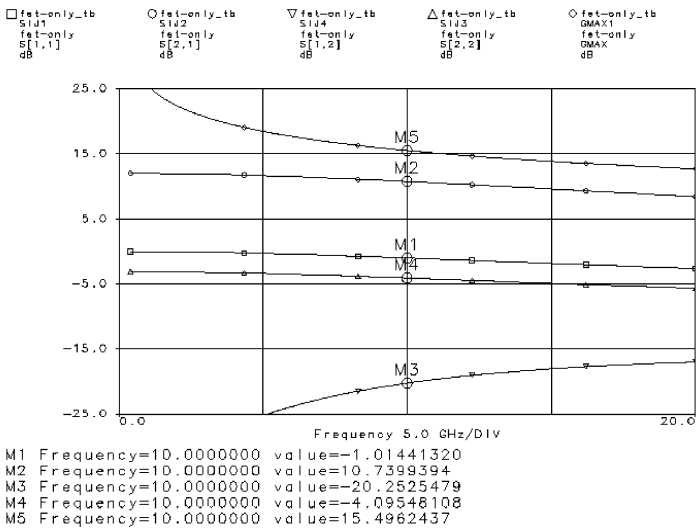
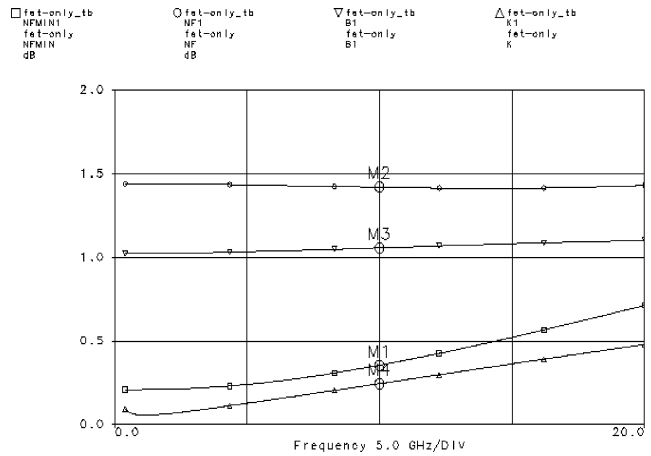



FIGURE 19
for $I_{DS} = 0.25I_{DSS}$

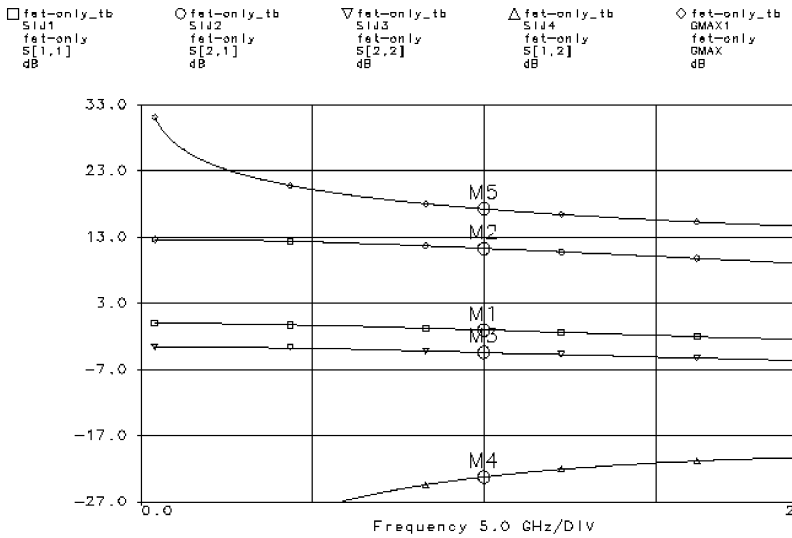
Where the output power supply voltage has been set to 3.5 V and the $V_{DS}$ voltage has been chosen to have the half value of the maximum allowable from the manufacturer ($V_{DS} = (1/2)5$ V).

Once the operation point and the bias conditions for both stages have been set the basic characteristics of the linear model for the chosen operation point are shown in Figures 19, 20, 21, 22.




M1 Frequency=10.0000000 value=0.35571549
M2 Frequency=10.0000000 value=1.41916576
M3 Frequency=10.0000000 value=1.05698514
M4 Frequency=10.0000000 value=0.24532820

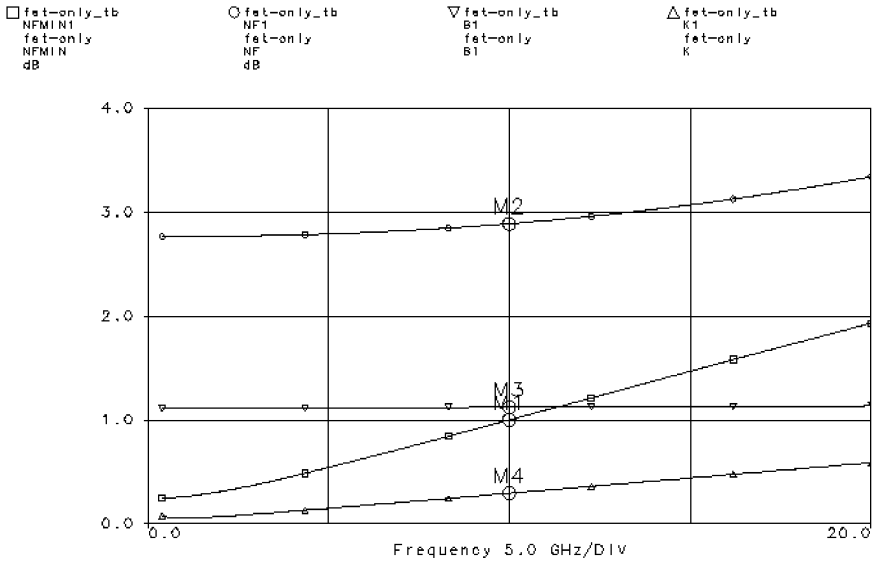
FIGURE 20
for $I_{DS} = 0.25I_{DSS}$




M1 Frequency=10.0000000 value=-1.00263041
M2 Frequency=10.0000000 value=11.3387021
M3 Frequency=10.0000000 value=-4.41778959
M4 Frequency=10.0000000 value=-23.2255103
M5 Frequency=10.0000000 value=17.2821062

FIGURE 21
for $I_{DS} = 0.80I_{DSS}$

Making some brief observations from the previous figures the main conclusions could be summarized to the following: To what it concerns the *S*-parameters there are minor differences between the two selected operation points. The HEMT is unmatched and thus $S_{11}$, $S_{22}$ are completely out of the specifications. The $S_{21}$ parameter is relatively high (10–11 dB) compared to the maximum available gain $G_{max}$(15.5–17 dB) since there is no




M1 Frequency=10.0000000 value=1.00302985
M2 Frequency=10.0000000 value=2.89050717
M3 Frequency=10.0000000 value=1.12559581
M4 Frequency=10.0000000 value=0.29710470

FIGURE 22
for $I_{DS} = 0.80 I_{DSS}$

matching at all. This fact denotes that there might be a stability problem with this model. Checking the $K$ factor (Fig. 20, 22) for both operation points denotes that this HEMT is potentially unstable (while $B > 0$ everywhere $K < 0.5$ everywhere). Special care should be taken for securing unconditional stability ($B > 0$, $K > 1$) [6] not only in our bandwidth but for a much larger portion of the spectrum (0–20 GHz) because there is always a danger for unwanted oscillations outside the amplifiers bandwidth.

The $G_{max}$ parameter, as it was expected is approximately 2 dB higher for the $I_{DS} = 0.80 I_{DSS}$ case while $NF_{MIN}$ is also increased (from 0.35 dB to 1 dB). The previous two observations prove that the operation points for both stages were properly selected. Finally, $S_{12}$ parameter is acceptable while the NF due to the lack of input matching is high (1.5 dB and 2.9 dB) for both stages.

### 5.3 Design of the Bias Networks

Based on the selected operation point, a bias network should be designed considering the following aspects: [3]

- This network should set with accuracy the operation point to both stages.
- The bias network should also improve the stability of the relevant stage and if possible its input and output matching.
- It should not affect the RF performance of the stage and it should add the least possible noise.

Based on the previous observations in Figures 23 and 24 the schematics of the bias networks of the drain and the gate respectively are presented:

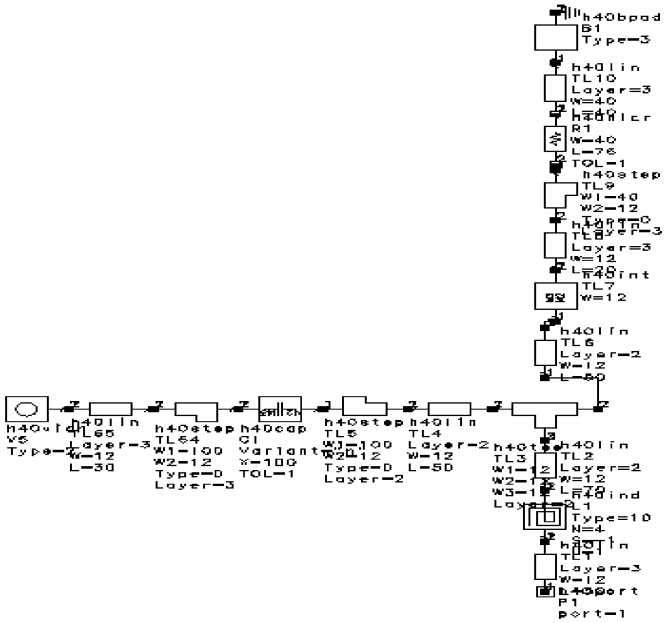


FIGURE 23

FIGURE 24

Some brief remarks about the bias networks are the following: The drain bias network is the same for both stages with a change only in the bias resistor. The gate bias network is exactly the same for both stages and in the place of the bias resistor there is a small protection resistor (50 Ohm). In order to ensure that the RF performance of both stages would not be altered with the addition of the biasing networks the values of the chocks and the capacitors were optimized for achieving an $S_{11} = -1$. The final simulation showed a $S_{11} = 0.982 \angle -1.7^\circ$ at 10 GHz, which is very close to the desired value. The values chosen for the elements of the

bias networks are more or less finalized and they should not be changed in the following design procedure. If any changes have to be made in order to achieve a better input and output matching performance or an improved NF, they should not be embedded in the networks without rechecking the compliance with the desired value of $S_{11}$.

The next step of the procedure was the simulation of $2 \times 60\,\mu m$ HEMTs basic characteristics with the addition of its biasing networks. Stabilization of the amplifier was also attempted by adding negative feedback from the source to the ground (it was realized with the use of an RF chock) [6]. The final simulation results are shown in Figures 25 and 26 and they are referring to $I_{DS} = 0.25 I_{DSS}$ stage.

Observation of the two previous figures lead to some important conclusions. These two graphs should be compared with Figures 19 and 20 where the same characteristics of the HEMT were presented without the presence of the bias networks. The values of $S_{11}$, $S_{22}$ parameters are changed but since there is no input or output matching yet this change has no valid significance. The value of $S_{12}$ has increased (3 dB) compared with one in Figure 19 and this can be perfectly explained by the appliance of the negative feedback. A significant decrease (almost 5 dB) also appears in the values of $S_{21}$, $G_{max}$ (compared with Fig. 19), which is also explained by the negative feedback. Unfortunately this is the price to be paid for the stabilization of the amplifier.

The value of $NF_{MIN}$ has actually been doubled (from 0.3 dB to 0.6 dB) because of the addition of the lossy elements of the bias networks. The value of NF is again relatively high compared to the one of $NF_{MIN}$ but since the noise input matching networks have not been added yet, this difference cannot be evaluated. Finally the unconditional stability of the amplifier has almost been achieved because $B > 0$ for the whole spectrum (0–20 GHz) and the value of $K$ varies between 0.95–1.05 for $f > 5$ GHz. It is expected that with the addition of the matching networks and the final optimizations $K$ will become $>1$ everywhere. It must noted that presentation of the results for the 2nd stage has been avoided because the same conclusions with the ones presented can be drawn.

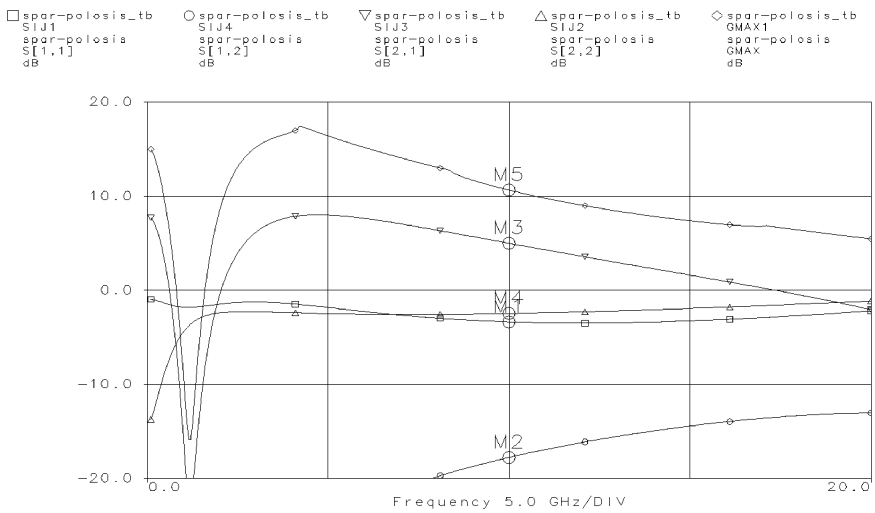



FIGURE 25

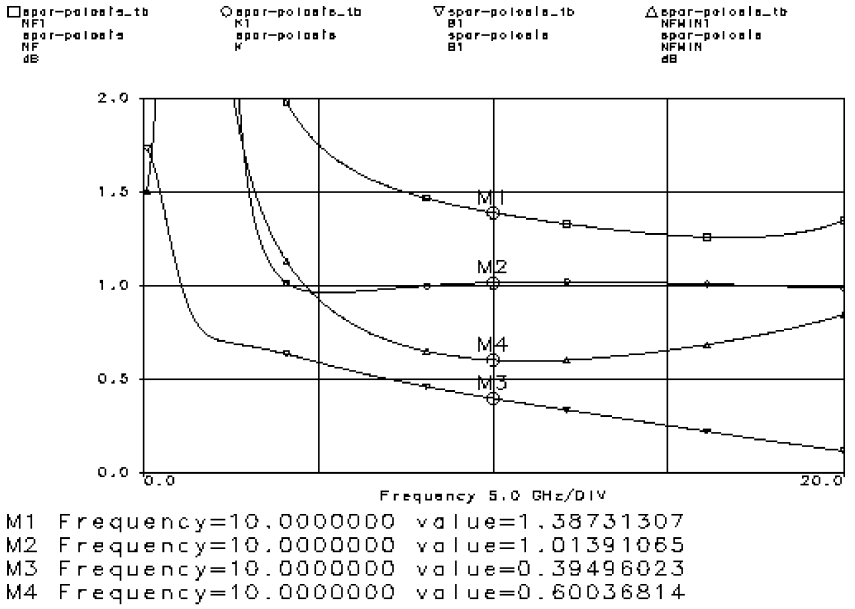



FIGURE 26

### 5.4 Design of the Input, Interstage and Output Matching Networks

This is the most important step in the design procedure because it ensures the achievement of the most crucial specifications [6, 7].

The main objective of the design is to develop a two-stage low noise amplifier. Referring to Figure 27 if the optimum input reflection coefficient of each linear $2 \times 60$ HEMT for a minimum noise figure (NF) is $G_{MN1}$, $G_{MN2}$ relatively then for a low noise design of a two-stage amplifier with an input and output matching the following relations must be accounted [6]:

- For the input network $N_S$: $\Gamma_s = G_{MN1}$
- For the interstage network M: $\Gamma_{OUT,M} = G_{MN2}$, $\Gamma_{IN,M} = \Gamma^*_{OUT,1}$
- For the output network $N_o$: $\Gamma_L = \Gamma^*_{OUT,2}$

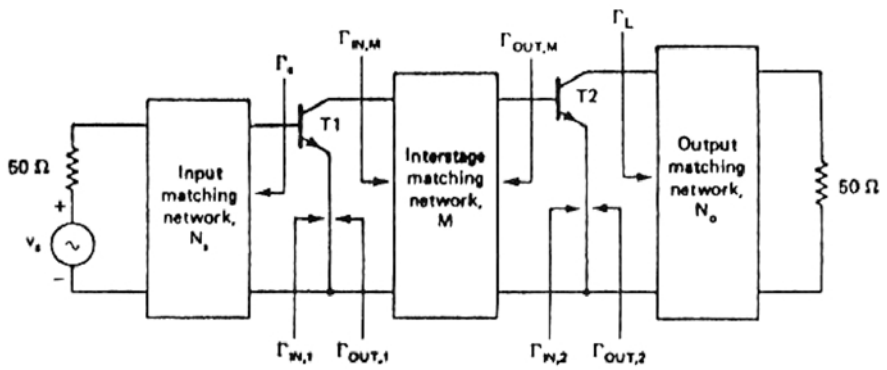



FIGURE 27

It is clear that the input matching network is focused to the minimization of the noise figure, the output to the maximization of the gain and the interstage network is used for the optimization of the noise added by the second stage and the matching between the two stages. In general in the design of two stages low noise amplifiers, while the use of the input and output circuits is straightforward the use of the interstage circuit can change according to the needs of the design. It can be mainly used for the improvement of $S_{11}$, $S_{22}$ of the whole amplifier, or for the improvement of the total NF or for both with the necessary trade-offs. In this case the main concern was the minimization of the overall NF and thus the overall performance of $S_{11}$, $S_{22}$ was not fully optimized.

In any case since there are 3 matching networks (3-degrees of freedom) and 3 parameters to optimize ($G_{MN}$, $S_{11}$, $S_{22}$) the theory suggests that there are realizable networks that could achieve all of the goals. So with the use of the Smith chart, along with a powerful tool provided by the Eesof (it is called E-syn) [4] which can match any type of passive load, each one of the three matching networks is developed and added to the circuit separately. When all the matching networks have been included a final optimization takes place for all three of $NF_{MIN}$, $S_{11}$, $S_{22}$ with the top priority being given to the minimizing of the total noise figure.

## 5.5 Design of Layout

Once the schematic of the two-stage amplifier has been finalized the relevant layout design can be produced. This layout will be produced according to the layout rules of the manufacturer. Compliance with these rules may result in minor changes in the values of some elements (*e.g.* the length of a transmission line). These changes must be transferred in the schematic for a re-simulation and a re-optimization. If there is a change in the results then the values of some elements may be changed again and these changes must be encountered in the layout. This procedure can be repeated several times until the final layout with the relevant optimized schematic design is generated. Figure 30 presents the final layout while Figures 28 and 29 present the final measurements of the characteristics of the two stage amplifier.

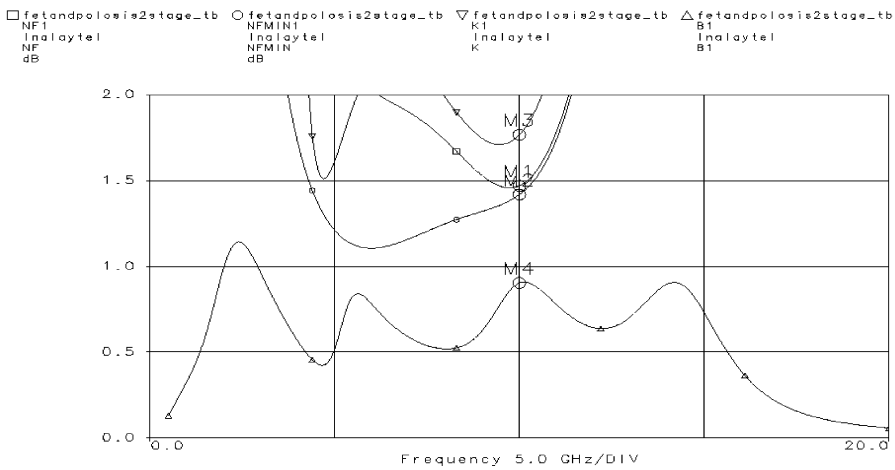
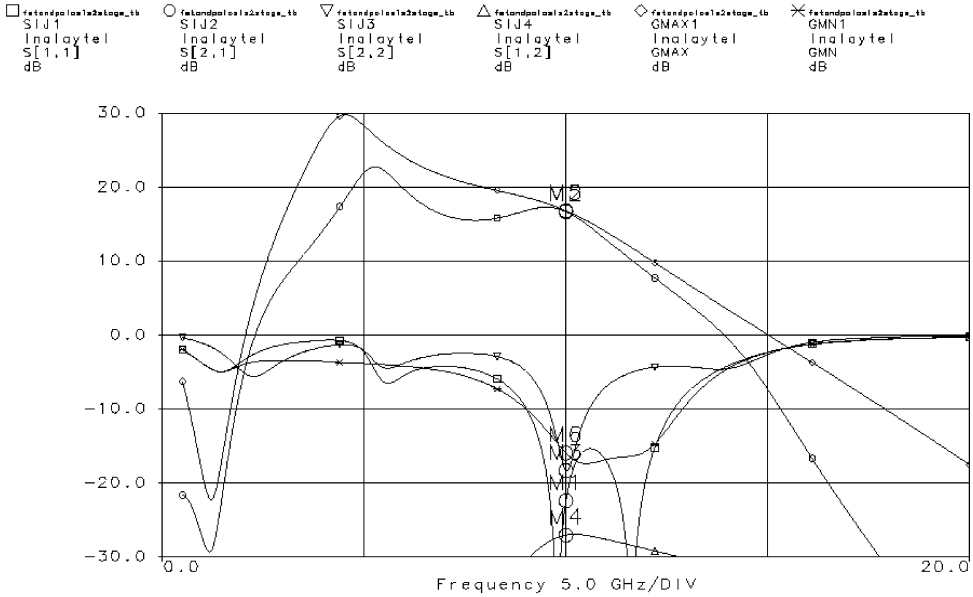



FIGURE 28




M1 Frequency=10.0000000 value=−22.4152896
M2 Frequency=10.0000000 value=16.6756216
M3 Frequency=10.0000000 value=−18.3548624
M4 Frequency=10.0000000 value=−27.0677227
M5 Frequency=10.0000000 value=16.7881266
M6 Frequency=10.0000000 value=−15.9531717

FIGURE 29

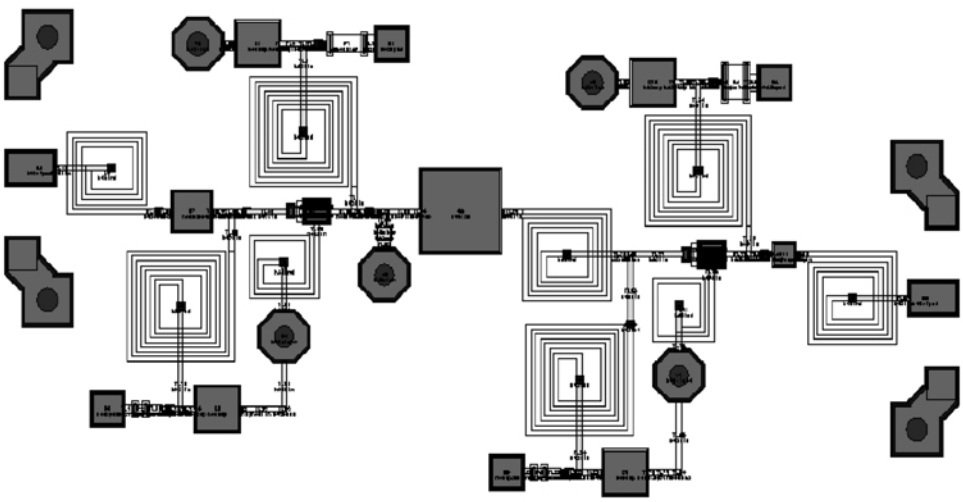


FIGURE 30

The total occupied area of the LNA is $2287 \times 1126\,\mu\text{m} = 2.6\,\text{mm}^2$ well within our specifications. Focusing now on the final results of Figures 28 and 29 the following observations can be made. The $S_{11}$, $S_{22}$ specifications are fully met (both of them are $< -15$ dB) and thus a good input and output matching has been achieved. The curves of $S_{21}$, $G_{\max}$ are practically identical in the area of 10 GHz, which means that the maximum available gain from both

stages has been obtained. (16.7 dB with 1.2 dB ripple). The slight deviation from the specifications ($18 \pm 1$ dB) could be explained with the increase in the negative feedback. Despite the fact that at the final simulation the amplifier seemed unconditionally stable ($K > 1$, $B > 0$) in such cases not only the overall $K$ of the two stages has to be $>1$ but also the $K$ of each stage separately. So in order to achieve $K > 1$ for each stage separately the amount of the negative feedback had to be increased something which had a negative effect to the gain. Finally the overall $K$ was $>1.5$ while the $K$ of each stage separately $>1.06$ and 1.12 respectively. The NF and $NF_{MIN}$ functions were very similar inside the amplifiers bandwidth and the value of NF was within the specifications ($\cong 1.46$ dB with a difference of 0.05 dB from the $NF_{MIN}$). Finally the $S_{12}$ parameter was also acceptable according to the specifications.

## 6 CONCLUSIONS

It is beyond any doubt that the H40 library presents several improvements in comparison to F20. The characteristics of its models are better and this can be easily shown from the results obtained from the LNA and the power amplifier that we have already presented. From the other hand serious problems were encountered with the H40 non-linear models and especially with their noise data. This fact forced us to use in the end a linear model instead of the non-linear one. Concluding the H40 library may have improved characteristics but it needs to be tested in several different applications in order to be fully and properly evaluated as it has already been done with the F20 one.

In conclusion, the manufacturing and testing of the designed power, low noise amplifiers and couplers show the reliability of the methods implemented. The correspondence between simulation and experimental results is extracted while focused on the comparison between the different technologies used and on the final implementation of the above circuits to wireless telecommunication systems.

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