Research Article

A 12 dB 0.7 V 850 μW CMOS LNA for 866 MHz UHF RFID Reader

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The design of a narrow-band cascode CMOS inductive source-degenerated low noise amplifier (LNA) for 866 MHz UHF RFID reader is presented. Compared to other previously reported narrow-band LNA designs, in this paper the finite $g_{ds} \times g_{eff}$ effect has been considered to improve the nanometric design, achieving simultaneous impedance and minimum $F_{min}$ noise matching at a very low power drain of 850 μW from a 0.7 V supply voltage. The LNA was fabricated using the IBM 130 nm CMOS process delivering a forward power gain ($S_{21}$) of $\approx 12$ dB, a reverse isolation ($S_{12}$) of $\approx −34$ dB, an output power reflection ($S_{22}$ @866 MHz) of $\approx −25$ dB, and an input power reflection ($S_{11}$ @866 MHz) of $\approx −12$ dB. It had a minimum pass-band $NF$ of around 2.2 dB and a third-order input referred intercept point (IIP3) of $\approx −11.5$ dBm.

1. Introduction

RFID (radio-frequency identification) is one of the fastest growing wireless communication technologies for commercial product tracking. As the low noise amplifier (LNA) is the first block in the front-end of the RFID reader which is tuned at a certain transceiver frequency, it needs to be designed optimally to minimize the noise for the following stages and avoid the distortion of the source signal (requires good linearity). To overcome design trade-off difficulties between gain, power, noise figure ($NF$) and matching in the optimization of the LNA, the design of the matching circuits at the input and the output are based, respectively, on minimal $NF$ and maximal power transfer. In recent years, considerable research on CMOS LNA design in submicron technologies at 900 MHz have been reported by many authors in [1–4]. A lower frequency standard for UHF RFID at 866 MHz is also implemented in Europe, Africa, and New Zealand. Low power dissipation at low supply voltage is a significant design criterion for RFID applications synthesized by design trade-off between gain, $NF$, input and output impedance matching and high linearity. In this paper we discuss the design and the experimental results for a 0.7 V low-power 130 nm CMOS 866 MHz single-ended common-source telescopic cascode LNA using an enhanced power constrained simultaneous noise and impedance matching (PCSNIM [5, 6]) technique.

2. Principles and Circuit Design

An inductively source degenerated telescopic cascode topology has been chosen for the 866 MHz RFID LNA design due to its current reuse structure and hence it consumes less bias current than the folded cascode. Figure 1 shows the circuit diagram of the proposed RFID LNA. $M_1$ and $M_2$ forms the cascode configuration and their bias currents are driven by $M_3$ and $R_{ref}$. $L_d$, $R_d$, and $C_d$ form the output tank circuit tuned at 866 MHz with an angular frequency bandwidth of $1/(R_d \ast C_d)$. $C_{ac}$ denotes ac-coupling capacitor (one at the source input and the other at the output load) while $C_b$ is an ac grounding capacitor at the gate of the cascoding device $M_2$. $L_i$ provides the inductive source degeneration. An improved PCSNIM technique is adopted here for the telescopic cascode LNA structure optimization. $C_{re}$ is in parallel with $C_{opt}$ of $M_1$ in order to achieve minimum noise figure $F_{min}$ with power constraint and higher unity gain frequency $\omega_T$. Optimal impedance $Z_{opt}$...
for noise match can be derived to achieve the theoretical $F_{\text{min}}$ [5, 6]. The effect of the finite device conductance $g_{ds}(=1/r_0)$ due to the deeply scaled short channel length is included in this design optimization. With regard to the input impedance matching at resonance, we can easily derive

$$Z_{\text{in}} \approx \frac{g_{m1}}{C_t} \frac{L_s g_{m2}}{(g_{ds1} + g_{m2})}, \quad (1)$$

where $C_t$ equals $C_{g1} + C_e$, $g_{ds1}(=1/r_{01})$ is the output conductance of $M_1$, while $g_{m1}$ and $g_{m2}$ are the transconductances of the cascode transistors $M_1$ and $M_2$, respectively. Typically $Z_{\text{in}}$ at resonance changed by 6%–12% due to the inclusion of $g_{ds}$ in (1) as indicated by the plot in Figure 2 of the analytical $Z_{\text{in}}$ with variation in the $r_{01}$ of $M_1$ (being around 450 ohms in this design) from the long channel assumption ($r_{01} \to \infty$). In addition, as shown in Figure 2, the extent of $Z_{\text{in}}$ inaccuracy with long channel assumption also varies

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**Figure 1**: Proposed narrow-band circuit topology for 866 MHz RFID LNA.

**Figure 2**: Variation of the analytical $Z_{\text{in}}$ with finite output impedance ($r_{01}$) of $M_1$ for nanometric CMOS.

**Figure 3**: Analytical and simulated gain-magnitude ($A_V$ in dB) of the RFID LNA.
with the chosen value of \(L_s\), the source inductor. Equation (1) also indicates that for deep nanometric design the finite output conductance of \(M_1\) adds an additional trade-off factor in determining the value of the capacitor \(C_e\) (in \(C_t\)) required for achieving power-constrained input matching. Changing the overdrive and/or the geometry of \(M_2\) (and hence \(g_{m2}\)) in relation to \(g_{ds}\) provides an additional degree of freedom to reach this value of \(C_e\) for input matching. Essentially this trade-off enables a lower value of \(C_e\) and hence a higher \(\omega_T\) in achieving input impedance matching for a given \(g_{m1}\).

In addition, inclusion of the finite \(g_{ds}\) effect provides a more accurate power constrained simultaneous optimization of noise and impedance matching for nanometric CMOS (hence it is termed enhanced PCSNM). The s-domain gain transfer function of the RFID LNA can be determined by first finding the short circuit transconductance (\(g_{m1}\)) and then the open circuit output impedance (\(Z_{\text{OUT}}\)) at the drain of \(M_1\). Hence, we can deduce the voltage gain as

\[
A_v(s) = \left[\frac{g_{m1}}{1 + sC_t(R_s + R_{tg} + R_{Lg} + R_{ct} + sL_s + sL_t)} + (g_{m1} + sC_t)((r_{01}(R_{Lg} + sL_e))/(r_{01} + R_{Lg} + sL_t))\right] * (1/(sC_d + 1/R_d + 1/sL_d)),
\]

where \(R_s\) is the source resistance, \(R_{tg}\) is the series resistance of the gate inductor, \(R_{Lg}\) is the series resistance of the source inductor, and \(R_{ct}\) is an equivalent gate resistance due to the addition of \(C_e\), which is smaller than the original gate resistance \(R_g\) of the transistor \(M_1\). The dB magnitude comparison of the theoretical (analytical) gain with the simulated gain is shown in Figure 3 indicating close agreement between the two. A technique based on determining the short circuit output noise current power at the drain of \(M_1\) was used for the noise analysis. In this method the output load is shorted compared to the method in [5] where the output noise current is determined with

\[
N(f) = 1 + \frac{\delta_1}{5} \frac{\omega^2 C_t^2}{g_{m1}} \left\{ \frac{r_{01}^2}{R_s g_{m1}} \left[ L_s + g_{m1} r_{01} \left( L_t + L_e \right) \right] \right\}^2 + \frac{\omega^2 C_t^2}{\omega C_{d1}^2} \left\{ \frac{1 - \omega^2 C_t(L_e + L_t)}{\omega^2 C_t^2} + \omega^2 C_t^2 R_s^2 \right\} + 2j|c_1| \frac{\omega C_{d1} r_{01}}{R_s \omega^2 C_t^2 (\omega L_s + g_{m1} r_{01}/\omega C_t)^2}
\]

where \(\delta_1\) denotes \(g_{m1} r_{01}^2 R_s - \omega^2 L_s \left[ L_s + g_{m1} r_{01} (L_t + L_e) \right]^2\). It is evident from (3) that inclusion of \(g_{ds} = (1/r_{01})\) provides a more detailed expression and hence a more accurate estimate of the noise factor.

### 3. Simulation and Experimental Results

The LNA (as part T8BTAU) was fabricated using the 130 nm IBM CMOS process available through MOSIS. Figure 4 shows the microphotograph of the 0.571 sq. mm die. The outer diameters of the inductors were, respectively, 240 \(\mu\)m for \(L_d\) and 140 \(\mu\)m for \(L_s\) with 5 \(\mu\)m wide trace of top thick aluminum layer MA and underpass contact copper layer E1. The capacitors \(C_e\) and \(C_d\) were fabricated as MIM (metal-insulator-metal) capacitors, and the resistors were fabricated using p+ poly layer with high-sheet resistance (340 \(\Omega/\square\)). Figure 5 shows the simulated and measured forward power gain, \(S_{21}\) under matched condition [8], indicating reasonably high-Q tuning at 866 MHz with measurement being 4 dB below simulation due to loss along external matching circuit. The measured input reflection coefficient \(S_{11}\) is approximately \(-12\) dB at 866 MHz as shown in Figure 6, while the

\[
\text{Active and Passive Electronic Components}
\]
**Figure 4:** Microphotograph of the fabricated RFID LNA.

**Figure 5:** Forward gain, $S_{21}$ (in dB) of the RFID LNA.

**Figure 6:** Input reflection coefficient, $S_{22}$ (in dB) of the RFID LNA.

**Figure 7:** Output reflection coefficient, $S_{22}$ (in dB) of the RFID LNA.

**Figure 8:** Noise figure ($NF$ in dB) of the RFID LNA.

**Figure 9:** The IIP3 and 1 dB compression points for the UHF RFID LNA.
Table 1: Summary of the 866 MHz UHF RFID LNA performance and comparison with previous UHF LNA designs.

<table>
<thead>
<tr>
<th>Technology (nm)</th>
<th>This work</th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
<th>[5]</th>
<th>[7]</th>
</tr>
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<tbody>
<tr>
<td>S11 (dB)</td>
<td>−12</td>
<td>−11.8</td>
<td>−10</td>
<td>−29</td>
<td>−14</td>
<td>−18</td>
<td>N/A</td>
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<td>S12 (dB)</td>
<td>12</td>
<td>7.2</td>
<td>17.5</td>
<td>12.5</td>
<td>17</td>
<td>12</td>
<td>15</td>
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<tr>
<td>S21 (dB)</td>
<td>−34</td>
<td>−27.4</td>
<td>N/A</td>
<td>−60</td>
<td>−22</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>S22 (dB)</td>
<td>−25</td>
<td>−20</td>
<td>N/A</td>
<td>−33</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
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<tr>
<td>NF (dB)</td>
<td>2.2</td>
<td>4.7</td>
<td>2</td>
<td>0.7</td>
<td>3.4</td>
<td>1.35</td>
<td>2.9</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>−11.5</td>
<td>−1.8</td>
<td>−6</td>
<td>−4</td>
<td>−5.1</td>
<td>−4</td>
<td>N/A</td>
</tr>
<tr>
<td>P1dB (dBm)</td>
<td>−16.1</td>
<td>−9.3</td>
<td>N/A</td>
<td>−9</td>
<td>−23</td>
<td>−15</td>
<td>−15</td>
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<tr>
<td>Pdiss (mW)</td>
<td>0.85</td>
<td>19.5</td>
<td>21.6</td>
<td>3.9</td>
<td>13</td>
<td>2</td>
<td>4.32</td>
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<tr>
<td>Supply Voltage (V)</td>
<td>0.7</td>
<td>2.5</td>
<td>2.7</td>
<td>1.8</td>
<td>2.3</td>
<td>1.25</td>
<td>1.8</td>
</tr>
<tr>
<td>f0 (MHz)</td>
<td>866</td>
<td>900</td>
<td>900</td>
<td>915</td>
<td>900</td>
<td>900</td>
<td>900</td>
</tr>
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</table>

output reflection coefficient \( S_{22} \) is measured to be \( \approx -25 \) dB at 866 MHz as shown in Figure 7. These measurements were carried out using external matching elements and indicates close agreement with the simulation. All measurements include trace and connector losses. Figure 8 shows the comparison of the analytical, simulated and measured \( NF \) spectrum which verifies the close approximation provided by (3) due to the inclusion of the finite \( g_{ds} \) effect. The measured \( NF \) was around 2.2 dB. The IIP3 and the 1-dB compression points were determined to be \(-11.5\) dBm and \(-16.1\) dBm, respectively, as shown in Figure 9. Finally, Table 1 shows a summary of performance comparison of the proposed UHF LNA with other UHF LNA designs indicating the low \( NF \) achieved at sub-mW power.

4. Conclusion

The improved power constrained optimization of an UHF RFID LNA design at 866 MHz considering finite \( g_{ds} \) effects is presented and measurement results are demonstrated. The design achieves very low \( NF \) using only a 0.7 V supply voltage and consuming only 850 \( \mu W \).

References
