

## Research Article

# VM and CM Universal Filters Based on Single DVCCTA

Neeta Pandey<sup>1</sup> and Sajal K. Paul<sup>2</sup>

<sup>1</sup>Department of Electronics and Communications Engineering, Delhi Technological University, Delhi 110042, India

<sup>2</sup>Department of Electronics Engineering, Indian School of Mines, Dhanbad, Jharkhand 826004, India

Correspondence should be addressed to Sajal K. Paul, sajalkpaul@rediffmail.com

Received 15 January 2011; Revised 23 February 2011; Accepted 24 February 2011

Academic Editor: Ching Liang Dai

Copyright © 2011 N. Pandey and S. K. Paul. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

A universal voltage-mode filter (VM) and a current-mode filter (CM) based on recently proposed active building block, namely, differential voltage current conveyor transconductance amplifier (DVCCTA) are proposed. Both the circuits use a single DVCCTA, two capacitors, and a single resistor. The filters enjoy low-sensitivity performance and low component spread and exhibit electronic tunability of filter parameters via bias currents of DVCCTA. SPICE simulation using 0.25  $\mu\text{m}$  TSMC CMOS technology parameters is included to show the workability of the proposed circuits.

## 1. Introduction

The current mode approach for analog signal processing circuits and systems has emerged as an alternate method besides the traditional voltage-mode circuits [1]. The current mode active elements are appropriate to operate with signals in current, voltage, or mixed mode and are gaining acceptance as building blocks in high-performance circuit designs. A number of current mode active elements such as operational transconductance amplifier (OTA) [2], current conveyors (CC) [3–5], differential voltage current conveyor (DVCC) [6], differential difference current conveyor (DDCC) [7], and current feedback operational amplifier (CFOA) [8] are available in the literature.

Recently there is report of some new analog building blocks, such as current-conveyor transconductance amplifier (CCTA) [9, 10], current controlled current conveyor transconductance amplifier (CCCCTA) [11], current difference transconductance amplifier (CDTA) [12], current controlled current difference transconductance amplifier (CCCDDTA) [13], differential voltage current conveyor transconductance amplifier (DVCCTA) [14], and differential voltage current controlled conveyor transconductance amplifier DVCCCTA [15], which may be obtained by cascading of current mode building blocks with TA analog building blocks in monolithic chip for compact implementation of

signal processing circuits and systems. It is well known that DVCC has some advantages [6, 16, 17], specially for applications demanding differential and floating inputs, over CCII or CCCII owing to two high input impedance terminals for DVCC compared to one high input impedance terminal for CCII or CCCII. However, DVCC does not have a powerful inbuilt tuning property in contrast to CCCII.

This paper presents a universal voltage-mode filter and a universal current mode filter based on recently proposed active building block, namely, differential voltage current conveyor transconductance amplifier (DVCCTA) [15] which has DVCC [6] as input block and is followed by transconductance amplifier (TA). The DVCCTA has all the good properties of CCTA or CCCCTA including the possibility of inbuilt tuning of the parameters of the signal processing circuits to be implemented and also all the versatile and special properties of DVCC such as easy implementation of differential and floating input circuits [6, 16, 17]. The proposed circuits have been implemented using 0.25  $\mu\text{m}$  TSMC CMOS technology and are validated through SPICE simulations for their functionality.

## 2. Circuit Description

**2.1. DVCCTA.** The DVCCTA is based on DVCC [6] and consists of differential amplifier, current mirrors, and

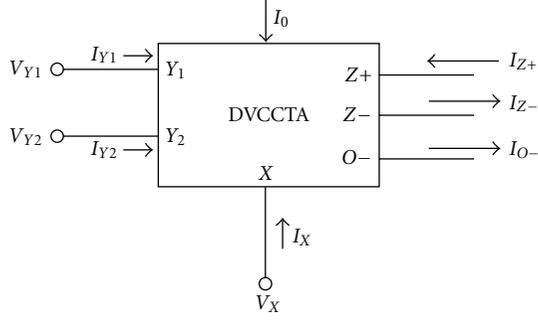


FIGURE 1: Circuit symbol of DVCCTA.

TABLE 1: Aspect ratio of various transistors.

Transistor	Aspect ratio (W( $\mu\text{m}$ )/L( $\mu\text{m}$ ))
$M_1$ – $M_4$	10/0.5
$M_5, M_6$	5/0.5
$M_7, M_8$	27.25/0.5
$M_9, M_{11}, M_{13}, M_{15}, M_{16}$	8.5/0.5
$M_{10}, M_{12}, M_{14}, M_{17}, M_{18}$	44/0.5
$M_{19}, M_{20}, M_{23}$ – $M_{26}$	5/0.5
$M_{21}, M_{22}$	27/0.5

transconductance amplifier (TA). The port relationships of the DVCCTA as shown in Figure 1 can be characterized by the following matrix:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z+} \\ I_{Z-} \\ I_{O-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_{Z+} \\ V_{Z-} \\ V_{O-} \end{bmatrix}, \quad (1)$$

where  $g_m$  is transconductance of the DVCCTA.

The CMOS-based internal circuit of DVCCTA in CMOS is depicted in Figure 2 and is based on internal circuit of DVCC [6] which is followed by a transconductance amplifier. The value of  $g_m$  is obtained as  $2\mu C_{ox}(W/L)I_0$  which can be adjusted by bias current  $I_0$ . The TSMC 0.25  $\mu\text{m}$  CMOS process model parameters and supply voltages of  $V_{DD} = -V_{SS} = 1.25 \text{ V}$  and  $V_{BB} = -0.8 \text{ V}$  are used. The aspect ratio of various transistors for DVCC is given in Table 1.

**2.2. Universal Voltage-Mode Filter.** In this section, a universal voltage-mode (VM) filter is proposed. It uses a single DVCCTA, two capacitors, and a grounded resistor. The proposed universal VM filter is shown in Figure 3. The analysis

TABLE 2: The  $V_{in1}$ ,  $V_{in2}$ , and  $V_{in3}$  values selection for each filter function response.

Filter responses	Inputs			Output
	$V_{in1}$	$V_{in2}$	$V_{in3}$	
Low-pass	1	0	1	$V_{out1}, R = 1/g_m$
High-pass	0	1	0	$V_{out1}$
	1	0	1	$V_{out2}, R = 1/g_m$
Band-pass	0	0	1	$V_{out1}$
	1	0	0	$V_{out2}$
Notch	0	1	0	$V_{out2}$
	1	1	1	$V_{out1}, R = 1/g_m$
All pass	1	1	1	$V_{out1}, R = 2/g_m$

of circuit yields the output voltages at two nodes as follows

$$V_{out1} = \frac{(sC_2 + g_m)V_{in1} + s^2C_1C_2RV_{in2} - sC_2Rg_mV_{in3}}{D(s)}, \quad (2)$$

$$V_{out2} = \frac{-sC_1V_{in1} + sC_1V_{in2} + V_{in3}D(s) - g_mV_{in3}}{D(s)}, \quad (3)$$

where

$$D(s) = s^2C_1C_2R + sC_2 + g_m. \quad (4)$$

Table 2 shows the availability of each filter response and corresponding selection of input voltages  $V_{in1}$ ,  $V_{in2}$ , and  $V_{in3}$ . Thus the proposed structure is a three-input and two output voltage-mode filter. The responses are characterized by pole frequency ( $\omega_0$ ), bandwidth ( $\omega_0/Q_0$ ), and quality factor ( $Q_0$ ) as follows:

$$\omega_0 = \left( \frac{g_m}{RC_1C_2} \right)^{1/2}, \quad \frac{\omega_0}{Q_0} = \frac{1}{RC_1}, \quad Q_0 = \left( \frac{g_mRC_1}{C_2} \right)^{1/2}. \quad (5)$$

It may be noted that the value of  $g_m$  can easily be varied by bias currents  $I_0$ . The resistance  $R$  being a grounded one may easily be implemented as a variable resistance using only two MOSs [17] or replacing DVCCTA along with resistor  $R$  by DVCCCTA [15]. Equation (5) reveals that for high-pass and band-pass responses, the pole frequency ( $\omega_0$ ) and quality factor ( $Q_0$ ) can be adjusted by  $g_m$ , that is, by bias current ( $I_0$ ) of DVCCTA, without disturbing  $\omega_0/Q_0$ . The  $\omega_0$  and  $Q_0$  are orthogonally adjustable with simultaneous adjustment of  $g_m$  and  $R$  such that the product  $g_mR$  remains constant, and the quotient  $g_m/R$  varies and vice versa. Equation (5) also indicates that high values of  $Q$  factor will be obtained from moderate values of ratios of passive components, that is, from low component spread [21]. These ratios can be chosen as  $g_mR = (C_1/C_2) = Q_0$ . Hence, the spread of the component values becomes of the order of  $\sqrt{Q_0}$ . This feature of the filter related to the component spread allows the realization of high  $Q_0$  values more accurately compared to the topologies where the spread of passive components becomes  $Q_0$  or  $Q_0^2$ . It can also be easily evaluated to show that the sensitivities of

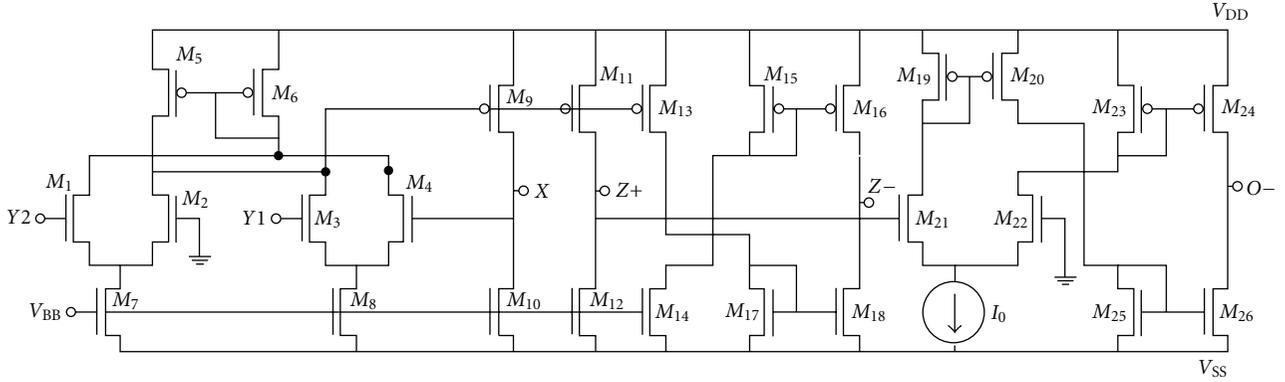


FIGURE 2: Internal circuit of DVCCTA.

TABLE 3: Comparative study of the available similar type of single active element-based VM filters.

Reference	Active element used and number of passive components	Availability of universal filter responses (i.e., low-pass, band-pass, high-pass, notch, and all pass)	No inversion of input voltage	No requirement of gain of input signal such as $2V_{in}$ and $3V_{in}$	Tunability	Simple/no matching condition
[11]	CCCCTA, 2	Yes	No	No	Yes	Yes
[15]	DVCCCTA, 2	No	Yes	Yes	Yes	Yes
[18]	DBTA, 5	No	Yes	Yes	Yes	Yes
Proposed	DVCCTA, 3*	Yes	Yes	Yes	Yes	Yes

\* Passive components may be reduced to 2 by replacing DVCCTA with DVCCCTA.

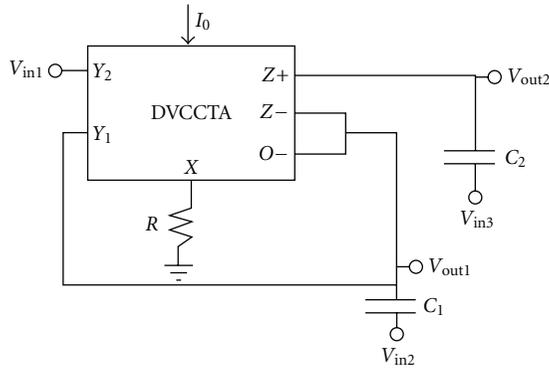


FIGURE 3: Proposed universal voltage-mode filter.

TABLE 4: The  $I_{in1}$ ,  $I_{in2}$ , and  $I_{in3}$  values selection for each filter function response.

Filter responses	Inputs		
	$I_{in1}$	$I_{in2}$	$I_{in3}$
Low-pass	0	1	0
High-pass	1	0	0
Band-pass	0	0	1
All pass	1	1	1
Notch	1	1	0

pole  $\omega_0$  and pole  $Q_0$  are within unity in magnitude. Thus, the proposed structures can be classified as insensitive.

A detailed study of the available similar type of single active element- (such as CCCTA, DBTA, and DVCCCTA) based voltage-mode filters and the proposed one is given in Table 3. It reveals that the topology in [18] uses excessive number of passive components whereas the proposed topology uses one extra passive component, namely, resistor ( $R$ ) in comparison to structures in [11, 15]; however this resistor ( $R$ ) may be eliminated as discussed above. Structures in [15, 18] do not provide for all standard universal filter functions. Topology in [11] needs input signal  $V_{in}$ ,  $-V_{in}$ , and  $-2V_{in}$ ; hence, there is a requirement of additional circuits. Thus the proposed structure possesses all the advantageous features as tabulated in Table 3 without any additional components, rather passive components used may be reduced to 2 by eliminating resistor ( $R$ ) at  $x$  terminal with the use of DVCCCTA instead of DVCCTA.

To verify the functionality of the proposed single DVCCTA-based voltage-mode filter, SPICE simulations have been carried out using TSMC 0.25  $\mu\text{m}$  CMOS process model parameters and supply voltages of  $V_{DD} = -V_{SS} = 1.25\text{ V}$  and  $V_{BB} = -0.8\text{ V}$ . The aspect ratio of various transistors is given in Table 1. The filter is designed for a pole frequency of  $f_0 = 1.59\text{ MHz}$ ,  $Q = 1$ , the component values are found to be  $C = C_1 = C_2 = 100\text{ pF}$ ,  $R = 1\text{ k}\Omega$ , and bias current of DVCCTA equals  $100\text{ }\mu\text{A}$ . Figure 4(a) shows the simulation results for low-pass ( $V_{out1}$ ) and high-pass ( $V_{out2}$ ) filter responses which are available simultaneously for  $V_{in} = V_{in1} = V_{in3}$ ,  $V_{in2} = 0$ . Figure 4(b) shows the simulation results for high-pass ( $V_{out1}$ ) and band-pass ( $V_{out2}$ ) filter responses which are available

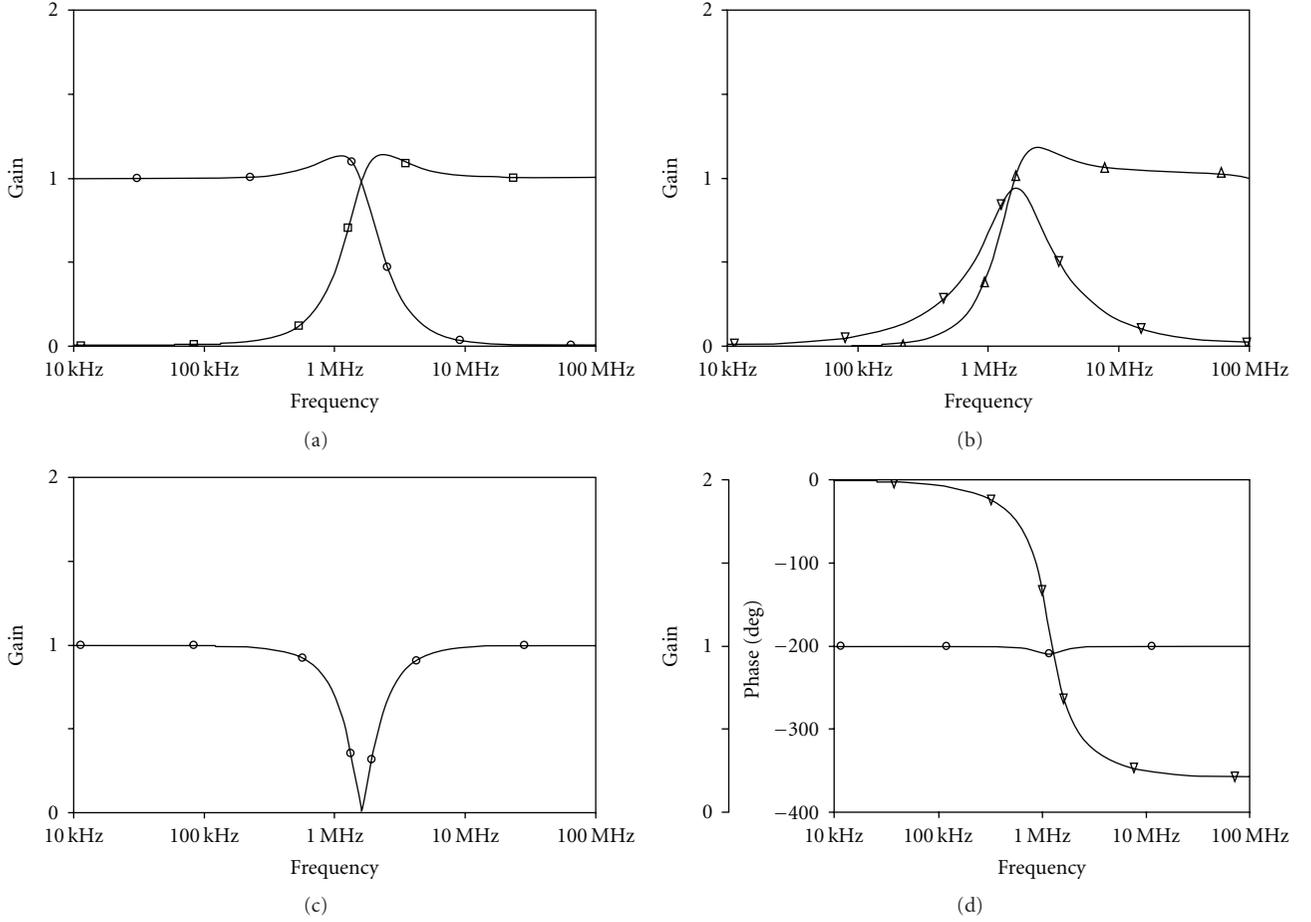


FIGURE 4: Simulated response of the proposed universal voltage-mode filter: (a) high-pass and low-pass, (b) high-pass and band-Pass, (c) notch, (d) all pass.

TABLE 5: Comparative study of the available similar type of single active element based CM filters.

Reference	Active element used and number of passive components	Grounded passive components	Availability of low-pass, band-pass, high-pass, notch, and all pass responses	No requirement of current inversion	No requirement of gain of input signal such as $2I_{in}$ and $3I_{in}$	Output current at high impedance	Tunability	Simple/No matching condition
[11]	CCCCTA, 2	Yes	Yes	Yes	No	Yes	Yes	Yes
[13]	CCCDTA, 2	Yes	Yes	No	Yes	No	Yes	Yes
[19]	CCCDTA, 2	Yes	Yes	Yes	No	Yes	Yes	Yes
[20]	CCCCTA, 2	Yes	No	Yes	Yes	No	Yes	Yes
Proposed	DVCCTA, 3	Yes	Yes	Yes	Yes	Yes	Yes	Yes

simultaneously for  $V_{in} = V_{in2}$ ,  $V_{in1} = V_{in3} = 0$ . Notch and all pass responses are shown in Figures 4(c) and 4(d) with  $V_{in} = V_{in1} = V_{in2} = V_{in3}$  and  $R = 1 \text{ k}\Omega$  and  $2 \text{ k}\Omega$ , respectively.

**2.3. MISO Current Mode Universal Filter.** A multiple-input single-output (MISO) universal current mode (CM) filter is proposed in this section which is obtained by grounding all voltage inputs in Figure 3 and exciting them with current inputs as shown in Figure 5. Here, an extra Z-terminal is

added to obtain  $I_{out}$  at high impedance. It employs a single DVCCTA, two grounded capacitors, and a grounded resistor. Analysis of this circuit gives the output current as follows:

$$I_{out} = \frac{s^2 C_1 C_2 R I_{in1} - s C_2 I_{in3} + g_m I_{in2}}{D(s)}, \quad (6)$$

where

$$D(s) = s^2 C_1 C_2 R + s C_2 + g_m. \quad (7)$$

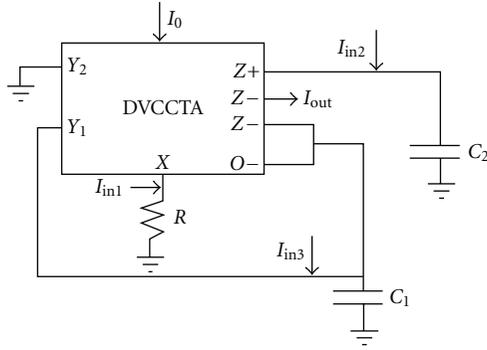


FIGURE 5: Current mode universal filter.

TABLE 6: Component values for orthogonal adjustment of  $f_0$  with  $Q_0$ .

Sl. no.	Bias current ( $\mu\text{A}$ )	Resistance $R$ ( $\text{k}\Omega$ )	$Q_0$	$f_0$ (MHz)
1	50	1.3	1	1.22
2	100	1.0	1	1.59
3	200	0.732	1	2.17
4	400	0.604	1	2.63

TABLE 7: Component values for orthogonal adjustment of  $Q$  with  $f_0$ .

Sl. no.	Bias current ( $\mu\text{A}$ )	Resistance $R$ ( $\text{k}\Omega$ )	$f_0$ (MHz)	$Q_0$
1	50	0.708	1.59	0.7
2	100	1.0	1.59	1.0
3	200	1.259	1.59	1.3
4	400	1.526	1.59	1.5

Table 4 shows the availability of each filter response and corresponding selection of input currents  $I_{in1}$ ,  $I_{in2}$ , and  $I_{in3}$ . Thus, the proposed structure is a three-input single output current mode filter. It may be noted that there is no component matching constraint for obtaining any filter response. The filter parameters are the same as given in (5). The grounded resistance ( $R$ ) may easily be implemented as variable one using only two MOSs [17] for full electronic control of filter parameters. The  $\omega_0$ ,  $Q_0$ , and  $\omega_0/Q_0$  can be orthogonally adjusted the way discussed in Section 2.2.

A detailed study of the available similar type of active element (such as CCCCTA, CCCDTA, and CC-CCTA) based CM filters and the proposed one is given in Table 5. It reveals that although the proposed structure needs one extra resistor, the reported structures in [11, 13, 19, 20] suffer from one or more features. In addition some active elements are required to sense current [13, 20]. Thus structures in [11, 13, 19, 20] will require some extra circuits to compensate the shortcomings in their features in comparison to the proposed one.

The proposed universal MISO current mode filter is validated through SPICE simulations. The circuit of Figure 5 for a pole frequency of  $f_0 = 1.59$  MHz,  $Q = 1$  has been designed with the component values of  $C = C_1 = C_2 = 100$  pF,  $R = 1$  k $\Omega$  and bias current of DVCCTA equals to  $100 \mu\text{A}$ . The low-pass, band-pass, high-pass, notch, and

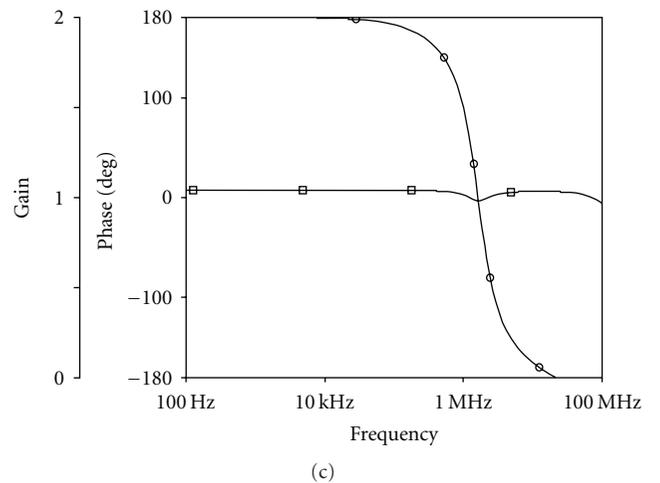
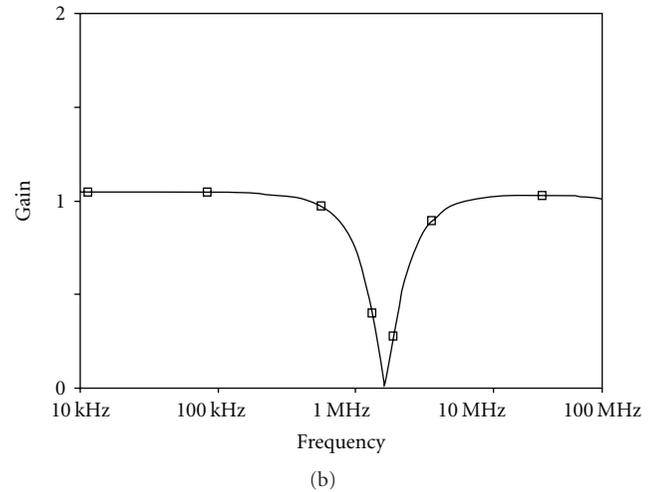
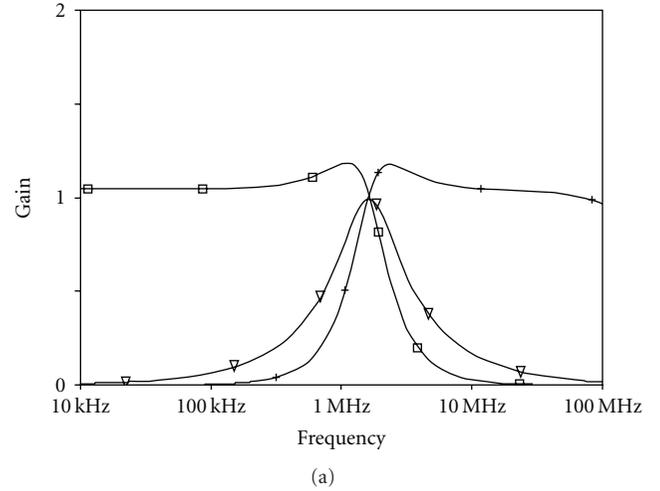


FIGURE 6: Simulated response of the proposed current mode universal filter: (a) high-pass, low-pass and band-pass, (b) notch, (c) all pass.

all pass responses are shown in Figure 6 which show close agreement with the theoretical formation.

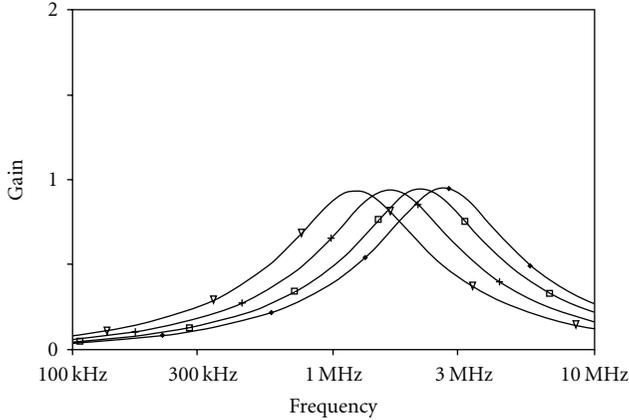


FIGURE 7: Response of band-pass filter for constant  $Q_0 = 1$  and different  $f_0$ .

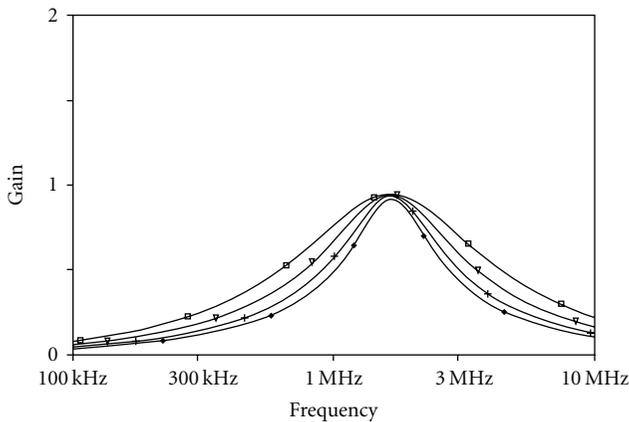


FIGURE 8: Response of band-pass filter for constant  $f_0 = 1.59$  MHz and different  $Q_0$ .

The orthogonal adjustment of  $f_0$  with  $Q_0$  is depicted in Figure 7. This is designed for a constant value of  $Q_0 = 1$  with  $C_1 = C_2 = 100$  pF for different values of  $f_0$  as given in Table 6. Figure 8 shows orthogonal adjustment of  $Q_0$  with  $f_0 = 1.59$  MHz. The values of  $Q_0$  for constant value of  $f_0$  as obtained with  $C_1 = C_2 = 100$  pF and other component values are listed in Table 7.

The simulations have also been carried out to study the limits on tunability. Figure 9 shows the tuning of pole frequency ( $f_0$ ) of the band-pass filter with bias current ( $I_0$ ) (i.e., with  $g_m$ ) for  $C_1 = C_2 = 100$  pF and  $R = 1$  k $\Omega$ . It may be noted that the tuning of pole frequency ( $f_0$ ) is adequate up to about  $200 \mu\text{A}$  and then the tuning is slow till  $450 \mu\text{A}$ . The decreases in pole frequency for larger bias currents than  $450 \mu\text{A}$  are due to transistors ( $M_{21}$ ,  $M_{22}$ ) entering in linear region of operation from saturation region.

### 3. Conclusion

New universal voltage-mode and current-mode filters using a single DVCCTA have been presented. The circuits use one DVCCTA, two capacitors, and a resistor for realization.

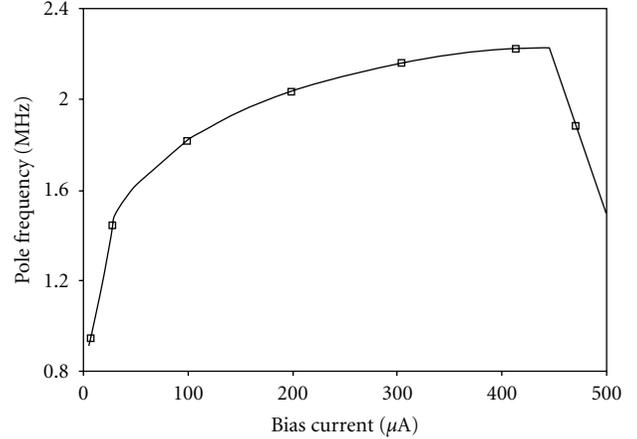


FIGURE 9: Tunability of pole frequency with bias current.

The resistor being grounded may easily be implemented as a variable one using only two MOSs [17]. The resistor may be eliminated by replacing DVCCTA with DVCCCTA in the case of VM filter. The simulation results verify the theory. The salient features of the proposed circuits are as follows: they employ a single DVCCTA, low sensitivity performance, electronic tunability of both  $\omega_0$  and  $\omega_0/Q_0$  and  $\omega_0$  and  $Q_0$ , high output impedance for CM filter, which are suitable for cascading, and low component spread for high- $Q$  application.

### References

- [1] G. Ferri and N. C. Guerrini, *Low-Voltage Low-Power CMOS Current Conveyors*, Kluwer Academic Publishers, London, UK, 2003.
- [2] R. L. Geiger and E. Sanchez-Sinencio, "Active filter design using operational transconductance amplifiers: a tutorial," *IEEE Circuits and Devices Magazine*, vol. 1, no. 2, pp. 20–32, 1985.
- [3] A. Sedra and K. C. Smith, "A second-generation current conveyor and its applications," *IEEE Transactions on Circuit Theory*, vol. 17, no. 1, pp. 132–134, 1970.
- [4] A. Fabre, O. Saaid, F. Wiest, and C. Boucheron, "High frequency applications based on a new current controlled conveyor," *IEEE Transactions on Circuit and Systems I*, vol. 43, no. 2, pp. 82–91, 1996.
- [5] I. A. Awad and A. M. Soliman, "Inverting second generation current conveyors: the missing building blocks, CMOS realizations and applications," *International Journal of Electronics*, vol. 86, no. 4, pp. 413–432, 1999.
- [6] H. O. Elwan and A. M. Soliman, "Novel CMOS differential voltage current conveyor and its applications," *IEE Proceedings: Circuits Devices Systems*, vol. 144, no. 3, pp. 195–200, 1997.
- [7] W. Chiu, S. I. Liu, H. W. Tsao, and J. J. Chen, "CMOS differential difference current conveyors and their applications," *IEE Proceedings: Circuits Devices Systems*, vol. 143, no. 2, pp. 91–96, 1996.
- [8] C. Toumazou and A. Payne, "Current feedback op-amps: a blessing in disguise?" *IEEE Circuits and Devices Magazine*, vol. 10, no. 1, pp. 34–37, 1994.

- [9] R. Prokop and V. Musil, "CCTA—a new modern circuit block and its internal realization," in *Proceedings of International Conference on Electronic Devices and Systems (IMAPSCZ '05)*, pp. 89–93, Brno, Czech Republic, 2005.
- [10] W. Jaikla, P. Silapan, C. Chanapromma, and M. Siripruchyanun, "Practical implementation of CCTA based on commercial CCII and OTA," in *Proceedings of the International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS '09)*, pp. 1–4, Bangkok, Thailand, February 2009.
- [11] M. Siripruchyanun and W. Jaikla, "Current controlled current conveyor transconductance amplifier (CCCCTA): a building block for analog signal processing," *Electrical Engineering*, vol. 90, no. 6, pp. 443–453, 2008.
- [12] D. Birolek, "CDTA—building block for current-mode analog signal processing," in *Proceedings of the European Conference on Circuit Theory and Design (ECCTD '03)*, pp. 397–400, Krakow, Poland, 2003.
- [13] M. Siripruchyanun and W. Jaikla, "CMOS current-controlled current differencing transconductance amplifier and applications to analog signal processing," *AEU—International Journal of Electronics and Communications*, vol. 62, no. 4, pp. 277–287, 2008.
- [14] A. Jantakun, N. Pisutthipong, and M. Siripruchyanun, "A synthesis of temperature insensitive/electronically controllable floating simulators based on DV-CCTAs," in *Proceedings of the 6th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON '09)*, pp. 560–563, May 2009.
- [15] W. Jaikla, M. Siripruchyanun, and A. Lahiri, "Resistorless dual-mode quadrature sinusoidal oscillator using a single active building block," *Microelectronics Journal*, vol. 42, no. 1, pp. 135–140, 2010.
- [16] M. A. Ibrahim, S. Minaei, and H. Kuntman, "A 22.5 MHz current-mode KHN-biquad using differential voltage current conveyor and grounded passive elements," *AEU—International Journal of Electronics and Communications*, vol. 59, no. 5, pp. 311–318, 2005.
- [17] T. M. Hassan and S. A. Mahmoud, "New CMOS DVCC realization and applications to instrumentation amplifier and active-RC filters," *AEU—International Journal of Electronics and Communications*, vol. 64, no. 1, pp. 47–55, 2010.
- [18] N. Herencsar, K. Vrba, J. Koton, and I. Lattenberg, "The conception of differential-input buffered and transconductance amplifier (DBTA) and its application," *IEICE Electronics Express*, vol. 6, no. 6, pp. 329–334, 2009.
- [19] M. Siripruchyanun and W. Jaikla, "Electronically controllable current-mode universal biquad filter using single DO-CCCDTA," *Circuits, Systems, and Signal Processing*, vol. 27, no. 1, pp. 113–122, 2008.
- [20] S. Mangkalakeeree, D. Duangmalai, and M. Siripruchyanun, "Current-mode KHN filter using single CCCCTA," in *Proceedings of the 7th PSU Engineering Conference*, pp. 306–309, Songkla, Thailand, May 2009.
- [21] S. I. Liu, "High input impedance filters with low component spread using current-feedback amplifiers," *Electronics Letters*, vol. 31, no. 13, pp. 1042–1043, 1995.



**Hindawi**

Submit your manuscripts at  
<http://www.hindawi.com>

