Research Article

Novel Power Reduction Technique for ReRAM with Automatic Avoidance Circuit for Wasteful Overwrite

Takaya Handa,1 Yuhei Yoshimoto,1 Kazuya Nakayama,2 and Akio Kitagawa1

1 School of Electrical and Computer Engineering, College of Science and Engineering, Kanazawa University, Kakuma, Kanazawa 920-1192, Japan
2 School of Health Sciences, College of Medical, Pharmaceutical and Health Sciences, Kanazawa University, 5-11-80 Kodatsuno, Kanazawa 920–0942, Japan

Correspondence should be addressed to Kazuya Nakayama, knaka@kenroku.kanazawa-u.ac.jp

Received 18 October 2011; Accepted 5 January 2012

Academic Editor: Daisaburo Takashima

Copyright © 2012 Takaya Handa et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Low-power operations can be great advantageous for ReRAM devices. However, wasteful overwriting such as the SET operation to low-resistance state (LRS) device and the RESET operation to high-resistance state (HRS) device causes not only an increase in power but also the degradation of the write cycles due to repeatedly rewriting. Thus, in this paper, we proposed a novel automatic avoidance circuit for dealing with wasteful overwriting that uses a sense amplifier and estimated the energy consumption reduction rate by conducting a circuit simulation. As a result, this circuit helped to reliably avoid the wasteful overwriting operation to reduce about 99% and 97% of wasteful energy using VSRC and CSRC, respectively.

1. Introduction

Resistance random access memory (ReRAM) has been widely expected for use as the next generation nonvolatile memory because of its superior characteristics, such as low voltage operation, high-speed performance, and low power. ReRAM has a Metal-Insulator-Metal (MIM) structure in which the transition metal oxide is sandwiched between two electrodes as a storage element. This device has two switching modes: (i) unipolar switching in which the device depends on the pulse width and amplitude of the applied voltage and (ii) bipolar switching in which the device depends on the polar character [1]. In this paper, we used a bipolar switching device that made the best use of this proposed circuit. Figure 1 shows (a) the structure of the ReRAM device and (b) the definition of the SET and RESET operations.

In this research, SET is defined as an operation conducted to change from HRS to LRS, and RESET is an operation to change from LRS to HRS. ReRAM has the great advantage of being a low power device. However, in order to have this advantage, not only the necessary device characteristics but also peripheral circuits, such as read/write circuits, are needed. On one hand, wasteful overwrite operations such as SET for LRS devices or RESET for HRS not only increase the power consumption but also degrade the write cycles [2]. One solution is for the circuit to judge whether or not the device needs to be written after the circuit initially reads the resistance state like verifying operation in conventional NAND flash memory [3]. However, in this way, both the power consumption and processing time increase because an additional full read operation is required for the write operation, as shown in Figure 2(a). Therefore, in this paper, we propose a new circuit that can automatically judge whether or not the circuit needs to write by using the avoidance function of the wasteful overwrite to reduce the wasteful power consumption by improving the conventional sense amplifier [4], as shown in Figure 2(b). In this proposed scheme, write operation can be conducted during read operation, so full read operation is not necessary, and this circuit has some advantage in aspects of speed and power. And also this scheme has merits of using the result of sense amplifier to write operation and adding the “write function” to conventional “read circuit,” and so read and write circuit needs not to be separated and achieving wasteful overwrite avoidance with added only 4 MOSFET against conventional sense amplifier.
This paper is organized as follows. An explanation about the circuit configuration and the principle of the operations are presented in Section 2. A Verilog-A empirical model of a ReRAM device and our simulation results are presented in Section 3. The conclusion is summarized in Section 4.

2. Circuit Structures

We propose two write circuits to avoid the wasteful overwrite that are composed of a voltage sense amplifier (VSA) and a current sense amplifier (CSA) because we compare the reduction power between these two circuits. These circuits have both functions, as a write decision circuit and a sense amplifier [4]. Here, we call these circuits a voltage sense rewriting circuit (VSRC) and a current sense rewriting circuit (CSRC).

2.1. Circuit Structure and Operations

(1) VSRC. Figure 3(a) shows the schematic of the VSRC, and 3(b) shows the symbol. The read and write current paths are drawn as solid and dashed lines, respectively.
Figure 4 shows a timing diagram for the VSRC. Operation of the VSRC is divided into three phases: (i) cell reading, (ii) amplification, and (iii) precharge.

(i) In the cell-reading phase, the Vout and Vout_ref of the VSRC are equalized. The input voltage dependent on the state of the ReRAM device is temporarily applied to gates of M1 and M2.

(ii) In the amplification phase, both read and write can be operated by charging Cin. The read process is operated through the solid line shown in Figure 2. In this phase, SL is set to the read voltage (Vread), rw to “H” (vdd), and se_control to “L” (gnd), and the potential difference between Vin and Vin_ref in the equalization phase is amplified and outputted in the latching part. Meanwhile, the write process is operated through the dashed line, and rw is set to “L”, and se_control is set to “H”. Here, SL is asserted to “L” or “H” in accordance with the SET or RESET operations, respectively.

(iii) In the precharge phase, the power supply of the VSRC is stopped because M8 is OFF in synchronization with the rising edge of the re signal (power saving mode).
flows through the memory cells depending on the ON resistance of M5, M6, and M8, so the size of MOSFET must be carefully decided on to prevent any disturbance.

(ii) In the amplification phase, the rw signal is set to “L” in the read operation and “H” in the write operation. By asserting se to “L”, M7 is OFF, and the current difference between the accessed cell and the reference cell is amplified and latched. If a ReRAM device is in HRS, the Vgs of M3 is smaller than that of M4. Thus, Vout is asserted to “H”, and Vout_ref is asserted to “L” because the discharge capacity of the Vout node is lower than that of Vout_ref. On the other hand, SL is fixed to “L” in the SET operation and asserted to “H” in the RESET operation.

Figure 4: Timing diagram for VSRC operation.

Here, as shown in Figure 4, the re signal is asserted to “L” just before the end of cell-reading phase to suppress wasteful DC current in the sense amplifier. Therefore, DC current that flows through sense amplifier is minimized even at long-time cell reading due to long bit-line lengths when large array size is adopted.

(2) CSRC. The schematic of the CSRC is shown in Figure 5. In this circuit, the rw signal is used to control the switching between read and write operations. The CSRC operations are also divided into the (i) cell reading and (ii) amplification phase in both the read and write operations. Figure 6 shows a timing diagram of the CSRC. In the initial condition, control signals such as se and rw are set to “H”, and re is set to “L”.

(i) In the cell reading phase, the control signals are the same for both the read and write operations. By setting re to “H”, the precharge of the current path for the read operation is started. Both the se and rw signals are set to “H” and SL is set to “L”. Output nodes Vout and Vout_ref are equalized to vdd/2, where the equalized voltage can be calibrated by optimizing the size of M3 and M4. Here, the precharge current flows through the memory cells depending on the ON resistance state and BL voltage is summarized as follows:

(i) SET Operation:

ReRAM (LRS) < Rref ⇒ SL → “L”, BL → “L”
(Set current does not flow: avoidance)

ReRAM (HRS) > Rref ⇒ SL → “L”, BL → “H”
(Set current flows through ReRAM: write).

(i) RESET Operation:

ReRAM (LRS) < Rref ⇒ SL → “L”, BL → “L”
(RESET current flows through ReRAM: write)

ReRAM (HRS) > Rref ⇒ SL → “H”, BL → “H”
(RESET current does not flow: avoidance).
3. Simulation

3.1. Simulation Condition. The device characteristics of the ReRAM used in this paper and the simulation conditions are listed in Tables 1 and 2, respectively [4].

3.2. Verilog-A Modeling. The behavioral device model of ReRAM was developed using a Verilog-A based on the characteristics in Table 1. In this paper, we described the transient response of the bipolar operation of a ReRAM device. Figure 8 shows the simulation results of the transient response in the write and read operations using only the Verilog-A model.

Using this Verilog-A model makes it possible to simulate more a realistic circuit behavior while taking the phenomenon typically found in ReRAM devices such as sharp resistance switching in the write operation into consideration.

3.3. Simulation Circuit Structure. The circuit structure for our simulation is shown in Figure 9. Here, we omitted the description of the other signals, such as the se and re signals. Here, peripheral control circuits, such as address decoding and timing generation aren’t included in our simulation condition.
The read/write sequence was given as (a) READ→SET→READ→SET→READ for an HRS device and (b) READ→RESET→READ→RESET→READ for an LRS device. We conducted a simulation with conventional circuit and proposed circuit as shown in Figure 10. Here, we used the reversed logic-VSRC and CSRC as conventional circuit. Reversed logic-VSRC and CSRC was designed to overwrite intentionally as RESET operation to HRS device and SET operation to LRS device by replacing Vout with Vout_ref in VSRC and CSRC as shown in Figure 3 and Figure 5, respectively. Therefore, we can compare the energy consumption using conventional and proposed circuit.

### Table 1: ReRAM device characteristics.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-resistance value</td>
<td>80 kΩ</td>
</tr>
<tr>
<td>Low-resistance value</td>
<td>20 kΩ</td>
</tr>
<tr>
<td>SET transition time [1]</td>
<td>~50 ns</td>
</tr>
<tr>
<td>RESET transition time</td>
<td>~50 ns</td>
</tr>
<tr>
<td>SET voltage</td>
<td>More than 2.2 V</td>
</tr>
<tr>
<td>RESET voltage</td>
<td>Less than −1.4 V</td>
</tr>
<tr>
<td>Read voltage</td>
<td>Less than 0.5 V</td>
</tr>
</tbody>
</table>

### Table 2: Simulation condition.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulator</td>
<td>HSPICE</td>
</tr>
<tr>
<td>Fabrication process</td>
<td>180-nm CMOS</td>
</tr>
<tr>
<td>Power supply</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Temperature</td>
<td>27°C</td>
</tr>
<tr>
<td>Amplification time</td>
<td>70 ns</td>
</tr>
<tr>
<td>Bit-line capacitance (Cb)</td>
<td>200 fF</td>
</tr>
</tbody>
</table>

### 3.5. Considerations for Power Consumption.

From the simulation results shown in Figure 11, the amount of power consumption per one ReRAM device that the VSRC and CSRC can reduce is shown in Figure 12.

In Figure 12(a) with no avoidance, RESET voltage is applied to ReRAM and consumes wasteful power (Area 1). On the other hand, in Figure 12(b) with avoidance, RESET voltage is not applied to ReRAM because BL voltage is changed dynamically depending on the current resistance state, and, so, the voltage difference between ReRAM becomes zero. Here, we defined the power reduction ratio as

\[
\text{reduction\_ratio} = \frac{\text{Energy(Area1)} - \text{Energy(Area2)}}{\text{Energy(Area1)}}, \quad (1)
\]

where Energy(Area1) is an energy caused by wasteful overwrite with no avoidance, and Energy(Area2) is an overhead energy caused by using proposed circuit.

We evaluated the reduction ratio of the consumed energy using the proposed circuit (w/avoidance) against the conventional wasteful overwrite energy (w/o avoidance).

We calculated the energy reduction ratio for the SET→SET and RESET→RESET operation sequences, as shown in Figure 13. Table 3 shows each energy consumption and reduction ratio in RESET and SET operation. Here, Energy(Area1) and Energy(Area2) in Figure 12 correspond to 3405 [fJ] and 135 [fJ] in Table 3, respectively. We achieved almost a 90% power reduction using the proposed circuit as shown in Table 3. Optimizing the timing of the se\_control and SL makes it possible to reduce the power consumption of the CSRC although the power reduction ratio of the CSRC was smaller than that of the VSRC. Here, the speed overhead using proposed circuit can be controlled to only 1.1
times increase of time compared to conventional one because equalization time (10 ns) is 7 times smaller than amplification time (70 ns).

Generally, the time constant of the BL load depends on the resistances of ReRAM devices, the parasitic capacitances of the cell transistors, the distributed wire resistance, capacitance of BL, and the array size. These variations are solved by carefully controlling the timing of sensing (cell reading time). In practice, the sensing behaviors of these circuits depend on the data patterns stored in the memory cell array because the different data patterns on a column cause various BL loads. The waveform of the BL voltage is fluctuated within 2% for any data pattern in the condition that assumes 1024 cell per bitline.

The power reduction ratio in Table 3 was estimated for the consumed energy only in ReRAM array including activated memory cells and word-line/bit-line voltage swing. The energy consumption in the sense amplifier is mainly due to the DC current through the transistor M8 in VSRC and CSRC, and the DC current path is formed when both re and se signals are asserted during the cell-reading phase. Assuming that the period of the DC current flow is 10 ns, the approximate energy reduction ratio considering DC current consumed in sense amplifier is about 84% for the VSRC and CSRC though we haven’t done complete optimization.
Figure 11: Simulation results.
of this circuit in consideration of the minimum DC current in the sense amplifier. The DC current can be suppressed by further optimization of the circuit and the timing of re signal.

4. Conclusion

We proposed an automatic avoidance circuit of the wasteful overwrite and evaluated the proposed circuit. As a result,
Figure 13: Simulation results.
we achieved about a 99% and a 97% energy reduction ratio using the VSRC and CSRC, respectively.

Acknowledgments

This work was supported by VLSI Design and Educational Center (VDEC), the University of Tokyo in collaboration with Cadence Corporation and Mentor Graphics, Inc. The VLSI chip in this study has been fabricated in the chip fabrication program of VDEC, the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation. This work was also supported by Grant-in-Aid for Scientific Research (C) (20510116, 23560391), Grant-in-Aid for Exploratory Research (23651136) of Japan Society for the Promotion of Science (JSPS), and Adaptable & Seamless Technology Transfer Program through Target-driven R&D (AS2121327) of Japan Science and Technology Agency (JST).

References

Submit your manuscripts at
http://www.hindawi.com