

## Research Article

# Modeling of Current-Voltage Characteristics of the Photoactivated Device Based on SOI Technology

**Doron Abraham, Avraham Chelly, David Elbaz, Shimron Schiff, Michah Nabozny, and Zeev Zalevsky**

*Faculty of Engineering, Bar Ilan University, 52900 Ramat Gan, Israel*

Correspondence should be addressed to Zeev Zalevsky, zalevsz@biu.ac.il

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An analytical model of the silicon on insulator photoactivated modulator (SOI-PAM) device is presented in order to describe the concept of this novel device in which the information is electronic while the modulation command is optical. The model, relying on the classic Shockley's analysis, is simple and useful for analyzing and synthesizing the voltage-current relations of the device at low drain voltage. Analytical expressions were derived for the output current as function of the input drain and gate voltages with a parameterization of the physical values such as the doping concentrations, channel and oxide thicknesses, and the optical control energy. A prototype SOI-PAM device having an area of  $4\ \mu\text{m} \times 3\ \mu\text{m}$  with known parameters is used to experimentally validate and support the model. Finally, the model allows the understanding of the physical mechanisms inside the device for both dark and under illumination conditions, and it will be used to optimize and to find the performance limits of the device.

## 1. Introduction

Silicon-based nanophotonic devices have attracted appreciable attention and effort because of their potential applications in silicon-integrated circuits. Although silicon may be not the ideal platform for optical devices, the usage of silicon is mandatory for the generation of optoelectronic integrated circuitry. The quality of commercial silicon on insulator (SOI) wafers driven by the microelectronics industry still continues to improve while the cost continues to decrease. Moreover, as previously mentioned the compatibility with silicon integrated circuits manufacturing is an important reason for this interest in silicon photonics [1].

The optical capabilities are used to overcome some limits of the non optical devices. Those capabilities are high propagation velocity, reduced cross talks and absence of noise coupled by electrical inductance and capacitance [2–4]. Such devices can operate at very low operational power and have parallel processing capabilities [5, 6].

In this paper, we present the first analytic model of the previously presented hybrid optical-electrical device, the *silicon on insulator photo-activated modulator* (SOI-PAM) [7]. As deduced from its name, the device is controlled by optical command. like a junction field effect transistor (JFET), the information current flows between two terminals (source and drain) in a silicon channel. The device concept relies on the fact that the thickness of depletion layer in the channel, which affects the information current, can be controlled through external illumination and not only by applying a gate voltage.

The model was developed for the linear domain of the channel (drain to source) current voltage characteristic and adapted to experimental measurements.

In Section 2, we describe the operation principle of the SOIPAM device. In Section 3, we present the general assumptions for the model. In Section 4, we derive the analytical model in the depletion mode and in Section 5, we develop unified lineal model and extract its parameters. Section 6 concludes the paper.

## 2. SOI-PAM Device

The device is based on a structure consisting of a thin n-type silicon layer (30 nm) on insulator above p-type substrate (SOI-bonded wafer) [8]. The n-type layer was obtained by compensation of the original low-doped p-type silicon layer using an ion implantation of phosphorus.

As depicted in Figure 1, the channel is delimited by source and drain ohmic contacts made of  $n^+$  doped polysilicon. The length of the channel is about few microns as fabricated in the prototype version of the device [8]. The information channel is insulated from the p-type substrate by a buried oxide layer having a thickness  $t_{ox}$  of 150 nm (SOI wafer). The device is insulated from the surrounding devices by a thicker thermal field oxide.

In principle, when a given negative gate potential  $V_G$  is applied to the bottom side of the p-type substrate, a negatively charged depletion layer appears under the buried oxide layer. As a result, a positively charged depletion layer appears inside the n-type channel. Since the n-type doping level (donors concentration of  $N_d$  of about  $10^{17} \text{ cm}^{-3}$ ) of the channel is designed to be larger than the p-type substrate (acceptors concentration  $N_a$  of  $10^{15} \text{ cm}^{-3}$ ), the thickness of the depletion layer in the n-type area is narrower than the depletion layer in the p-type region. Moreover, the device is designed in such a way that, in dark conditions, the depletion layer in the channel is smaller than the channel thickness so the device is partially depleted and can be considered as normally on, that is, moderately conducting under dark condition and zero gate voltage. Note that the gate voltage should be applied with a sufficiently high frequency (few kHz) or swept at a sufficient rate in order to bring the substrate into the “deep” depletion mode and consequently to avoid the inversion of the channel.

If a short pulse of a visible laser illuminates the area under the oxide layer (oblique illumination), the photo generated electrons will accumulate at the bottom silicon-oxide interface and consequently increase the positively charged depletion layer in the channel. With a pulse of sufficient energy, the channel will be cut off. In a future version of the device, a sweeping potential will be added so that the modulation will be limited by the drift time of the photogenerated carriers in a micrometric region rather than by the time consuming recombination process. Assuming a saturation velocity of  $10^7 \text{ cm/s}$  and a one micron sweeping length, the drift time is expected to be as small as 10 ps, that is, achievable modulation rates can be as high as 100 GHz.

## 3. General Assumptions

In a similar way used for other field effect devices, the 2D-Poisson's equation will be solved in one dimension (which is the  $y$  axis that is being perpendicular to the plane of the Si-SiO<sub>2</sub>-Si interface) by assuming the Shockley's Gradual Channel Approximation (GCA) [9]. For small drain voltage values, it is reasonable to assume that the electric field varies more rapidly in the  $y$  direction than the variations of the lateral field along the channel direction ( $x$  axis) due to the

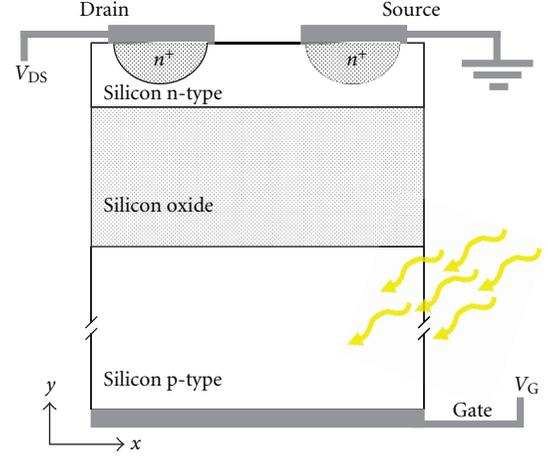


FIGURE 1: Schematic cross section of the SOI-PAM device. Like in a field effect device the information current flows through silicon channel that is limited by two terminals (source and drain). The source is connected to ground. Gate voltage  $V_G$  is applied at sufficient rate to bring the substrate into its deep depletion mode. An oblique illumination generates charges in the p-type substrate.

large ratio between the channel length and the buried oxide thickness.

The geometry of the device is sketched in Figure 1. The channel, having a length  $L$  of  $3 \mu\text{m}$ , is assumed to be along the  $x$  direction. The thickness of the channel  $t_n$  is 30 nm and is measured in the  $y$  direction. The width of the device  $W$  is  $4 \mu\text{m}$  measured in the  $z$  direction. The channel potential  $V(x)$  is a function of the distance  $x$  along the channel.

In order to derive an expression for the drain current, it is useful to make some simplifying assumptions.

- (1) All the regions of the device are assumed to be uniformly doped.
- (2) The current flow occurs only within the nondepleted (neutral) portion of the channel.
- (3) The mobility of the carriers is not drain voltage dependent (low field mobility is mainly gate voltage dependent).
- (4) The oxide is an ideal insulator such the oxide and interface charges are negligible.
- (5) The contact series resistances are negligible.
- (6) The generation current is negligible.

## 4. Derivation of the Analytic Model for the Depletion Mode

The Poisson's equation is solved separately for each region of the SOI-PAM device structure composed by a p-n depleted junction separated by an oxide layer. As supposed in the GCA approximation, the channel voltage  $V(x)$  induced by the drain-source bias  $V_{DS}$  is added to the applied negative gate voltage  $V_{GS}$  according to the following equation:

$$V_n + V_p + V_{ox} = V_{FB} - V_{GS} + V(x), \quad (1)$$

where  $V_n, V_p, V_{ox}$  are the potentials in n-type depleted region, p-type depleted region and the oxide layer respectively.  $V_{FB}$  is the Flat Band (FB) bias of the SOI-PAM device that includes the built-in bias of the p-n junction and the work function differences between the contact metals and the silicon regions (substrate and channel, resp.). Oxide and interface charges are considered to be negligible. Finally, we get from (1) that:

$$\frac{qN_d d_n^2}{2\epsilon_s} + \frac{qN_a d_p^2}{2\epsilon_s} + \frac{qN_a d_p t_{ox}}{\epsilon_{ox}} = V_{FB} - V_{GS} + V(x), \quad (2)$$

where  $d_n$  and  $d_p$  are the depletion thicknesses of the n and p-type areas respectively.  $\epsilon_{ox}, \epsilon_s$  are the dielectric permittivities of silicon oxide and silicon, respectively. Then, the charge neutrality of the device is expressed in the following equation:

$$N_d d_n = N_a d_p. \quad (3)$$

The channel depletion layer thickness,  $d_n(x)$ , can be solved accordingly:

$$d_n(x) = \alpha_0 t_n \left( \sqrt{1 + \frac{V_{FB} - V_{GS} + V(x)}{\phi_0}} - 1 \right), \quad (4)$$

where  $\alpha_0$  is defined as the oxide coupling factor (dimensionless):

$$\alpha_0 = \left( \frac{N_a}{N_a + N_d} \right) \frac{\epsilon_s t_{ox}}{\epsilon_{ox} t_n} = 0.148 \quad (5)$$

and  $\phi_0$  is the oxide coupling voltage defined as:

$$\phi_0 = \left( \frac{N_a N_d}{N_a + N_d} \right) \left( \frac{\epsilon_s t_{ox}}{\epsilon_{ox}} \right)^2 \frac{q}{2\epsilon_s} = 0.155 \text{ V}. \quad (6)$$

We can easily check that the depleted  $d_n$  is zero for  $V_{GS}$  equals  $V_{FB}$ , that is, the flat band voltage is the transition between accumulation and depletion modes as for MOS capacitor.

The maximum value of  $d_n(x)$  equals to  $t_n$  when the corresponding gate voltage  $V_G$ , equals to the threshold (or cut off) voltage  $V_T$  when taken without drain voltage ( $V(x) = 0$ ). Then from (4) we obtain:

$$V_T = V_G(d_n(x) = t_n)|_{V(x)=0} = V_{FB} - \frac{\phi_0}{\alpha_0^2} (1 + 2\alpha_0) \quad (7)$$

$$= V_{FB} - \phi_{PO} (1 + 2\alpha_0) = V_{FB} - 9.170 \text{ V},$$

where  $\phi_{PO}$  is the internal pinch off voltage for the device without oxide and at zero drain voltage as following:

$$\phi_{PO} \equiv \frac{\phi_0}{\alpha_0^2} = N_d \left( 1 + \frac{N_d}{N_a} \right) \frac{q}{2\epsilon_s} t_n^2 = 7.076 \text{ V}. \quad (8)$$

Assuming that the drain current  $I_{DS}$ , flowing in the neutral upper part of the depleted channel, is constant along the  $x$  axis, we can write that:

$$I_{DS} = qN_D W \mu_n [t_n - d_n(x)] \frac{dV}{dx}. \quad (9)$$

By integrating the expression for  $V(x)$  between 0 and  $V_{DS}$  we get the oxide-modified Shockley's equation for drain current (as far as  $V_{DS} < V_{GS} - V_T$ ):

$$I_{DS} = g_{\max} \left[ \frac{V_{DS}(1 + \alpha_0)}{3\sqrt{\phi_{PO}}} \left\{ \frac{[\phi_0 + V_{FB} - V_{GS}]^{3/2}}{-[\phi_0 + V_{FB} - V_{GS} + V_{DS}]^{3/2}} \right\} \right] \quad (10)$$

where  $g_{\max}$  is the maximum value of the conductance (for undepleted channel).

$$g_{\max} = \frac{qN_d W \mu_n t_n}{L}. \quad (11)$$

One can then derive the channel conductance  $g_d$  of the SOI-PAM device from (10):

$$g_d = \frac{\partial I_{DS}}{\partial V_{DS}} = g_{\max} \left[ 1 + \alpha_0 - \sqrt{\frac{V_{FB} + \phi_0 - V_{GS} + V_{DS}}{\phi_{PO}}} \right]. \quad (12)$$

In the depleted case (where  $V_{DS} \ll V_{FB} + \phi_0 - V_{GS}$ , that is,  $V_{GS} \ll V_{FB} + \phi_0 - V_{DS}$ ) the channel conductance does not longer depend on  $V_{DS}$  but on  $V_{GS}$ . So, according to (12) and (4), the conductance can be simply related to the closure of the channel by the depletion region entirely controlled by  $V_{GS}$  as following:

$$g_d = g_{\max} \left[ \frac{t_n - d_n(V_{GS})}{t_n} \right]. \quad (13)$$

At the saturation point, for a given  $V_{GS}$ , the drain current reaches its maximum value, so that the saturation voltage  $V_{DS,sat}$  is obtained by zeroing the channel conductance  $g_d$ , in (12), yielding:

$$V_{DS,sat} = \phi_{PO}(1 + 2\alpha_0) - V_{FB} + V_G = V_G - V_T \equiv V_{GT}. \quad (14)$$

From (7) the threshold voltage  $V_T$  is expected to be high in the device, so the saturation will not occurred for the relatively small values of  $V_{DS}$  considered in the depletion mode.

According the above equations, we can derive some qualitative expectations on the influence of material parameters on the conductance  $g_d$ . According to (11) and (12)  $g_d$  is increased by increasing: the channel doping concentration  $N_d$  or the channel thickness  $t_n$  or also the buried oxide thickness  $t_{ox}$ . Also,  $g_d$  is increased by decreasing the substrate concentration  $N_a$ . Finally, we can notice that for the limit case where the oxide layer vanishes ( $t_{ox} \rightarrow 0$ ) both the silicon oxide coupling factor in (5) and the silicon oxide coupling voltage in (6) vanish while  $V_{FB}$  equals to the junction's built-in voltage  $\phi_i$ . So, the above expressions (12)–(14) are reduced to those describing a classic JFET n-channel device (for which  $N_a \gg N_d$ ).

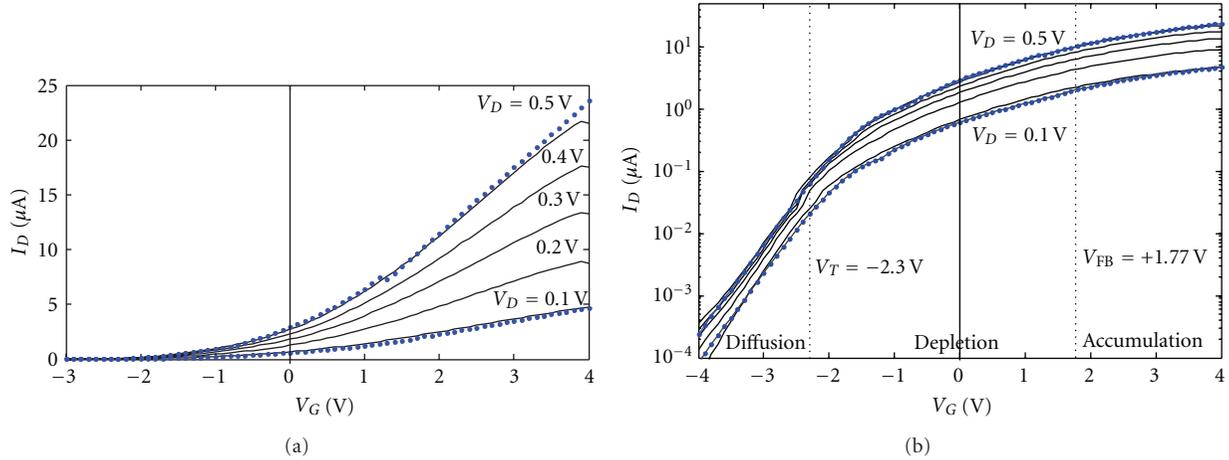


FIGURE 2: Experimental  $I_{DS}$ - $V_{GS}$  characteristics: linear scale in (a) and semi-log in (b). The measurements are taken in dark conditions (solid lines) for several values of  $V_{DS}$  between 0.1 V and 0.5 V. The dotted lines result from the calculated current according to the proposed unified model. For clarity, only results obtained for  $V_{DS} = 0.1$  V and  $V_{DS} = 0.5$  V are presented. The  $V_{GS}$  domains of the operation modes are specified in (b).

## 5. The Unified Linear Model and Parameters Extraction

5.1.  $I_{DS}$ - $V_{GS}$  Characteristics and Operation Modes. A prototype of the constructed SOI-PAM device was experimentally characterized using the Keithley SCS-4200 parameter analyzer. As seen in Figure 2, the  $I_{DS}$ - $V_{GS}$  characteristics are measured over  $[-4$  V,  $4$  V]  $V_{GS}$  range for several low  $V_{DS}$  values (0.1–0.5 V) in order to get a linear relation between  $I_{DS}$  and  $V_{DS}$ .

In this section we develop a unified model of the  $I_{DS}$ - $V_{GS}$  characteristics based on the MESFET unified model [9] available for the three operation modes of the device and at low  $V_{DS}$  values. A similar approach was used by Colinge for a SOI p-channel MOSFET [10].

(1) *Accumulation Mode* ( $V_{GS} > V_{FB} > 0$ ). The n-channel is conducting through the accumulation layer of majority carriers located at the top of the silicon-buried oxide interface. The electron concentration is determined by  $V_{GS}$ - $V_{FB}$ .

(2) *Depletion Mode* ( $V_T < V_{GS} < V_{FB}$ ). The n-channel is partially depleted but is still conducting through the squeezed neutral region of the channel above the depletion region.

(3) *Diffusion Mode* ( $V_{GS} < V_T$ ). The n-channel is fully depleted; there is a small diffusion current flowing from the  $n^+$  source region through the  $n$  depleted channel. The current is controlled exponentially by the gate voltage as observed in MESFET devices [9]. The  $V_{GS}$  sweep is performed quickly enough such the channel inversion is not achieved so the channel is considered in a “deep depletion” state.

We will now express the drain current model for each one of those mode as following:

(1) *Accumulation Mode* ( $V_{GS} > V_{FB} > 0$ ). The linear drain current can be described by the following relation as observed in the pseudo-MOSFET device [11]:

$$I_{DS} = \frac{W}{L} \mu_n C_{ox} (V_{GS} - V_{FB}) V_{DS}, \quad (15)$$

where  $C_{ox}$  is the buried oxide capacitance per unit area, given by:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = 23 \text{ nF/cm}^2. \quad (16)$$

From the linear extrapolation at positive values of  $V_{GS}$ , we can extract the values of  $V_{FB}$  ( $\sim 0.1$  V) and  $\mu_n$  ( $\sim 700$  cm<sup>2</sup>/Vs) which are roughly constant with  $V_{DS}$ . The extracted mobility value is found consistent with the similar thin pseudo SOI-MOSFET [11] having the same silicon film thickness and the doping concentration range of the n-channel ( $10^{17}$  cm<sup>-3</sup>). However due to the non uniformity of the ion implant process, the doping value is not precisely known for each device. Moreover due to the rapid variation of the mobility with doping concentration in this range ( $10^{17}$  cm<sup>-3</sup>), the doping concentration cannot be extracted accurately from the mobility.

(2) *Depletion Mode* ( $V_T < V_{GS} < V_{FB}$ ). The drain current in the partially depleted channel can be rewritten by the following relation [9]:

$$I_{DSa} = q n_{sa} \mu_n \frac{W}{L} V_{DS} \quad (17)$$

with  $n_{sa}$  being the electron sheet density in the channel above the threshold voltage  $V_T$ . This density is simply given by:

$$n_{sa} = N_d (t_n - d_n) \quad (18)$$

while  $d_n$  is the thickness of the depleted region in the channel at low  $V_{DS}$  so it is mainly a square root function of  $V_{GS}$  as given by (4).

(3) *Diffusion Mode* ( $V_{GS} < V_T$ ). For  $V_{DS}$  positive values, the saturation condition ( $V_{DS} > V_{GS} - V_T$ ) is always satisfied in this mode, so the drain current in the fully depleted channel is being described as a saturated diffusion current (independent of  $V_{DS}$ ) according to [9]:

$$I_{DSb} = qn_{sb}D_n \frac{W}{L} = qn_{sb}\mu_n \frac{W}{L} V_{th}, \quad (19)$$

where  $V_{th}$  is the thermal voltage (25.6 mV at room temperature) and  $n_{sb}$  is the electron sheet density in the channel below the threshold voltage  $V_T$ . For  $V_{DS}$  larger than  $V_{th}$ ,  $n_{sb}$  is defined by a Boltzmann's distribution like:

$$n_{sb} = n_0 \exp\left(\frac{V_{GS} - V_T}{\eta V_{th}}\right) < n_0 \quad (20)$$

with  $n_0$  being the electron sheet density at  $V_T$  [9]:

$$n_0 = \left(\frac{C_{si}C_{ox}}{C_{si} + C_{ox}}\right) \frac{\eta V_{th}}{q}. \quad (21)$$

And  $C_{si}$  is the fully depleted silicon channel capacitance per unit area at  $V_T$ , given by:

$$C_{si} = \frac{\epsilon_{si}}{t_n} = 345 \text{ nF/cm}^2 = 15C_{ox}, \quad (22)$$

$\eta$  is the ideality factor extracted from the slope of the subthreshold exponential fit and is evaluated to be 11.5 as the mean value over several  $V_{DS}$  values as seen in Figure 2(b). This value is comparable to the  $C_{si}/C_{ox}$  ratio as also reported in the subthreshold current model for MOSFET devices [9].

According to (19) and (20), the threshold voltage  $V_T$  can be extracted as the departure point of the exponential fit [9] and is found to be  $-2.3$  V as shown in Figure 2(b) for  $V_{DS}$  equals 0.1 V. The corresponding threshold current  $I_{DSb,T}$  is 25 nA which is the maximum diffusion current allowed in the channel.

However, according to (7), the expected value of  $V_T$  is  $-9$  V. Actually, the measured current is not vanishing at  $-9$  V. Moreover, the depletion current  $I_{DSa}$  is a power law function of  $V_{GS}$  while the diffusion current  $I_{DSb}$  is an exponential decay with  $V_{GS}$  below  $-2.3$  V. So the diffusion is the limiting process in the subthreshold mode. Consequently, the measured drain current can be modeled by the following expression [9]:

$$I_{DS,depl} = \frac{I_{DSa}I_{DSb}}{I_{DSa} + I_{DSb}}. \quad (23)$$

Experimentally (see Figure 2(b)),  $I_{DSb}$  is found to be slightly  $V_{DS}$  dependent in spite of the saturation condition assumed above. In fact, we can link this dependence to those of  $V_T$  with  $V_{DS}$  at low  $V_{DS}$  values. This is similar to the DIBL effect found in MOSFET's devices [9]. The  $V_T$  values are extracted from the threshold current  $I_{DSb,T}$  fixed at 25 nA for each  $I_{DS}-V_{GS}$  from Figure 2(b). For instance, for  $V_{DS}$  equals 0.5 V, the extracted  $V_T$  value is  $-2.6$  V. These values are used in the model.

5.2. *Fine Tuning of the Doping Concentration*. Due to the lack of accuracy of the doping concentration, this latter can be refined in order that (23) will best fit the measured drain current in Figure 2(b) in particular at  $V_{DS} = 0.5$  V. The matching value for  $N_d$  is found as  $8 \times 10^{16} \text{ cm}^{-3}$ , instead of the initial designed value of  $10^{17} \text{ cm}^{-3}$ , but still reasonable in regard to the doping distribution. This tuning is performed according the mobility voltage-dependent model as presented below.

5.3. *Mobility Voltage Dependence*. The electron mobility can be evaluated from the extracted threshold voltage  $V_T$  ( $-2.3$  V) using (19) and (20) as follows:

$$\mu_n(V_T) = \left(\frac{qn_0}{I_{DSb,T}} \frac{W}{L} V_{th}\right) = 200 \text{ cm}^2/\text{Vs}. \quad (24)$$

This mobility value is found to be much lower than the value measured in the accumulation mode ( $700 \text{ cm}^2/\text{Vs}$ ). This is not surprising since the low field mobility in the depletion mode is reported to increase rapidly for gate voltages above  $V_T$  in MESFET devices [12]. This should be explained by the decreasing of the depletion layer while increasing  $V_{GS}$  above  $V_T$ . According to this reference, we can expect a linear relation of the mobility with  $V_{GS}$  in order to match the experimental  $I_{DS}-V_{GS}$  characteristics in the depletion mode like

$$\mu_n(V_{GS}) = \mu_0 + \theta(V_{GS} - V_T). \quad (25)$$

Another assumption is necessary for the physical coherence of the proposed model. On the one hand, the mobility cannot vanish with  $V_{GS}$  so it should be pinned to the lower threshold limit value of  $200 \text{ cm}^2/\text{Vs}$  even for  $V_{GS}$  values below  $V_T$ . On the other hand, for the continuity sake, the depletion current above  $V_T$ ,  $I_{DSa}$ , should match the accumulation current voltage [11]. So the current matching between the accumulation and the depletion current (for which  $d_n \sim 0$ ) may occur at a specific "effective" flat band bias  $\underline{V}_{FB}$  defined as follows:

$$I_{DS,acc} = \frac{W}{L} \mu_n C_{ox} (\underline{V}_{FB} - V_{FB}) V_{DS} = I_{DSa} = qN_d t_n \mu_n \frac{W}{L} V_{DS}, \quad (26)$$

the expression of  $\underline{V}_{FB}$  is consequently given by

$$\underline{V}_{FB} = V_{FB} + \frac{qN_d}{C_{ox}} t_n = 1.77 \text{ V}, \quad (27)$$

with:  $N_d = 8 \times 10^{16} \text{ cm}^{-3}$ .

This "effective" flat band bias  $\underline{V}_{FB}$  value actually defines the lower limit of  $V_{GS}$  for which the accumulation current may be described by (15). Also,  $\underline{V}_{FB}$  defines the upper limit of  $V_{GS}$  for which the depletion current may be described by (10).

The mobility variation with  $V_{GS}$  can finally be modeled by using the following step function:

$$\mu_n(V_{GS}) = \begin{cases} \mu_0 \approx 200 \text{ cm}^2/V_S, & V_{GS} \leq V_T, \\ \theta(V_{GS} - V_T), & \theta \approx 175 \text{ cm}^2/V_S, \\ & V_T \leq V_{GS} \leq \underline{V}_{FB}, \\ \mu_n \approx 700 \text{ cm}^2/V_S, & V_{GS} \geq \underline{V}_{FB}. \end{cases} \quad (28)$$

The comparison between the experimental characterization and the unified model as described in this section shows a satisfying matching for  $V_{DS}$  values of 0.1 V and 0.5 V as can be seen from Figures 2(a) and 2(b).

**5.4.  $I_{DS}$ - $V_{DS}$  Characteristics.** In order to confirm and complete the current-voltage model of the SOI-PAM device, the measured  $I_{DS}$ - $V_{DS}$  characteristics are presented in Figure 3. The unified model is used to simulate these characteristics up to the saturation region for  $V_{GS}$  equals  $-1, 0, 1, 2,$  and  $3$  V, respectively, and for positive  $V_{DS}$  values up to 3 V. The linear behavior of the drain current in the saturation region can be interpreted as a drain-induced channel length modulation [9].

For  $V_{GS}$  equals 3 V, the device is in the accumulation mode so the corresponding  $I_{DS}$ - $V_{DS}$  characteristic is well fitted by (15) by adding the parabolic term in  $V_{DS}$  up to the saturation region as used for MOSFET device:

$$I_{DS} = \frac{W}{L} \mu_n C_{ox} \left[ (V_{GS} - V_{FB}) V_{DS} - \frac{V_{DS}^2}{2} \right]. \quad (29)$$

The saturation voltage is then defined as

$$V_{DS,sat} = V_{GS} - V_{FB} \quad (30)$$

with  $V_{FB}$  equals to 0.1 V.

The measured saturation voltage (Figure 3) matches the expected value ( $-2.9$  V).

For  $V_{GS}$  equals 2 V, the device is still in the accumulation mode, so the previous equation is valid till the  $V_{GS}$  equals  $\underline{V}_{FB}$ , that is, 1.77 V as extracted from (26). However, a small discrepancy is observed above 1 V near the saturation region. This may happen due to an enhancement of the channel length modulation effect as mentioned above [9].

For  $V_{GS}$  equals 1 V, the device is now in the depletion mode, so (17) can be used to fit the corresponding characteristic by taking  $\mu_n$  value of  $577 \text{ cm}^2/V_S$  as estimated from (28). The saturation voltage  $V_{DS,sat}$  measured as 2.3 V on Figure 3, is overestimated by the modeled  $V_{GS}-V_T$  value (3.3 V from (14)) may be due to the velocity saturation [9] that was not included in the present model.

For  $V_{GS}$  equals 0 V, the contribution of the diffusion current is negligible and (17) is still sufficient to fit the corresponding characteristic by taking  $\mu_n$  value of  $402 \text{ cm}^2/V_S$  as estimated from (28) but with slight overestimation of the current value and of  $V_{DS,sat}$  as noticed above.

For  $V_{GS}$  equals  $-1$  V, the contribution of the diffusion current is now not negligible and (23) is used to fit the corresponding characteristic by taking  $\mu_n$  value of  $227 \text{ cm}^2/V_S$  as

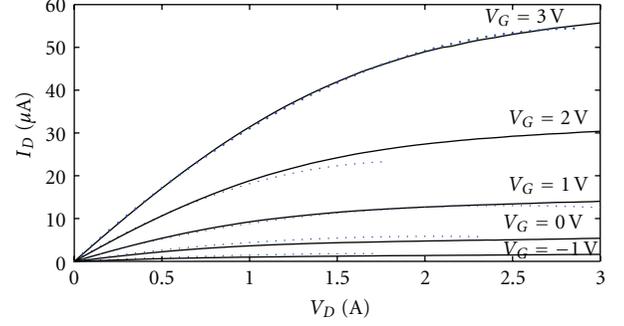


FIGURE 3: Experimental  $I_{DS}$ - $V_{DS}$  characteristics: the measurements are taken in dark conditions (solid lines) for several values of  $V_{GS}$  between 3 V and  $-1$  V. The dotted lines result from the calculated current according to the proposed unified model.

estimated from (28) but again with slight overestimation of the current value and of  $V_{DS,sat}$  as noticed above.

**5.5. Simulation of the Illumination Effect.** By synchronously and directionally illuminating the p-type substrate, the free photogenerated electrons concentration can be significantly and instantly increased to build the inversion (negatively charged) layer under the silicon oxide. Consequently, the positively charged depletion layer in the n-type channel is widening and could fully deplete the channel.

We can express the n-type drop voltage dependency by the amount of electrons that are generated by the applied illumination. The number of incident photons  $N_{ph}$  is related to the total energy  $E_{ph}$  as:

$$E_{ph} = N_{ph} \frac{hc}{\lambda}, \quad (31)$$

where  $h$  is Planck's constant,  $c$  is the speed of light and  $\lambda$  is the photon's wavelength. The capacitances of the partially depleted silicon layer  $C_{Si}$  and the buried oxide  $C_{ox}$  are associated in series, so the total capacitance per unit area is

$$C = \frac{C_{ox} C_{Si}}{C_{ox} + C_{Si}} [\text{F}/\text{cm}^2]. \quad (32)$$

Then, channel's voltage drop, that is, the "illumination induced voltage" can be expressed by

$$V_{ph} = \frac{Q_{ph}}{CWL} = \frac{q\eta\lambda N_{ph}}{CWL}, \quad (33)$$

where  $\eta\lambda$  is the quantum efficiency of silicon for the given  $\lambda$ . So, for relatively low illumination levels, the thickness of the channel depletion layer  $d_n(x)$  can be increased by the illumination-induced voltage  $V_{ph}$  according to (4)

$$d_n(x) = \alpha_0 t_n \left( \sqrt{1 + \frac{V_{FB} - V_{GS} + V(x) + V_{ph}}{\phi_0}} - 1 \right). \quad (34)$$

Consequently, the depleted channel region will grow and the depletion mode current  $I_{DSa}$  will decrease when

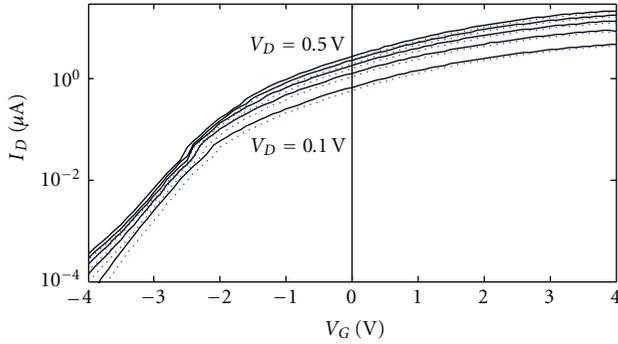


FIGURE 4: Measured  $I_{DS}$ - $V_{GS}$  characteristics (semilog) taken at dark (solid line) and under room light illumination (dashed line). The dashed line is slightly shifted to more positive  $V_{GS}$  values especially in the depletion and the diffusion modes ( $V_{GS} < 1.77$  V).

the illumination energy is increased, as expected from the operation principle of the device. For the actual device parameters, we can evaluate from (34) that the channel will be fully closed (for small  $V_{DS}$ ) by taking  $V_{ph}$  equals 4.5 V, that is, by supplying 75,000 photons (assuming an ideal unity quantum efficiency). In terms of light power, taking for instance, a green diode laser ( $\lambda = 532$  nm), it would be estimated to 2.8 mW per device for a 10 ps pulse. This value can be minimized by decreasing the size of the device and increasing the oxide thickness.

Experimentally, by simply exposing the device to room (fluorescent) light, we can notice a slight positive shift of the whole  $I_{DS}$ - $V_{GS}$  characteristics as shown in Figure 4. This evidence roughly the light-induced decreasing of the drain current as expected from the present model.

Of course, a more in depth measurements of this photoelectric modulation should be performed to validate the model more accurately and will be the object of further publication.

## 6. Conclusions

In this paper, we have derived a unified analytical model of the  $I_{DS}$ - $V_{GS}$  and  $I_{DS}$ - $V_{DS}$  characteristics for whole the operation modes of the SOI-PAM device matching the linear  $I_{DS}$ - $V_{GS}$  domain.

The analysis of the depletion mode is based on the classical Shockley's model but originally adapted to the presence of buried oxide thickness between the n-type channel and the p-type substrate.

The effect of the light on the channel current modulation could be simply expressed as a positive shift of the gate voltage, and a qualitative behavior of the modulation has been demonstrated.

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