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Research Article

Design Optimization of Transistors Used for Neural Recording

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Neurons cultured directly over open-gate field-effect transistors result in a hybrid device, the neuron-FET. Neuron-FET amplifier circuits reported in the literature employ the neuron-FET transducer as a current-mode device in conjunction with a transimpedance amplifier. In this configuration, the transducer does not provide any signal gain, and characterization of the transducer out of the amplification circuit is required. Furthermore, the circuit requires a complex biasing scheme that must be retuned to compensate for drift. Here we present an alternative strategy based on the g_m/I_d design approach to optimize a single-stage common-source amplifier design. The g_m/I_d design approach facilitates in circuit characterization of the neuron-FET and provides insight into approaches to improving the transistor process design for application as a neuron-FET transducer. Simulation data for a test case demonstrates optimization of the transistor design and significant increase in gain over a current mode implementation.

1. Introduction

A transistor represents a unique type of transducer because it can both convert one type of energy to an electrical signal and amplify the resulting signal simultaneously. To amplify the signal, the correct amplification circuit topology must be chosen. A clever designer will optimize both the amplifier circuit and the transistor as part of an iterative design process. To our knowledge, a systematic methodology has not been presented to optimize the transistor structure and the amplification circuitry of neuron-FETs. The approach presented here relies on a circuit design strategy using the level of inversion methodology, also referred to as the g_m/I_d approach [1–3]. This technique has recently gained widespread attention in the integrated circuit design community because it offers techniques for reducing power consumption and maximizing bandwidth in circuits designed to perform analog signal processing.

The process of design may vary considerably as a function of the parameters under the designer's control. Printed circuit board-level engineering is done with discrete components. These system-level engineers select components from a range of available devices and then bias them appropriately. This is done by choosing the appropriate DC (static) operating points. Design with discrete components does not allow the designer control of intrinsic device parameters (i.e., width, length, oxide thickness, mobility, etc.). In contrast, integrated circuit engineers choose a process technology and then select dimensions (width and length) of individual transistors. However, integrated circuit designers rarely have control over the processes used to fabricate the transistors. The effects of process design on transistor performance can be significant. Any circuit will benefit from design optimization techniques applied at the process technology level. In digital circuits, transistors are typically optimized for low off-state leakage, high-drive current, and fast switching. For analog circuits, transistor optimization varies depending on the function of the circuit. For example, the same circuit topology can be optimized at the transistor design level for speed or low noise but not both.

Device engineers optimize the transistor fabrication process by tuning material parameters, oxide thickness, and transistor junctions. Design optimizations at this level may be extremely varied. Typical approaches include gate engineering, oxide engineering, source and drain engineering, and channel and substrate engineering. An excellent survey of the wide array of transistor topologies that have been developed is presented in [4]. Transistors employed as

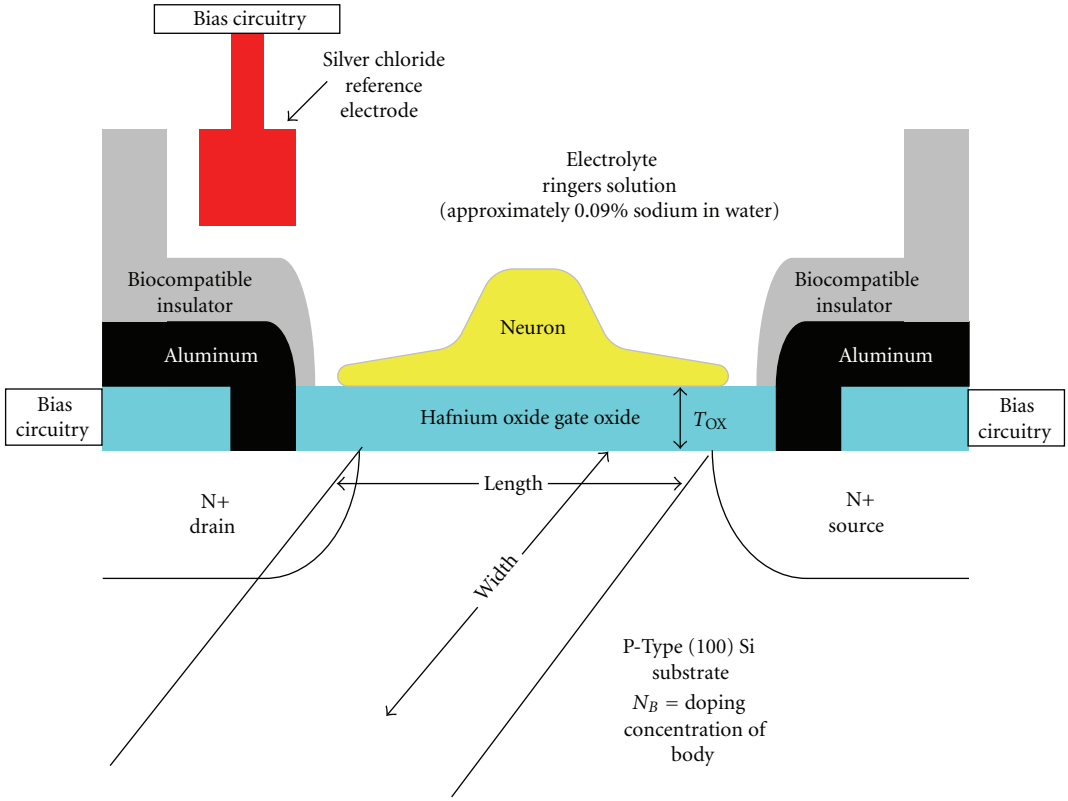

Figure 1: Neuron-FET cross-section. Modified from [27].

transducers represent an even more specialized case of design optimization. Transistor transducer elements are easily created by fabricating a transistor structure and modulating the electric field in the channel region via an energy conversion. For example, when a transistor is fabricated without a gate and submersed in a solution, the ionic charge in the solution serves to create a potential over the channel, modulating the current flow through the device [5, 6]. If neurons are cultured over the channel region where the gate would typically reside, as shown in Figure 1, the electrogenic activity of neurons may be directly detected. Using open-gate field-effect transistors in this manner was first proposed in [7, 8], and later a neuron was directly coupled to the transistor [9]. Excellent reviews that cover the development and application of the neuron-FET are [10–13].

The neuron-silicon hybrid transistor represents an interesting case for transistor and circuit design optimization. In addition to low-noise and high-gain requirements, transistor device sizing is constrained and not necessarily controllable. The boundary of the transistor sizing is set by the size of the neural cells under study and how well they adhere to the channel region. Shorter length and wider channel area result in greater intrinsic gain in transistors. However, for neuron-FETs, the actual width and length are set by the area of the cell membrane that adheres to the channel region. Thus, a large cell may have only a small patch of membrane adhered close enough to the substrate to induce a potential in the transistor channel region. There are several microstructures under study to increase and control the area of the cell that is adhered to substrate, but these will not be reviewed here.

There is a significant range of sizes of cultured neurons ranging from diameters as small as 2 μm for *Drosophila Melanogaster* (fruit fly) neurons to the large cells (300 μm) from *Aplysia Californica* (sea slug). Mammalian cells commonly used for culture include the *Rattus Norvegicus* (rat) Hippocampal neurons (20 μm). Invertebrate neurons grown in culture include retzius cells from *Hirudo Medicinalis* (leech) (60 μm), *Lymnaea Stagnalis* (pond snail) (30–100 um) [14], and *Helix Aspersa* (land snail) (100 μm). Thus, the effective width and length of the neuron-FET has an upper limit defined by the cell size, but is actually defined by the adherent membrane patch area. In each case, the length should be set to a minimum to ensure that a membrane patch is in place over the full length of the transistor or else flow of carriers from source to drain will not be modulated. The lower limit of the transistor length is set by the effect of channel length modulation on the intrinsic gain. The width is set to the approximate area where the neural cell will reside, in the hopes that a significant adherent patch will form across the width of the channel region.

Further design complication arises from the lack of access to the gate terminal. The gate area is covered by a neuron and the electrolyte solution and, thus, not readily available. The most common application of neuron-FETs is in an array topology sensing the response from many neurons simultaneously. The industry standard approach

for sensing large numbers of neurons is the microelectrode array (MEA). Neuron-FETs offer the possibility of realizing significant advantages over MEAs in that the electrodes must be completely covered by the neuron for signal fidelity [15]. Since neurons rarely adhere to the substrate with perfectly circular footprints, shorting to the bath solution in low-density neural cultures is a common problem. Neuron-FETs may be able to record when part of the transducer is exposed to the bath potential, unlike MEAs, but in an array of neuron-FETs the gate DC potential is shorted across all terminals. Thus, separate DC gate biasing of individual transistors is not possible. This also means that decoupling capacitors on the gate or gate resistances cannot be part of the circuit design. The remaining design parameters are a relatively narrow range of lengths and access to the source and drain terminals.

The third major design challenge is the lack of a stable threshold voltage and an inherent DC gate bias. ISFETs are widely known to have threshold voltage drift [16–18]. Drift arises from several sources including hydration of the dielectric, ionic penetration, dielectric erosion under culturing conditions, and wear of the exposed dielectric due to cleaning and sterilization procedures. Drift is assumed to be part of the process of hydration of the dielectric layer over the channel region. Culturing neurons on top of silicon devices may result in mobile ions such as sodium and potassium, part of the required components of a culture media, penetrating into the gate dielectric. Penetration of ions into the dielectric may also cause a threshold voltage drift [19]. There has also been some evidence presented [14] that indicates that silicon dioxide is eroded in physiological saline at physiological temperatures. Gate oxide capacitance may also change through erosion due to cleaning processes if the neuron-FETs are reused. Finally, there is always a bias at the gate terminal because the sum of the metal-electrolyte voltage potential and the electrolyte-insulator dipole potential voltage creates an offset potential along the channel of the neuron-FET [20]. A typical value for a silver chloride electrode is about 250 mV.

Integrated circuit design is typically accomplished through adjusting the width, length, bias voltages and/or bias currents through the transistors. Transistors are assumed to have a stable threshold voltage and a fixed dielectric thickness. This is not the case with open-gate transistors used in biological applications. In amplifier designs using neuron-FETs dimensioning is limited to selection of the length, so optimization of the fabrication process and the circuitry providing biasing currents and amplification becomes paramount.

Neuron-FETs represent a special class of ion sensitive field effect transistors (ISFETs). ISFETs are commonly used as transducers for detection of ion concentrations in bulk solutions. In this application, ISFETs and the associated signal amplification circuitry are designed to operate on slower times scales (seconds) and used to measure ionic concentrations with precision and linearity. In looking to ISFET circuit topologies for design inspiration, there are three significant issues. First, ISFET topologies are optimized for signals that change very slowly (on the order of seconds) and not the 0.5 mS to 2 mS timescale of a neural action potential. Second, ISFETs also do not have constraints on the transistor dimensions, so often they are made large (long width and length) to improve flicker noise performance. Often a feedback system is used to maintain the potential at the reference electrode to improve linearity and enhance measurement of relative change. For this circuit implementation, the ISFET must be maintained in strong inversion to provide a linear output. A good review of topologies and limitations of each ISFET amplifiers topology can be found in [21]. We mention several cases here which are relevant to neuron-FET design. In several examples presented in the literature, the ISFET transducer has been used as a circuit element. In [22], a simple common-source amplifier with a tuned source resistance was introduced. The problem with this system is that the reference electrode supplying the gate bias system is controlled by an operational amplifier that directly controls the drain current potential using a negative-feedback loop. This architecture makes the ISFET less sensitive to changes in the material electrolyte interface and more sensitive to changes in the concentration. The former is the ideal case for neuron-FETs, the latter for ISFETs. A current mode technique is suggested in [23]. This approach uses a complex circuit and a reference FET (reFET) to maintain linearity. The reFET is a transistor designed to be much less sensitive to changes in ion concentration. Since it is impossible to place a reFET and a neuron-FET in near proximity and have the same adherent patch been in place across both transistor channels, approaches that use reFETs in their design are of limited utility.

In the first reports of ISFETs used for transduction of electrogenic cells, cross-coupled amplifiers were suggested as a way of amplifying signals. The issue with this architecture is that it does not allow biasing of the current through the neuron-FET and thus limits the design area. Weak inversion operation of ISFETs was first presented in [24, 25] and developed in subsequent work. The weak inversion regime circuits are designed for wide dynamic range as opposed to sensitivity in a narrow range. However, the weak inversion ISFETs and amplification circuitry were applied to the development of a circuit cell that was used as part of a larger circuit proposed for detecting action potential propagation along and axon, presented in [26]. This topology used pixels that are quite large, intended for recording from nerve bundles. The most common amplifier topology used for neuron-FET recording is the transimpedance amplifier with the transistor biased to produce gains below unity, shown in Figure 2, as presented in [9]. This circuit employs the neuron-FET as a current source with the output fed to a transimpedance amplifier. The problem with this is that the transducer operated in this manner has a less than unity gain. Since the transistor operates in the strong inversion region, it is a low-impedance source. The noise gain of a transimpedance amplifier driven by a low-impedance source is much higher in comparison to that of the noise gain of an equivalent voltage feedback amplifier. In addition, operation in this manner requires a voltage bias for the source and the drain, with the gate (bath) electrode held at ground. To characterize the transistor using a parameter extraction routine to measure changes in gain and threshold

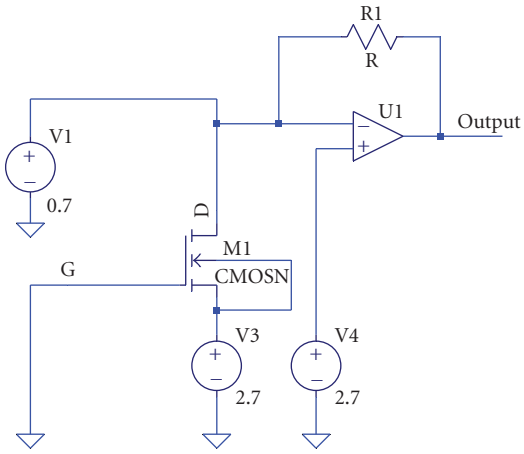

Figure 2: Neuron-FET transimpedance amplifier, as described in [9].

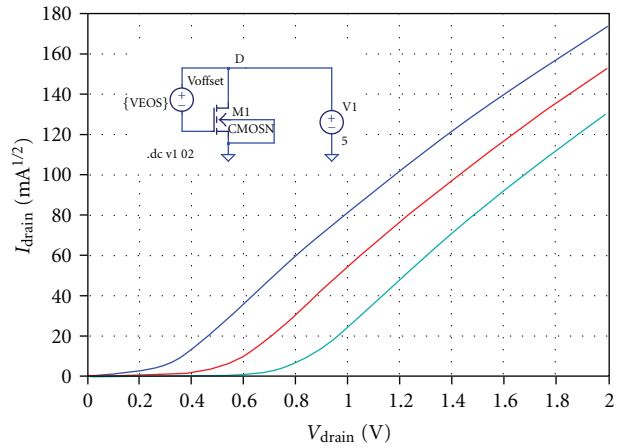

Figure 3: Extraction of V_t and K_n using a diode-connected transistor. Note that the offset potential produced by the reference electrode is incorporated into the estimate for threshold voltage used for design purposes. The offset voltages are −0.250 mV (blue line), 0 V (red line), and +0.250 mV (green line). The V_t of the simulated device is 0.57 V.

voltage, this bias network must be removed. This is an issue because of the changes in the threshold voltage and dielectric properties that occur affecting transducer performance, as discussed earlier.

In the following section, a method to characterize the neuron-FET without direct access to the gate terminal is outlined. This characterization strategy must take into account the potential offsets that occur from the reference electrode and the dielectric layer. During this characterization process, offset bias from the reference electrode is included. The approach used differs from other g_m/I_d design approaches in that transit frequency (f_T) is not considered. Neural signals are far below the upper frequency limits of most transistors and single-stage amplifiers. The characterization process drives the design of a gain stabilized common-source amplifier topology. The common-source degenerated amplifier is an excellent choice because of the gain stabilization it provides, simplicity that allows tuning of the circuit components, and biasing control. This design is compared to the current-transimpedance topology. A first-order evaluation of noise is included.

2. Methodology

Here, we outline a transistor characterization process that facilitates the circuit design process. The methodology provides insight into approaches to improve neuron-FET amplifier performance at both the transistor processing and circuit level. In the first section, a characterization process for the neuron-FET is described. The extracted parameters are required for design, and they provide insight into strategies to improve the operation of the open-gate neuron-FET. Biasing using the g_m/I_d figure of merit is introduced to determine an ideal drain current and gate voltage pair for biasing for peak-gain and low-noise operation. In the second section, feedback is used to stabilize the AC and DC gain of a common-source amplifier. Verification of the design flow demonstrates gain stability in the presence of threshold voltage drift, sufficient bandwidth for amplification, and low harmonic distortion. Several opportunities for system improvement are outlined at the end of this section based upon insight gained from analysis of the design flow.

2.1. Characterization of the Fabricated Device. There can be significant variations in intrinsic transistor performance in neuron-FETs. Prototype transistors are often made using experimental processes and can exhibit wide variabilities when compared to transistors fabricated in a commercial production process. During operation, drift has an unknown effect on the threshold voltage, and the oxide capacitance may also be variable. Therefore a simplified strategy of extracting transistor performance curves is critical. Furthermore, the design strategy should be modified to use data from the simplified extraction routine. Only two parameters and a reference graph are required for the design method presented here. They are; the drain current at moderate inversion and the channel length modulation parameter, λ [$V^{1/2}$], or output resistance, r_o [Ω]. The extracted transconductance efficiency curve then allows determination of a point for gate bias. It is prudent to extract the threshold voltage, V_t [V], and the transconductance parameter, K_n [μA/v^2], to record changes due to drift and dielectric changes. The transconductance parameter and threshold voltage are extracted by shorting the source terminal and applying a voltage source to the drain terminal and the reference electrode and sweeping voltage while measuring current. Data are plotted as V_d [V] versus $I_d{}^{1/2}$ [A]. The test circuit and resulting curve are shown in Figure 3. K_n is calculated as

$$K_n{}' = 2 * \text{slope}^2. \tag{1}$$

And the V_t is estimated as the intersection of the line with the x intercept, using the standard slope intercept form of $y = mx + b$; thus the threshold voltage may be evaluated as

$$V_t = \frac{-b}{m}. \tag{2}$$

This allows determination of the transistor performance parameters V_t and K_n. Electrochemical potentials introduce an error as shift in the threshold voltage. Consequently, the offset becomes part of the system design. Alternatively, the voltage offset may be measured between the bulk and the reference electrode treating the device as a MEIS (metal electrolyte insulator semiconductor) capacitor. Since sensitive calibrated capacitance voltage meters may not be available and would require removing the transistor from the operating circuit, the voltage sweep method has more utility. In reality, the slope will vary significantly with higher drain currents. However, the extraction routine is performed in the operating area of interest. In this region, the values are more stable.

The other critical parameter to enable design is the output resistance, r_o. This is determined by measuring the channel length modulation effect. The test is conducted by measuring the drain current versus the drain voltage as the gate voltage is stepped. However, the output resistance changes as a function of both the gate voltage and the applied drain voltage at each fixed width and length. Thus, the biasing point for the transistor needs to be determined before the output resistance can be measured. Output conductance is a complex function of channel length, gate-to-source voltage, and drain-to-source voltage. The maximum is reached at the onset of moderate inversion and then stabilizes through the weak inversion regime.

Using the g_m/I_d figure of merit, shown in Figure 5, the relationship between transconductance efficiency and drain current can be more easily understood. Transistors biased deeply into the weak inversion region have maximal gain per unit current, but very low drive currents. A minimum acceptable drive current may be determined from the current required to produce a full-swing output across a typical bypass capacitor, according to

$$I = C\frac{\partial V}{\partial t}. \tag{3}$$

Transistors in strong inversion have less gain per unit current, so while the gain increases, the noise, power consumption, and drive current requirements also increase. A good compromise is the transition between the two that is described as moderate inversion. Moderate inversion also describes a region of high-output conductance. Supplementing Figure 4, an alternate method to understand the relationship between intrinsic gain and output resistance is found by plotting the product of g_m/g_{ds} versus I_d (not shown). Both of these methods show that the maximum gain at a fixed width and length is reached at the onset of weak inversion, in the moderate inversion region.

The inversion coefficient can be measured directly by further characterizing the transistor and extracting a process-related value called specific current. Instead of determining an exact value for the inversion coefficient the drain voltage of the diode-connected transistor can be swept and the plot can be inspected for the transition between weak and strong inversion, shown in Figure 5. Measurement is made by diode connecting the transistor and sweeping the drain voltage while the drain current is monitored, the same data as is collected for estimation of the output resistance. The rate of change of the drain current with respect to the drain current ($\partial I_d/I_d$ versus I_d) is plotted versus the drain current on a log-log plot, shown in Figure 6. This approach is derived from

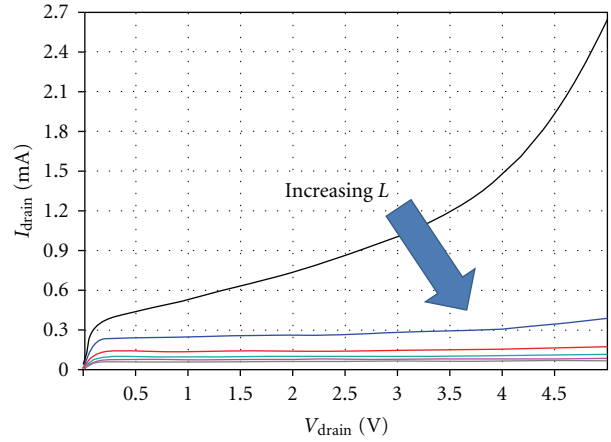

Figure 4: Channel length modulation effects on output resistance as an effect of increasing drain voltage and increasing length. The upper line (black) is a 100 μm transistor with a 0.5 μm length, with each line describing a transistor of increasing length by 0.5 μm.

$$\frac{g_m}{I_d} = \frac{\partial I_d/V_d}{I_d} = \frac{\partial I_d}{I_d}(V_d). \tag{4}$$

Since the procedure for extracting the bias point is so streamlined, it can be routinely performed as part of a measurement process to account for significant changes in threshold voltage and offset potentials.

2.2. Selection of the Amplifier Topology. Typically, in g_m/I_d design voltages are not used to control the level of inversion, but instead drain currents are precisely controlled. In neuron-FET designs, the drain current is difficult to control due to leakage current and inherent variation. The feedback network, part of the amplifier design, can then be used to mitigate variation in the transistor operation and hold the transistor in a moderate inversion regime. Using this technique compensates for the offset produced by the electrochemical potential of the reference electrode, any offset generated at the electrolyte-semiconductor interface and any effects of drift. The drain current bias point determined from Figure 7 allows the correct DC gate voltage biasing for the transistor to maintain operation in the moderate inversion regime and subsequently drives the design of the biasing network for the amplifier circuitry. This figure of merit is generated by shorting the gate and drain and measuring the drain voltage while sweeping the drain current. The drain voltage and g_m/I_d are plotted versus the swept drain current. Notice that the moderate inversion region remains stable across different voltage offset values. The weak inversion region is unavailable if the voltage offset is biased positively.

There are three basic single-transistor amplifiers. They are the common-source, common-drain, and common-gate topologies. Since neurons source very small currents

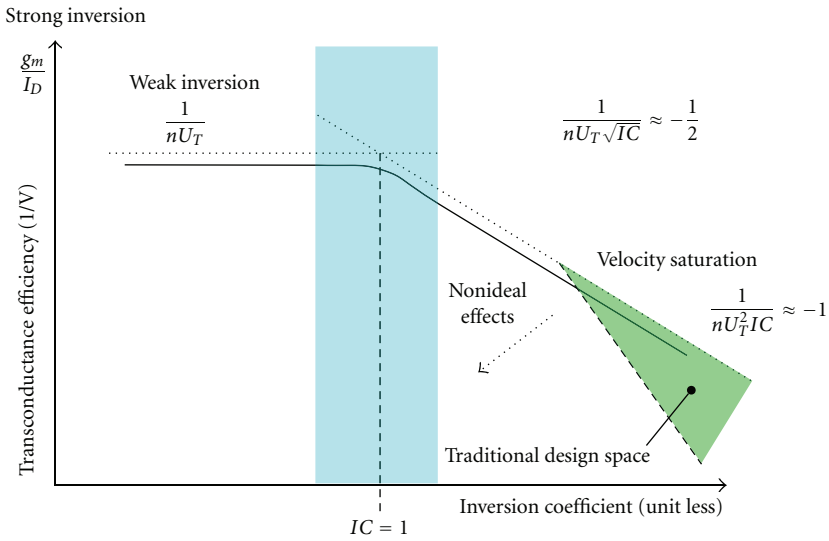

Figure 5: Theoretical transconductance efficiency figure of merit graph. U_T is thermal potential KT and n is the slope factor or body effect factor.

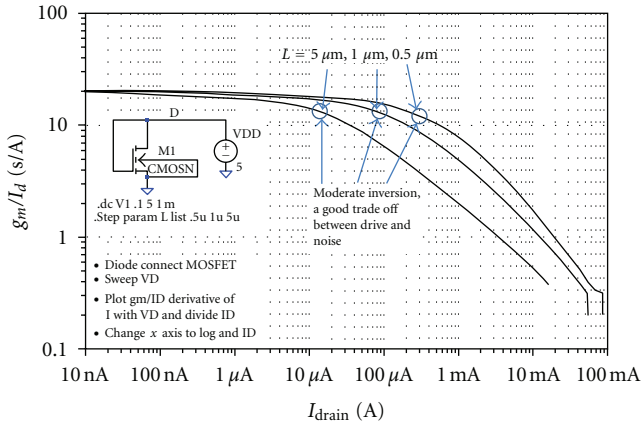

Figure 6: Transconductance figure of merit extracted from simulation of a diode-connected FET. The effect of length on the transition from weak to strong inversion is clearly seen. Longer transistor channel lengths have larger output resistance because they are less affected by channel length modulation, but have lower drive currents in moderate inversion.

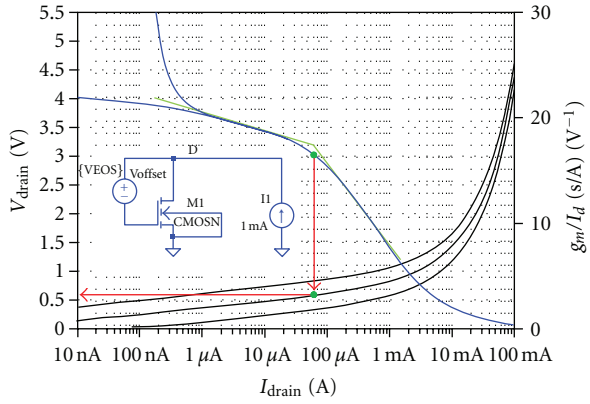

Figure 7: Determination of the DC gate bias as a function of the moderate inversion transition. The blue line is the transconductance efficiency curve (left axis), and the black line is the drain (gate) voltage (right axis). Each of these are stepped a −0.250 V, 0 V and +0.250 V, voltage offset values. The selection of the knee in the transconductance efficiency curve leads to the selection of a 2 μA I_d. The point at which this intersects the gate voltage to provide the DC gate voltage bias point. This pair of values is used to design the single-stage amplifier circuitry.

(nA to pA), they are an inappropriate source for low-input-impedance amplifiers such as the common-gate amplifier. The common-drain amplifier is not appropriate for design because gains are typically less than one and the output resistance is low. Only the common-source amplifier (Figure 8) provides gain from a high-impedance signal source with a high impedance output. Using a source degeneration resistor provides additional benefits because the offset voltage becomes less important, so small variations are mitigated.

The bypass capacitors are selected to pass signals in the bandwidth covering typical neural signals (approximately 500 Hz–10 kHz). Using standard-size components this is a capacitor size of 1 μF and is selected for the source capacitance. Basically, the impedance of the bypass capacitor at the lowest operation frequency (100 Hz) should be much smaller than the resistance of the source resistor (generally 10 times smaller). After a source resistance is selected, the capacitance may be calculated using

$$Z = \frac{R_S}{10} = \frac{1}{2\pi C f}. \quad (5)$$

This in turn drives the current requirements for the device. Feedback is used to reduce the gain and stabilize the circuit over a wider range. The estimate used is to set R_d to a

value equal to the output resistance divided by 10. This makes the drain resistor the dominant effect over the output resistance, r_o, and thus small variations in output resistance are mitigated. R_s is then selected by using a value that distributes equal voltages across R_d, R_s, and the neuron-FET. This results in the following design relationship:

$$V_{\mathrm{DS}} = \frac{1}{3}V_{\mathrm{DD}}, \tag{6}$$

then,

$$V_{\mathrm{DD}} = I_{\mathrm{D}}R_{\mathrm{D}} + \frac{1}{3}V_{\mathrm{DD}} + I_{\mathrm{D}}R_{\mathrm{S}} \tag{7}$$

and, by simplification,

$$\begin{aligned} \frac{2}{3}V_{\mathrm{DD}} &= I_{\mathrm{D}}R_{\mathrm{D}} + I_{\mathrm{D}}R_{\mathrm{S}}, \\ I_{\mathrm{D}}R_{\mathrm{S}} &= \frac{2}{3}V_{\mathrm{DD}} - I_{\mathrm{D}}R_{\mathrm{D}}, \\ R_{\mathrm{S}} &= \frac{2}{3}\frac{V_{\mathrm{DD}}}{I_{\mathrm{D}}} - R_{\mathrm{D}}. \end{aligned} \tag{8}$$

The outcome is that values of R_s are typically slightly larger than R_d. Since the DC intrinsic transistor gain, g_m, approaches $1/R_s$ as R_s becomes large with respect to $1/g_m$ the total DC gain can be estimated as $A_v = -(R_d/R_s)$ and will typically be less than 1. AC gain, in contrast, will approach g_mR_d as the bypass capacitor shorts out the AC signal. If the transistor length is long enough that $r_o \gg Rd$, then bigger r_o means a larger R_d can be used in the circuit and the overall circuit gain can be larger. Also, if $r_o \gg R_d$ then r_o drops out of the gain equation and thus makes the system even less sensitive to r_o variation due to process variation (i.e., variations in length and CLM effects). Overall the resistor source degeneration makes the entire system more stable by providing feedback. The constraint is that the transistor length must be short enough to provide enough drive current to drive bypass capacitors, but long enough to mitigate channel length effects. R_s also has the effect of mitigating the effects of an unstable V_t. As R_s goes to infinity, V_{gs} becomes equal to V_t. This means that K_n becomes dominant and improvements in the process to improve K_n have significant impact on the overall performance.

3. Results and Analysis

Determination of gain and distortion provide valuable metrics in the evaluation of the design stability.

3.1. Gain. Figure 9 clearly shows that a stable gain of approximately 10 is achieved. In addition, the gain varies less than 3 dB across a threshold variation of ±0.5 V.

3.2. Distortion. The distortion is shown in Figure 10 to be even throughout the signal bandwidth of interest. The peak at 1 kHz is due to the input test vector. The first harmonic appears at 3 kHz.

3.3. Noise Effects. Noise analysis reveals interesting characteristic of this amplifier topology. A common source transistor has a voltage thermal noise of

$$\overline{\mathbf{V}_{n,th}^2} = 4kT\left(\frac{2}{3}\frac{1}{g_m}\right) \tag{9}$$

and a current thermal noise of

$$\overline{\mathbf{I}_{n,th}^2} = 4kT\left(\frac{2}{3}\right)g_m \tag{10}$$

that implies that the transistor transconductance must be maximized if the transistor is to amplify a voltage signal at the gate and minimized if the transistor operates as a current source input. The source-degenerated common-source amplifier has a thermal noise of

$$\overline{\mathbf{V}_{n,in}^2} = 4kT\left(\frac{2}{3}\frac{1}{g_m} + R_s + R_D\left(\frac{1+g_mR_S}{g_mR_D}\right)^2\right) \tag{11}$$

excluding the bypass capacitors. This means that at DC, the noise of the source-degenerated common-source amplifier is larger than the simple common-source stage. However, the bypass capacitor at the output blocks DC signals, and at AC the source bypass capacitor shorts R_s. The effect is that no DC noise is passed to the amplifier and the AC thermal noise is equivalent to the common-source amplifier without source degeneration. Neuron-FETs are typically used as current source inputs to a transimpedance amplifier, but this configuration does not provide for amplification or DC blocking. By maximizing the gain and using the neuron-FET as a voltage amplifier, an improvement may be realized.

Noise is an important issue with small signals, and this is especially true in neuron-FETs where the signals are so highly attenuated. The issues are nicely reviewed in [28]. $1/f$ noise dominates the operation of ISFETs, and the same is true of Neuron-FETs. Nyquist noise of adhesion between the neuron and the transistor is another important source of noise [29]. An alternate strategy to mitigate noise effects based on chopper amplification was first presented in [30], but measurement results were inconclusive. Gate-related spectral noise density is given by

$$S_{V_{gs}}(f) \approx \frac{4kT}{c_{ox}^2}\frac{n_{ot}}{WL}\frac{1}{f}, \tag{12}$$

where c_{ox} is the oxide capacitance in F, n_{ot} is the number of oxide traps, W is the transistor width in μm, and L is the transistor length in μm, and f is frequency in Hz. It is already known that increased width and length result in a lower $1/f$ noise; however, these variables are constrained by the use of a transistor as a neuron-FET. Evaluation of the formula shows that significant increases in the oxide capacitance have significant effect on the gate-related spectral noise density when all other variables are held the same. In [28], the authors also suggest that increasing the oxide capacitance will lead to lower $1/f$ noise. In our lab, we have begun to explore high-k films for neuron-FETs [31–34].

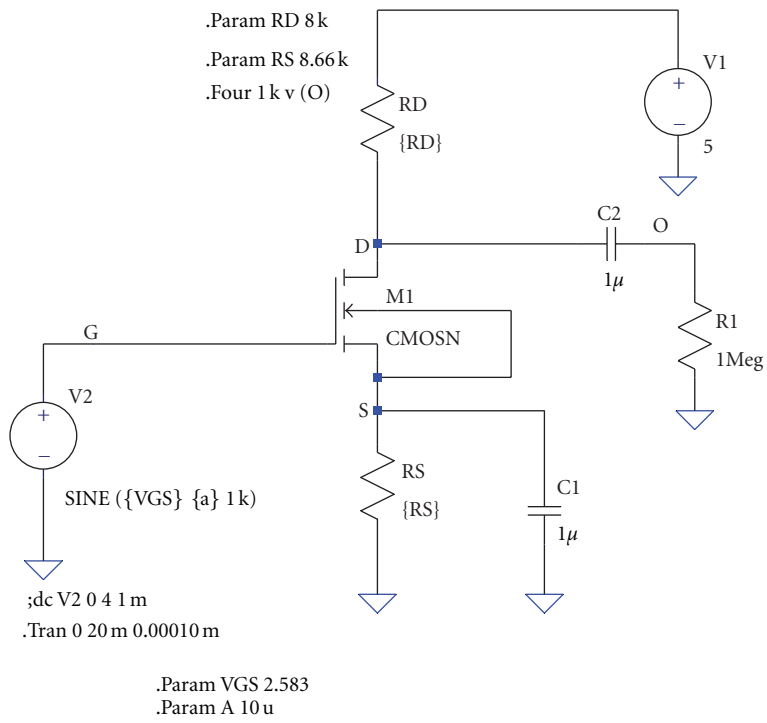

Figure 8: Common source with source degeneration, bypass capacitors, and load resistances.

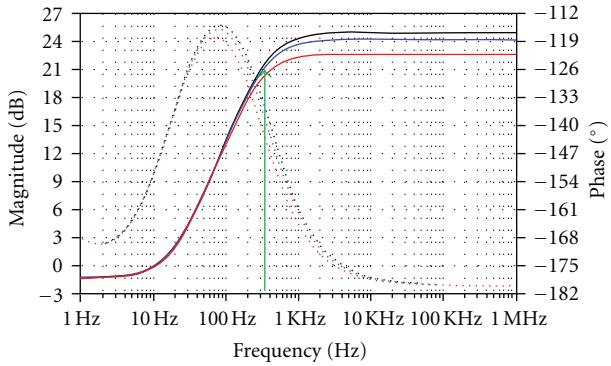

Figure 9: Gain verification. Output is measured from a 10 μV input source as approximately 11, missing the design estimate of 12.5 by about 15%. The green arrow shows the 350 Hz −3 dB frequency. The upper 3 dB (not shown) is much greater than the signal range of interest (approximately 10 kHz). The curves show performance of variable V_t in this configuration. Notice the gain has been stabilized to less than 3 dB across a threshold variation of 1volt.

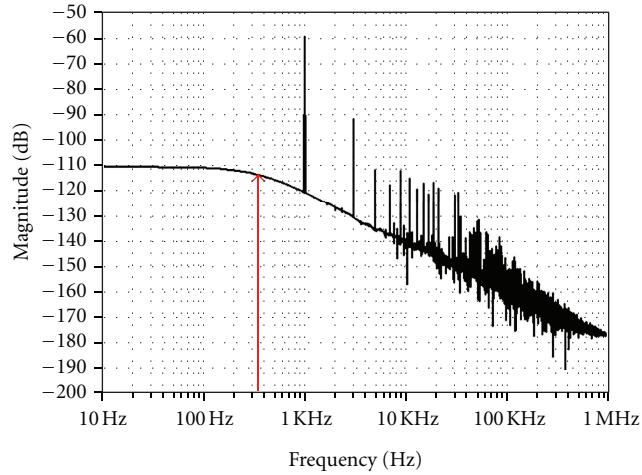

Figure 10: Distortion analysis using the fast Fourier transform. The worst case total harmonic distortion, measured at the lower −3 dB limit of 350 Hz is −114.116 dB or 0.0001969%, shown as a red arrow.

4. High-k Gate Dielectrics

Beyond the circuit topology the transistor fabrication can be optimized. Several labs have reported examples of transistor-level design optimizations. These include the use of high-k dielectrics for the gate. In addition to predicted noise enhancement high-k dielectrics may enhance the transconductance efficiency as well. This in turn may lead to higher gains per unit area, an important design boundary for neuron-FETs. In both cases, the transconductance figure of merit is a valuable design and diagnosis tool for evaluating process technologies. An example of the evaluation of thin and thick oxides and short and long devices using the approach presented in this paper is shown in Figure 11.

4.1. Effects of Ionic Penetration into the Gate Dielectric. To reduce the drift of the threshold voltage of neural sensing transistors, Wallrapp and Fromherz [35] proposed to use high-k dielectrics such as HfO_2 and TiO_2 as the dielectric (oxide) layer to prevent ion penetration of

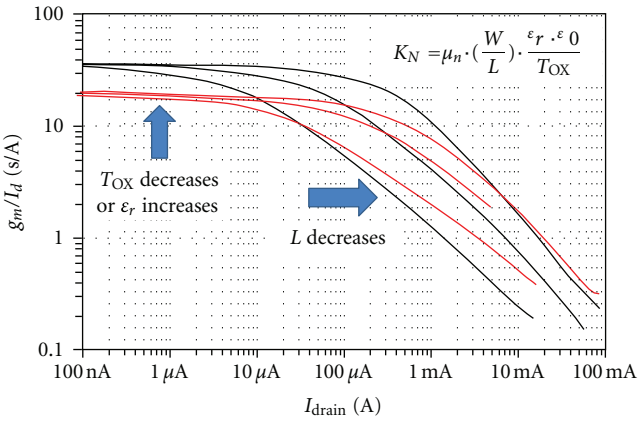

FIGURE 11: Use of the transconductance figure of merit to evaluate process changes. Effect of increasing oxide dielectric constant, increasing length or decreasing oxide thickness. The red line is a thick-oxide transistor; the black lines are from a thin oxide transistor. Both sets of curves are from transistors of a width of 100 μm and lengths $L = 5\,\mu$m, 1 μm, and 0.5 μm from left to right.

the oxide layer. However, there is some evidence that ISFETs with high-k dielectrics still demonstrate drift [36]. Capacitance measurements were presented for HfO_2 and TiO_2 films with thicknesses ranging from 50 to 190 Å that were measured with electrolyte-oxide-semiconductor (EOS) structures. These showed no ionic penetration from the electrolyte. In 2006 Meyburg et al. [37, 38] recorded extracellular signals from embryonic-rat cardiac myocytes using n-channel and p-channel MOSFETs with an extended-gate sensing area similar to that used by Cohen [39, 40]. The sensing oxide was 70 Å thick SiO_2. Sensors did not show the effect of light metallic ion penetration for up to two hours of exposure. In 2007, Meyburg et al. [41, 42] extended his previous work with a full CMOS process that had 2-, 5-bit decoders that were able to address an array of 32 × 32 sensors. In 2004, Cohen et al. [39] was able to measure extracellular voltage signals from *Aplysia* by using a floating-gate depletion mode MOS transistor. The sensing area was comprised of a 420 Å thick SiO_2 that was extended from the polysilicon gate of the transistor. The separation of the sensing area and the active channel reduced the effects of ionic contamination from the tissue culture and allowed the design of the sensing dimensions channel to be separated from the design of the channel dimensions. The depletion mode transistor (normally on) did not require a DC bias to record neural signals. In 2006, Cohen et al. [40] used this recording system to show that the morphology of the neuron controls the shape the field potentials measured from *Aplysia* neurons. This system was used again in 2008 [43] to show that applying mechanical pressure to a neuron can increase the signal-to-noise ratio of the recording. These examples represent important avenues for further investigation.

5. Conclusion

Neurons cultured directly on top of open-gate field-effect transistors result in a hybrid device, the neuron-FET. These represent a special class of an ion-sensitive field-effect transistor (ISFET). Neuron-FETs have significant differences in their operating regime in comparison to ISFETs that result in different design boundaries. These differences call for amplification circuitry specifically designed to amplify signals from neuron-FETs.

Therefore, we have presented a method to optimize circuits that include a transistor used as a transducer to record neural activity. This procedure is not dependent upon the transistor and will benefit from design optimization of the physical transistor device. Using the g_m/I_d technique the circuit designer can optimize the transistor design as part of the design flow. Using this technique we were able to find a transistor length long enough to provide a reasonable output resistance so that it can be made independent of device threshold voltage variations and limitations inherent in the test setup and short enough to drive the bypass capacitors. Simulation data for a test case demonstrates tolerance to variation and a significant increase in gain over typical implementations.

References

[1] P. Jespers, *The GM/ID Methodology, A Sizing Tool for Low-Voltage Analog Cmos Circuits*, Springer, New York, NY, USA, 2009.

[2] D. Foty, D. Binkley, M. Bucher et al., "Starting over: gm/ID-based MOSFET modeling as a basis for modernized analog design methodologies," in *Proceedings of the Technical International Conference on Modeling and Simulation of Microsystems (Nanotech '02)*, pp. 682–685, 2002.

[3] D. M. Binkley, *Tradeoffs and Optimization in Analog CMOS Design*, John Wiley & Sons, Chichester, UK, 2007.

[4] K. K. Ng, *Complete Guide to Semiconductor Devices*, IEEE Press, John Wiley & Sons, New York, NY, USA, 2nd edition, 2002.

[5] M. J. Madou and S. R. Morrison, *Chemical Sensing with Solid State Devices*, Academic Press, Boston, Mass, USA, 1989.

[6] P. Bergveld, "Thirty years of ISFETOLOGY: what happened in the past 30 years and what may happen in the next 30 years," *Sensors and Actuators B*, vol. 88, no. 1, pp. 1–20, 2003.

[7] P. Bergveld, "Development, operation, and application of the ion-sensitive field-effect transistor as a tool for electrophysiology," *IEEE Transactions on Biomedical Engineering*, vol. 19, no. 5, pp. 342–351, 1972.

[8] P. Bergveld, J. Wiersma, and H. Meertens, "Extracellular potential recordings by means of a field effect transistor without gate metal, called OSFET," *IEEE Transactions on Biomedical Engineering*, vol. 23, no. 2, pp. 136–144, 1976.

[9] P. Fromherz, A. Offenhäusser, T. Vetter, and J. Weis, "A neuron-silicon junction: a retzius cell of the leech on an insulated-gate field-effect transistor," *Science*, vol. 252, no. 5010, pp. 1290–1293, 1991.

[10] M. J. Schöning and A. Poghossian, "Recent advances in biologically sensitive field-effect transistors (BioFETs)," *Analyst*, vol. 127, no. 9, pp. 1137–1151, 2002.

[11] C. S. Lee, S. Kyu Kim, and M. Kim, "Ion-sensitive field-effect transistor for biological sensing," *Sensors*, vol. 9, no. 9, pp. 7111–7131, 2009.

[12] A. Poghossian, S. Ingebrandt, A. Offenhäusser, and M. J. Schöning, "Field-effect devices for detecting cellular signals,"

Seminars in Cell and Developmental Biology, vol. 20, no. 1, pp. 41–48, 2009.

[13] P. Fromherz, "Semiconductor chips with ion channels, nerve cells and brain," *Physica E*, vol. 16, no. 1, pp. 24–34, 2003.

[14] M. Merz and P. Fromherz, "Silicon chip interfaced with a geometrically defined net of snail neurons," *Advanced Functional Materials*, vol. 15, no. 5, pp. 739–744, 2005.

[15] D. A. Stenger and T. M. McKenna, *Enabling Technologies for Cultured Neural Networks*, Academic Press, San Diego, Calif, USA, 1994.

[16] J.-C. Chou and C.-N. Hsiao, "Drift behavior of ISFETs with a-Si:H-SiO_2 gate insulator," *Materials Chemistry and Physics*, vol. 63, no. 3, pp. 270–273, 2000.

[17] M. Klein, "Time effects of ion-sensitive field-effect transistors," *Sensors and Actuators*, vol. 17, no. 1-2, pp. 203–208, 1989.

[18] C. Jakobson, M. Feinsod, and Y. Nemirovsky, "Low frequency noise and drift in Ion sensitive field effect transistors," *Sensors and Actuators B*, vol. 68, no. 1, pp. 134–139, 2000.

[19] T. Prodromakis, P. Georgiou, K. Michelakis, and C. Toumazou, "Effect of mobile ionic-charge on CMOS based Ion-sensitive field-effect transistors (ISFETs)," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '09)*, pp. 2165–2168, May 2009.

[20] S. Martinoia and P. Massobrio, "ISFET-neuron junction: circuit models and extracellular signal simulations," *Biosensors and Bioelectronics*, vol. 19, no. 11, pp. 1487–1496, 2004.

[21] A. Morgenshtein, *Design and methodology of ISFET (Ion sensitive field effect transistor) microsystems for bio-telemetry*, M.S. thesis, Senate of The Technion—Israel Institute of Technology, Haifa, Israel, 2003.

[22] A. K. Covington and P. D. Whalley, "Recent advances in microelectronic ion-sensitive devices (ISFETs). The operational transducer," *Journal of the Chemical Society, Faraday Transactions*, vol. 82, no. 4, pp. 1209–1215, 1986.

[23] C. Wang and Y. Zhao, "A novel current-mode readout circuit for ISFET sensor," in *Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems*, pp. 407–410, December 2008.

[24] L. Shepherd and C. Toumazou, "Towards direct biochemical analysis with weak inversion ISFETS," in *Proceedings of the IEEE International Workshop on Biomedical Circuits and Systems*, pp. S1.5–S1.5, December 2004.

[25] L. Shepherd and C. Toumazou, "A biochemical translinear principle with weak inversion ISFETs," *IEEE Transactions on Circuits and Systems I*, vol. 52, no. 12, pp. 2614–2619, 2005.

[26] P. Georgiou, I. F. Triantis, T. G. Constandinou, and C. Toumazou, "Spiking chemical sensor (SCS): a new platform for neuro-chemical sensing," in *Proceedings of the 3rd International IEEE EMBS Conference on Neural Engineering (CNE '07)*, pp. 126–129, May 2007.

[27] D. W. Parent and E. J. Basham, "Hafnium transistor process design for neural interfacing," in *Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society: Engineering the Future of Biomedicine (EMBC '09)*, pp. 5875–5878, September 2009.

[28] C. Jakobson and Y. Nemirovsky, "I/f noise in ion sensitive field effect transistors from subthreshold to saturation," *IEEE Transactions on Electron Devices*, vol. 46, no. 1, pp. 259–261, 1999.

[29] M. Voelker and P. Fromherz, "Nyquist noise of cell adhesion detected in a neuron-silicon transistor," *Physical Review Letters*, vol. 96, no. 22, Article ID 228102, 2006.

[30] M. Dagtekin, *A chopper modulated amplifier system design for in vitro neural recording*, Ph.D.dissertation, North Carolina State University, Raleigh, North Carolina, 2006.

[31] D. Parent and E. Basham, "Hafnium transistor design for neural interfacing," in *Proceedings of the 30th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBS '08)*, pp. 3356–3359, August 2008.

[32] D. Parent and E. Basham, "A course for designing transistors for high gain analog applications," in *Proceedings of the 17th Biennial University/Government/Industry Micro-Nano Symposium—UGIM*, pp. 75–78, July 2008.

[33] D. W. Parent and E. J. Basham, "Hafnium transistor process design for neural interfacing," in *Proceedings of the Annual Engineering in Medicine and Biology Society (EMBC '09)*, pp. 5875–5878, Minneapolis, Minn, USA, September 2009.

[34] D. W. Parent, J. Davis, and E. J. Basham, "High-k dielectric fabrication process to minimize mobile ionic penetration," in *Proceedings of the Annual Engineering in Medicine and Biology Society Conference (EMBC '10)*, Buenos Aires, Argentina, 2010.

[35] F. Wallrapp and P. Fromherz, "TiO_2 and HfO_2 in electrolyte-oxide-silicon configuration for applications in bioelectronics," *Journal of Applied Physics*, vol. 99, no. 11, Article ID 114103, 2006.

[36] H. Hara and T. Ohta, "Dynamic response of a Ta_2O_5-gate pH-sensitive field-effect transistor," *Sensors and Actuators B*, vol. 32, no. 2, pp. 115–119, 1996.

[37] S. Meyburg, M. Goryll, J. Moers et al., "N-Channel field-effect transistors with floating gates for extracellular recordings," *Biosensors and Bioelectronics*, vol. 21, no. 7, pp. 1037–1044, 2006.

[38] S. Meyburg, G. Wrobel, R. Stockmann, J. Moers, S. Ingebrandt, and A. Offenhäusser, "Single cell recordings with pairs of complementary transistors," *Applied Physics Letters*, vol. 89, no. 1, Article ID 013901, 2006.

[39] A. Cohen, M. Spira, S. Yitshaik, G. Borghs, O. Shwartzglass, and J. Shappir, "Depletion type floating gate p-channel MOS transistor for recording action potentials generated by cultured neurons," *Biosensors and Bioelectronics*, vol. 19, no. 12, pp. 1703–1709, 2004.

[40] A. Cohen, J. Shappir, S. Yitzchaik, and M. E. Spira, "Experimental and theoretical analysis of neuron-transistor hybrid electrical coupling: the relationships between the electro-anatomy of cultured Aplysia neurons and the recorded field potentials," *Biosensors and Bioelectronics*, vol. 22, no. 5, pp. 656–663, 2006.

[41] S. Meyburg, R. Stockmann, J. Moers, A. Offenhäusser, and S. Ingebrandt, "Advanced CMOS process for floating gate field-effect transistors in bioelectronic applications," *Sensors and Actuators B*, vol. 128, no. 1, pp. 208–217, 2007.

[42] M. Schindler, S. Ingebrandt, S. Meyburg, and A. Offenhäusser, "Design and function principle of a large scale sensor array for the bi-directional coupling to electrogenic cells," in *Proceedings of the 4th International Conference on Solid-State Sensors, Actuators and Microsystems*, pp. 1243–1246, June 2007.

[43] A. Cohen, J. Shappir, S. Yitzchaik, and M. E. Spira, "Reversible transition of extracellular field potential recordings to intracellular recordings of action potentials generated by neurons grown on transistors," *Biosensors and Bioelectronics*, vol. 23, no. 6, pp. 811–819, 2008.