

## Research Article

# Multilayer, Stacked Spiral Copper Inductors on Silicon with Micro-Henry Inductance Using Single-Level Lithography

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We present copper structures composed of multilayer, stacked inductors (MLSIs) with tens of micro-Henry inductance for use in low frequency (sub 100 MHz), power converter technology. Unique to this work is the introduction of single-level lithography over the traditional two-level approach to create each inductor layer. The result is a simplified fabrication process which results in a reduction in the number of lithography steps per inductor (metal) layer and a reduction in the necessary alignment precision. Additionally, we show that this fabrication process yields strong adhesion amongst the layers, since even after a postprocess abrasion technique at the inner diameter of the inductors, no shearing occurs and connectivity is preserved. In total, three separate structures were fabricated using the single-level lithography approach, each with a three-layered, stacked inductor design but with varied geometries. Measured values for each of the structures were extracted, and the following results were obtained: inductance values of 24.74, 17.25, and 24.74  $\mu\text{H}$ , self-resonances of 9.87, 5.72, and 10.58 MHz, and peak quality factors of 2.26, 2.05, and 4.6, respectively. These values are in good agreement with the lumped parameter model presented.

## 1. Introduction

Over the last decade, researchers have done a considerable amount of work to model, characterize, and design air-core spiral inductors on silicon technology for both radio-frequency integrated circuits (RFIC) and monolithic microwave integrated circuits (MMICs). In most of these works, both performance and cost are typical issues examined. For many designers, performance relates directly to improving the quality  $Q$  factor of these spiral inductors. Most notably, this has been achieved using designs such as multilayered, stacked inductors (MLSIs), see Figure 1, which increase the inductance value due to the mutual magnetic coupling [1], and multiple shunt inductors, which lower the resistance [2, 3]. For those researchers concerned with cost, much of the focus is within analyzing the process with respect to the standard complementary metal oxide semiconductor (CMOS) technology, where the key factors in determining the cost are (1) feature size, (2) number and kinds of layers, and (3) chip area occupied [4]. Within this work, we focus on simplifying

the fabrication of integrated inductors for the emerging area of power converter technology. Specifying for this growing field, researchers must again balance performance and cost issues with new requirements like the need for much higher inductance in the order of micro-Henries and operation ranges below 100 MHz.

To highlight some examples of the balance of performance and cost issues, we cite here results of recent research within short-range radio frequency identifier (RFID) antennas, and DC/DC converters. For wireless technology, a typical approach of biomedical devices [5] and strain sensors [6] has been for researchers to use large, single in-plane inductors as short-range RFIDs. Thus they have chosen to balance the simplicity of single-layer inductor design with the cost of using large chip areas, which for [5, 6] yield 2.7 cm diameters in order to meet the 4-5  $\mu\text{H}$  inductance requirements. For DC-DC converter technology, researchers have chosen to modify the single-layer CMOS fabrication by orienting the final structure orthogonal to the substrate using magnets and a hinge design, known as plastic deformation magnetic



FIGURE 1: Three-dimensional rendering of a multilayered, stacked inductor (MLSI).

assembly (PDMA) [4]. The results are structures with  $1 \mu\text{H}$  inductance and a small chip area ( $0.1 \text{ mm} \times 0.1 \text{ mm}$ ), but with the increased types of layers adding cost and difficulty.

In this work, we introduce a simplified CMOS fabrication approach using single-level lithography in order to reduce the difficulty of the number of lithographic steps per layer over the traditional two-level lithographic approach. This simplified layer approach allows us to then extend the number of layers from a single-layer design to a MLSI design at a lower cost over the traditional approach. To substantiate the selection of the multilayer over single-layer design option, we compared, based on cost factors, several works aimed at achieving high-inductance monolithic inductors. From that review, we found that higher inductance, single-layer inductors were achieved using exotic substrates [7, 8], while MLSI on standard, silicon substrates [1, 9] were able to achieve similar, if not higher, inductance values, by exploiting the mutual magnetic coupling effects. When examining the results with respect to the factors for cost, the latter is seemingly better, especially with respect to increased inductance per unit area, and without the need for deviation from standard CMOS processes. By combining our simplified single-level lithography design, which features potential for decreased cost per inductor layer, with a multilayer process, which increases cost, the resulting reduction in chip area should provide a net cost advantage. Thus, we detail our simplified fabrication technique with respect to the standard two-level lithography approach to highlight the differences. In addition, we analyze the performance metrics of three structures fabricated using our single-level lithography approach, recording the inductance value,  $L$ , the inductance per unit area, the quality factor,  $Q$ , and the self-resonance frequency, SRF, so as to allow researchers to compare both performance and cost with future works. Lastly, we include a lumped parameter analytical model of the multilayer, stacked inductor so as to validate the measured results.

## 2. Multilayered, Stacked Spiral Inductor Theory

When designing single-layer, spiral inductors, typically a lumped parameter approximation using the  $\pi$ -type electrical model [10–13] is applied for simplicity, which is valid up to the self-resonance frequency, see Figure 2. This model can be viewed as an RLC circuit, where the inductance,  $L_s$ , and capacitance,  $C_s$ , of the coil are in parallel, with losses to the substrate induced by the capacitive and conductive

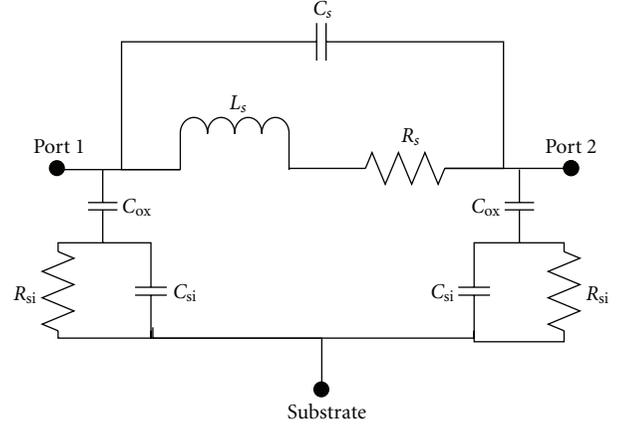


FIGURE 2:  $\pi$ -type electrical model of a single-layer, spiral inductor.

properties of the substrate. These and other parasitic losses vary with respect to the geometry and orientation of the inductor. Techniques for predetermining all of these parameters' values have ranged from empirical expressions [12] to Greenhouse's method [11] to electromagnetic field solvers [14].

Using this model, various geometries and materials have been studied within the literature to reduce the losses and produce higher performance metrics. Specifically, some researchers have experimented with various substrate materials, Quartz, GaAs, and Sapphire [7, 8, 15], to reduce the losses brought on by the  $R_{si}$  and  $C_{si}$  components. Researchers have also experimented with creating large trenches on the underside of the devices to increase the separation distance to the substrate and reduce the capacitive loss [16]. While these techniques are valid, they add considerable complexity and cost to the fabrication process, since they introduce costly materials and require long etching process times.

While the reduction of losses has shown improvement in inductor performance, large inductance variation can occur by manipulation of the inductor geometry itself [10]. We estimate the inductance of an in-plane spiral using the zeroth order approximation given by a current sheet expression [12].

$$L = \frac{\mu N_t^2 d_{ave} c_1}{2} \left[ \ln \left( \frac{c_2}{\rho} \right) + c_3 \rho + c_4 \rho^2 \right]. \quad (1)$$

Equation (1) assumes a nonferrous core, which results in the inductance being determined exclusively by the spiral geometry. We define  $\mu$  as the permeability,  $N_t$  as the number of turns,  $d_{ave}$  as the average diameter of the turns, and  $\rho$  as the fill ratio of the single-layer spiral. The coefficients  $c_i$  are dependent on the layout of the spiral, such as square, hexagonal, octagonal, or circular. To increase the inductance value of single-layer spirals, increasing the number of turns, or  $N_t$ , is a simple and effective option.

To increase the inductance values without further increasing the footprint area, we expand the single-layer spiral to a multilayered, stacked spiral. MLSI spirals have been shown in the literature to increase single-layer spiral

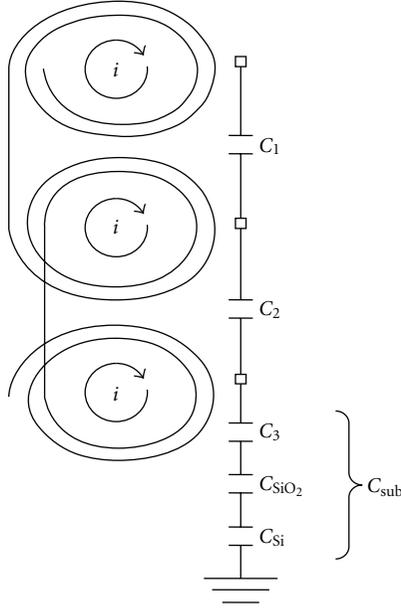


FIGURE 3: Schematic of triple-layer, stacked inductor.

inductance values by the summation of the individual single-layer spiral inductances and their mutual inductances between layers [3, 4]. The equivalent inductance,  $L_{eq}$ , for a MLSI is shown in [12]

$$L_{eq} = \sum_{i=1}^n L_i + \sum_{i=1}^n \sum_{j=1, j \neq i}^n M_{ij}. \quad (2)$$

The value  $n$  is the number of stacked layers, the term  $L_i$  refers to the  $i$ th single-layer spiral inductance value, and the term  $M_{ij}$  accounts for the mutual inductance between each set of single-layer spirals. If we assume that the inductance of each single-layer spiral is approximately the same, then (2) reduces to the inductance of a single-layer spiral times the square of the number of stacked spiral layers. Thus, by interconnecting the spirals, we can increase the inductance of each MLSI design by a square of the number of single-layer spiral turns and multiply that value by a square of the number of stacked spiral layers.

However, predicting only the inductance does not give an accurate estimate for the resultant reactance, or nominal inductance, of the integrated inductor measured using impedance analysis. For the reactance, a relationship between the capacitance and the resistance of the device is needed as well. A general form for calculating the capacitance of two adjoining surfaces is shown in

$$C = \frac{\epsilon A_{surf}}{\delta}. \quad (3)$$

The term  $\epsilon$  is the permittivity of the medium, and the term  $\delta$  is the separation distance between the two facing surface areas,  $A_{surf}$ . By increasing the number of turns for a single-layer spiral, the area and capacitance also increase. To lower the capacitance while increasing the inductance,

multilayered, stacked, spirals have the following equivalent capacitance, see Figure 3 [1]

$$C_{eq} = \frac{1}{3n^2} \left( 4 \sum_{i=1}^{n-1} C_i + C_{sub} \right) \quad (4)$$

Equation (4) is derived from the assumption that there exists perfect coupling between each two inductive elements, and thus the voltages in each turn are equal. The term  $C_i$  is then simply expressed as the capacitance between each of the single-layer spiral layers, which is determined by the dielectric layers in between. It is determined from (4) that MLSI design lowers the effect that the substrate has on the total capacitance when compared to single-layer inductors. In addition, the introduction of large separation distances between each single-layer spiral layer, using interconnect technology [17, 18], can further reduce the equivalent capacitance and increase the SRF.

To complete the lumped parameters, the series resistance is found using

$$R = \frac{\rho l}{S_{eff}}, \quad (5)$$

where  $\rho$  is the conductance of the inductor's metal trace,  $l$  is the total length of the spiral inductors, and  $S_{eff}$  is the effective cross-sectional area of the inductor's metal trace. At zero frequency, or DC, the effective cross-sectional area is the physical cross-sectional area of the inductor's trace. For low frequency designs, it can be assumed that the DC resistance is a good estimate of the actual resistance, as long as the proximity effects and skin depth effects, while present, are orders of magnitude less than the DC resistance [19].

Combining (2), (4), and (5), the MLSI shown in Figure 1 has a reactance,  $X$  of [20]

$$X = 2\pi f L_{eq} \left( 1 - \frac{R^2 C_{eq}}{L_{eq}} - 4\pi^2 f^2 L_{eq} C_{eq} \right). \quad (6)$$

The term  $f$  refers to the operational frequency of the inductor. Equation (6) approximates the MLSI as a LC circuit in parallel with a finite resistance. Thus, the self-resonance frequency, SRF, is when the reactance value is equal to zero. To increase the nominal inductance, or reactance, and the useful operation range, or SRF, it is clear that maximizing the inductance and minimizing the capacitance are the key aspects of the design. MLSI are thereby an excellent choice for high inductance devices, as both inductance and capacitance can be tailored with geometric parameters.

A final inductor performance metric to estimate is the value of the quality factor, or  $Q$ . The  $Q$  is a measure of the ratio of the energy stored over the energy lost in one cycle. A simple expression for the  $Q$  can be estimated up to the SRF using the relationship for the resistance, (5), and the reactance, (6)

$$Q = \frac{X}{R}. \quad (7)$$

Therefore, to increase the  $Q$  value for these low frequency devices, the length of the trace, which is increasing with every

single-layer turn or number of stacked layers, must be offset by a larger trace width and/or thickness. Both single- and multilayered, stacked inductors have the advantage that both the trace width and the thickness can easily be modified to larger values by creating a larger patterning mold [18].

By using the performance metric relationships listed, we have generated theoretical predictions for the measured reactance (nominal inductance), the resistance, the first self-resonance frequency, and the quality factor of MLSI. We have also shown the key geometrical considerations associated with creating high inductance and high  $Q$ . With the lumped parameter model established, we now focus on a how single-level lithography can lower the fabrication cost for these MLSI designs.

### 3. Device Fabrication

A major cost concern with CMOS fabrication is keeping the number of steps or processes involved, as well as the precision needed within each step, to a minimum. In accordance with these principles, to fabricate a multilayer, stacked copper inductor, we use a single-level lithography process as opposed to the traditional two-level lithographic process. To achieve this simplified process, we use two types of photo-resists, SU-8 and SPR-220. SU-8 is a permanent photo-resist that serves as a structural layer to build the coil layers onto, as well as the dielectric material between the layers. SPR-220 is then used after evaporating the copper inductor layer to pattern the inductor using wet-etching. Thus, unlike two-level lithography, single-level lithography eliminates the step of electroplating the patterned inductor layer. After the single-level lithography is finished, holes for interconnects between the stacked inductor layers are made on the SU-8 layer and filled with copper using electroplating. These copper connects create a conductive pathway from the seed layer to the first planar inductor and each subsequent planar inductor layer. By repeating these two processes, inductor layers can be stacked onto previous layers and the trace is able to maintain its connectivity through the connection holes. Thus, the entire process eliminates a lithographic step for each inductor layer, reducing the fabrication cost over two-level lithography. Lastly, we include an extremely fast process, abrasion drilling, as a way of creating an air core once the MLSIs are completed.

Figure 4 shows a simplified version of our process. First, a silicon wafer is thermally oxidized to create an insulator between the silicon substrate and the inductor structure, reducing the parasitic substrate loss, Figure 4(a). Next, a tantalum layer is evaporated onto the wafer to improve the adhesion of subsequent evaporated layer, the coil's copper seed layer. The seed layer provides a pathway for electroplating the deep interconnects, Figure 4(b). On top of the seed layer, SU-8 2010 photo-resist solution is spun at a specified thickness, which determines the thickness of the dielectric layer (relative permittivity of 2.46), or the separation distance to the first spiral inductor layer and the resultant capacitance,  $C_n$ . We pattern the SU-8 with a standard lithography process using the connecting layer mask in order to define the interconnect position. By creating only a single, large interconnect, the precision for alignment of the spiral layer is

lowered, reducing the difficulty of the lithography process. A final annealing step, of 115°C for 2 minutes, is applied after developing, to improve the adhesion of the SU-8 and copper inductor layers. When the wafer is dried, it is descummed with oxygen plasma etching, which increases the surface roughness, and assists the adhesion of the next copper layer, Figure 4(c).

To build each inductor layer, copper is evaporated over the entire area of the wafer at a rate less than 20 Angstroms per second, Figure 4(d). Next, P20 is spun to assist with the adhesion of the patterning layer, which is SPR220-7. Using a negative coil mask and a standard lithography process, the SPR220 is used to form an outline covering the in-plane spiral pattern, Figure 4(e). To remove the excess copper, the wafer is immersed in a copper etchant and careful attention is made to not agitate the solution, otherwise coil liftoff can occur. When the complete copper removal is visually observed, the wafer is taken out and thoroughly washed with distilled water. The area covered with SPR220 is left as the in-plane patterned inductor spiral, and the SPR220 is removed with a gentle spraying of acetone and then isopropanol, Figure 4(f). By doing the patterning of each in-plane spiral this way, we reduce the number of steps needed to only a single-level patterning and concurrently require only a low precision of the pattern be necessary for achieving alignment with the interconnect points between the layers, since the feature sizes are large for micro-Henry inductance. This process is significantly less difficult to achieve than most electroplating techniques used to produce coils, which require a two-level patterning lithography [18]. To explain further, in the two-level patterning, after the evaporation and patterning of the inductor, another level of photo-resist is needed in order to create channels for allowing electroplating of the inductor layer to increase the in-plane thicknesses. While larger thicknesses do reduce the series resistance, the process adds another step for every inductor layer as well as it introduces the possibility of needing to do chemical metal polishing (CMP) in order to form parallel layers for future mask alignments. So by using our single-level lithography we trade off constraining the thickness, and the resistance, of the inductor to the limits prescribed by the evaporation process in order to reduce the fabrication cost. In applications like power converter technology, this performance tradeoff is not as critical, since the high inductance values offset the high resistance, yielding reasonable  $Q$  values. To complete the process and make all the layers mutually conductive, we use the standard procedure of electroplating the interconnect layers.

In this step, we electroplate copper in a copper sulfate solution, Microfab SC from Enthone, Inc., at a current density of 0.02 mA/mm<sup>2</sup> to connect the copper in-plane spiral layer to the copper seed layer using the interconnect holes (Figure 4(g)). The rate and duration at which the electroplating process occur are dependent on the concentration of the electroplating solution and the amount of copper that needs to be deposited within the interconnect, that is, the amount needed to both fill the hole and make an electrical connection between the inductor layers. For our procedure, this electroplating process is simplified, because it requires only an electrical connection between the electroplating circuit's

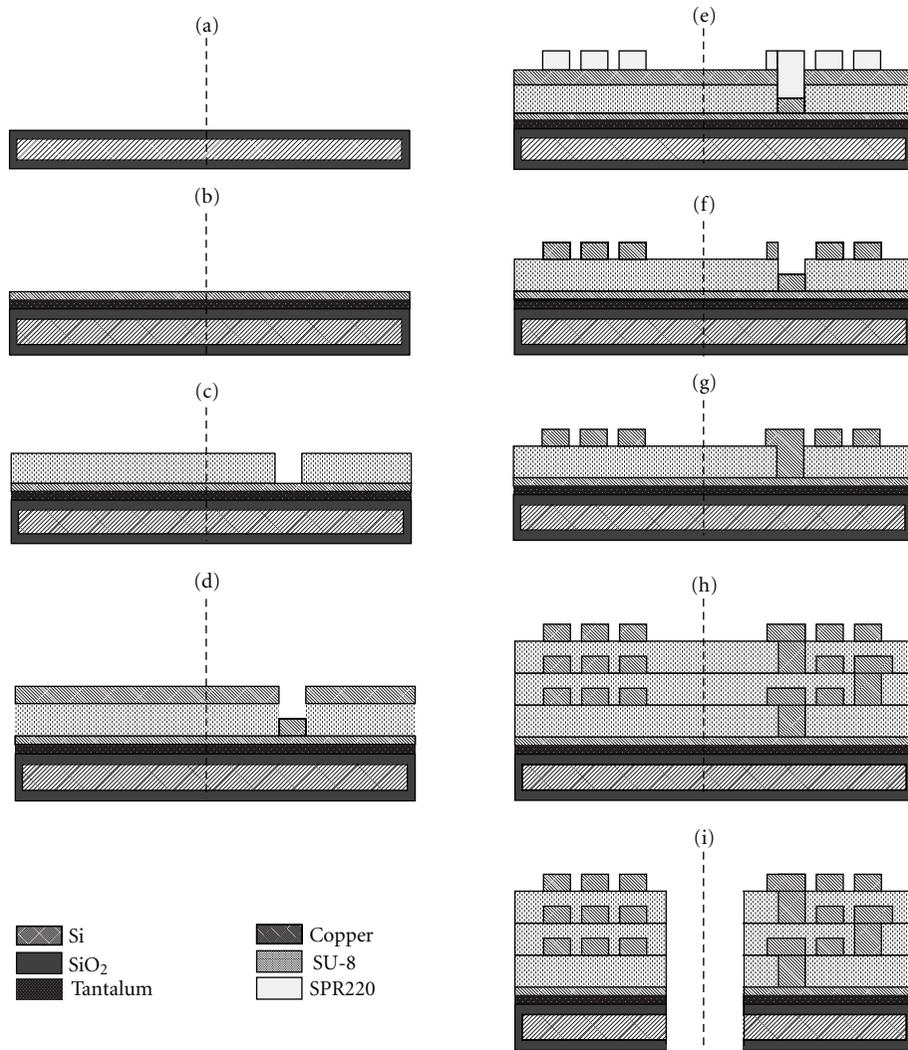


FIGURE 4: Simplified fabrication process. Note not drawn to scale in order to show layers.

clips and the seed layer, which is exposed at the edge of the wafer. With an electrical connection to the seed layer, current flow and copper deposition within the interconnect are easily achieved. Once the first interconnect is filled, continuity to the inductor layer is achieved. We are therefore able to verify completion of this process by solely checking that continuity exists.

The two processes are then repeated from the SU-8 spinning, Figure 4(c), to the copper interconnect between the copper inductor layers (Figure 4(g)), forming a MLSI design, Figure 4(h). For the electroplating process, once an interconnect makes continuity with the next inductor layer, the current will continually flow to the next interconnect. This continues until the electroplating process deposits copper within the last interconnect and makes a connection to the uppermost inductor layer. Since MLSIs need to have current flow in the same direction for all the inductor layers, in order to superimpose inductance effects, a total of four masks, two for alternating connecting layer masks and two for alternating coil layer masks, are needed. To summarize, our entire

procedure requires a single-level, low-precision lithography, and one simple continuity test to be passed after the electroplating process for each inductor layer of a MLSI design. We can conclude that the entire fabrication procedure meets many of the attributes considered for low difficulty and low cost.

Lastly, a final postprocessing step is performed that uses a simple, fast method for creating air cores within these MLSIs. The technique is an abrasion, or manual drilling process, in which we use a blunt, diamond-coated drill bit, sized to a diameter smaller than the inductor's inner diameter, to create a through hole at the center, Figure 4(i). By applying light hand pressure using a microdrill and manually turning the drill bit, a hole is created in the inner diameter of the multilayer coil within seconds (see Figure 5), which is far faster than etching techniques previously used in the literature for creating cavities [1]. In addition to the improvement on time, this step shows that with our fabrication technique, the single-level lithography provides adequate adhesion and support to maintain the inductor's structural integrity and



FIGURE 5: Air core created by abrasion drilling process.

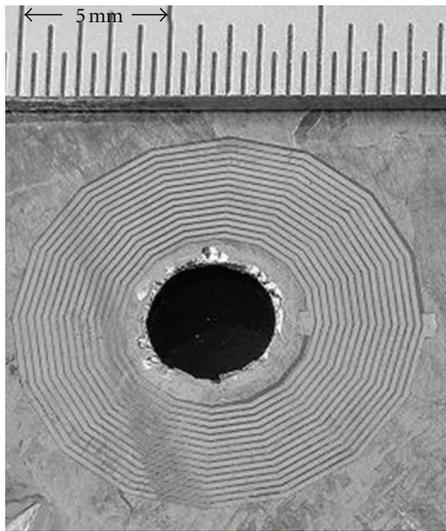


FIGURE 6: Overhead view of triple-layer inductor with air core.

electrical connectively even under abrasion, bending, and shear forces.

Figure 6 shows an overhead view of a MLSI fabricated using our single-level lithography process and with the inner core removed by the abrasion process. Each hash mark in the overhead scale depicts  $500\ \mu\text{m}$  increments. Figure 7 shows a cross-sectional cut of the same inductor in Figure 6, where the sections of light gray matter are the copper coil layers, and the dark gray matter is the SU-8 dielectric layers.

#### 4. Device Characterization and Results

Using our single-level lithography technique, we fabricated three MLSI designs (each with 3 inductor layers in series) with varying trace widths, trace thicknesses, and spacing between inductor layers (see Table 1). Each of the MLSIs were designed to have a nominal inductance value close to  $20\ \mu\text{H}$ . Measurements were conducted for each design to verify the nominal inductance as well as to observe the effects of the geometric variations on performance metrics such as nominal inductance per footprint area, resistance, quality factor, and SRF. Measurements were performed using a HP4194 impedance analyzer and on-chip cascade probes,

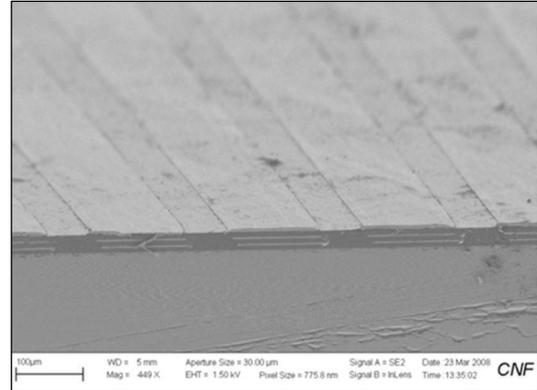


FIGURE 7: SEM cross-sectional image of triple-layer inductor.

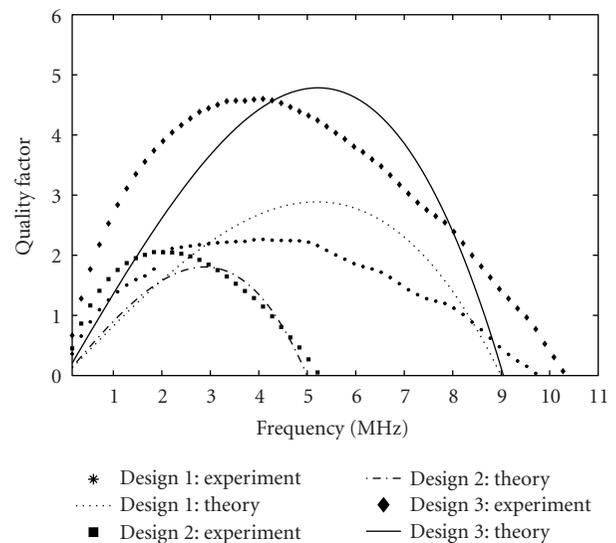


FIGURE 8: MLSI designs with variable geometries.

with averaging of the two-port  $s$ -parameters of the inductors from  $150\ \text{kHz}$  to  $15\ \text{MHz}$  frequency range. Averages were performed using 401 sample points distributed linearly over the frequency range, with 32 trials at each frequency point. Pad capacitance was deembedded by subtracting out the open-circuit structure  $y$ -parameters from the spiral  $y$ -parameters. The calibration procedure we used is the standard approach and is reported widely [14].

We observed general agreement between our lumped parameter model and our experimental results for nearly all performance metric values (see Figure 8 and Table 2). The only exception was the prediction for the maximum  $Q$  of Design 1, which has an unusually flat  $Q$  curve over its measured range. Since all other predictions lie within acceptable experimental results, less than 15%, we assume the model is an accurate first-order approximation up to the first self-resonance frequency. Here we note that Table 2 shows that the lumped parameter model is particularly useful for designing the nominal inductance values of these devices to the desired  $20\ \mu\text{H}$  inductance value. To explain, the nominal

TABLE 1: MLSI geometric variations.

Design	Trace width ( $\mu\text{m}$ )	Trace thickness ( $\mu\text{m}$ )	Trace spacing ( $\mu\text{m}$ )	Trace turns per layer	Inner diameter (mm)	Outer diameter (mm)	Dielectric layer (SU-8 photoresist) ( $\mu\text{m}$ )	Number of stacked inductor layers	MLSI volume ( $\text{mm}^3$ )
1	150	1.1	50	15	6	12.0	30	3	10.54
2	200	1.6	50	15	6	13.5	10	3	4.98
3	150	2.1	50	15	6	12.0	30	3	10.9

TABLE 2: Performance metrics for geometry variations (theory, experiment (*error*)).

Design	Nominal inductance ( $\mu\text{H}$ ) @ 1 MHz	Nominal inductance/footprint area ( $\text{nH}/\text{mm}^2$ ) @ 1 MHz	Resistance ( $\Omega$ ) @ 1 MHz	Q (maximum)	SRF (MHz)
1	26.59, 24.74 (7.5%)	235.1, 218.8 (7.5%)	120.7, 120.8 (0.1%)	3.05, 2.26 (35%)	9.11, 9.87 (7.7%)
2	19.19, 17.25 (11.2%)	134.0, 120.5 (11.2%)	65.6, 66.5 (1.4%)	1.80, 2.05 (12.2%)	5.1, 5.72 (10.8%)
3	26.82, 24.74 (8.5%)	237.2, 218.8 (8.5%)	60.4, 59.1 (2.2%)	4.78, 4.6 (3.9%)	9.12, 10.58 (13.8%)

inductance reported in Table 2 is defined as the linear slope of the reactance and the corresponding frequency,  $f$ , between an initial value in the low frequency range and a final value before the SRF

$$L_{\text{nom}} = \frac{(X_{\text{final}} - X_{\text{initial}})}{2\pi(f_{\text{final}} - f_{\text{initial}})}. \quad (8)$$

Thus, by designing the SRF higher than the intended operating range, we are able to confirm the nominal inductance is achieved for all three designs, using an intermediate frequency evaluation of 1 MHz.

To understand the fabrication implications of the geometric variations, we compare specific performance metrics such as the Q, SRF, and volume. With Design 1 as a baseline, Design 2 increases the trace thickness by 50% for each inductor layer and the trace width by 30%. These changes reduce the resistance by nearly one-half the value compared to Design 1, but result in a longer evaporation time for each inductor layer. To compensate, we reduce the inductor's volume by reducing the thickness of the SU-8 layer, the dielectric layer between the stacked inductors, to one-third its original value, which lowers the electroplating time for each interconnect layer. However, lowering the separation distance between the inductor layers increases the capacitance and reduces the SRF. The result is a design with a slight decrease in fabrication time at one-half the volume, but at the expense of lowered performance values for all values (nominal inductance, nominal inductance per footprint area, Q, and SRF) except the resistance. Focusing on improving the performance metrics with minor expense to the fabrication process, Design 3 uses the same SU-8 (dielectric) layer thickness between inductor layers and the same inductor pattern as Design 1, but increases the trace thickness of each inductor layer to twice the value. The result is a reduction of the resistance by one-half but at the expense of nearly doubling the evaporation time for each inductor layer. While this is a slight fabrication disadvantage, major performance metrics can be achieved such as increasing the Q to twice the value of Design 1, maintaining the nominal inductance, and slightly extending the SRF. Thus, from this small parametric analysis, we are able to compare the variation in performance metrics

and fabrication for changes in the geometry of these high-inductance devices as well as show the accuracy of our lumped parameter model.

When comparing these results to the literature [1, 9], these MLSI stand in an inductance class entirely by themselves. Previous researchers focused on maintaining SRF values close to or within the GHz range to allow for RF applications and resulted in inductance values limited to hundreds of nano-Henries. Our devices demonstrate tens of micro-Henries inductance and maintain Q factors at 2 to 4.6. Through optimization, a balance in designs for appropriate inductance, self-resonance, and Q could be made. Thus this new class of inductors demonstrates useful lumped-parameter modeling and a simplified fabrication process for achieving these performance metrics as well as potentially reduced cost.

## 5. Conclusions

Given the need for high-inductance devices in power converter technology, our main goal in this work was to simplify the CMOS process while increasing the performance of MLSI devices for low frequency range operation. We found that to achieve micro-Henry inductance values, the MLSI design required a balance between a large number of turns per inductor layer and a large number of stacked inductor layers. In addition, to lower the manufacturing difficulty to achieve such a design, a reduction in the number of lithographic steps, as well as an increase in feature size, was critical. Key points include the use of a single-level patterning for the lithography of each inductor layer, and the creation of large interconnects via an electroplating process, which allows for a low required alignment between spiral layers. The large interconnect (dielectric) layers also preserve the large nominal inductance values by reducing the capacitive effect. Finally, a fast abrasion drilling method was implemented to create air cores, which reduces the time required to produce the cavity to mere seconds and represents a significant time savings compared to etching. Together, this simplified approach results in a low cost fabrication method for micro-Henry inductance integrated inductors. In summary, the

single-level lithography fabrication process in conjunction with MLSI designs produced devices exhibiting performance and cost metrics for improving existing power converter technology.

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## References

- [1] A. Zolfaghari, A. Chan, and B. Razavi, "Stacked inductors and transformers in CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 4, pp. 620–628, 2001.
- [2] D. Suh and B. Mheen, "Analysis on the effect of parallel current path on the quality factor of CMOS spiral inductors for 1–10 GHz," *Microelectronic Engineering*, vol. 77, no. 3-4, pp. 292–296, 2005.
- [3] O. H. Murphy, K. G. McCarthy, C. J. P. Delabie, A. C. Murphy, and P. J. Murphy, "Design of multiple-metal stacked inductors incorporating an extended physical model," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 6, pp. 2063–2072, 2005.
- [4] S. Musunuri, P. L. Chapman, J. Zou, and C. Liu, "Design issues for monolithic DC-DC converters," *IEEE Transactions on Power Electronics*, vol. 20, no. 3, pp. 639–649, 2005.
- [5] C. H. Yang, J. H. Chien, B. Y. Wang, P. H. Chen, and D. S. Lee, "A flexible surface wetness sensor using a RFID technique," *Biomedical Microdevices*, vol. 10, no. 1, pp. 47–54, 2008.
- [6] Y. Jia, K. Sun, F. J. Agosto, and M. T. Quiones, "Design and characterization of a passive wireless strain sensor," *Measurement Science and Technology*, vol. 17, no. 11, article no. 002, pp. 2869–2876, 2006.
- [7] C. Leroy, M. B. Pisani, C. Hibert, D. Bouvet, M. Puech, and A. M. Ionescu, "High quality factor copper inductors integrated in deep dry-etched quartz substrates," *Microsystem Technologies*, vol. 13, no. 11-12, pp. 1483–1487, 2007.
- [8] J. M. Lee, I. H. Choi, S. H. Park et al., "Frequency responses of circular spiral inductors for GaAs RF MMIC applications," *Journal of the Korean Physical Society*, vol. 38, no. 2, pp. 123–128, 2001.
- [9] S. J. Pan, L. W. Li, and W. Y. Yin, "Compact equivalent circuit model of two-layer spiral inductors," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 13, no. 2, pp. 148–153, 2003.
- [10] H. A. Wheeler, "Simple inductance formulas for radio coils," *Proceedings of the IRE*, vol. 16, no. 10, pp. 1398–1400, 1928.
- [11] H. M. Greenhouse, "Design of planar rectangular microelectronic inductors," *IEEE Trans Parts Hybrids Packag*, vol. 10, no. 2, pp. 101–109, 1974.
- [12] S. S. Mohan, *Modeling, design, and optimization of on-chip inductors and transformers*, Ph.D. thesis, Stanford University, 1999.
- [13] N. J. Oh and S. G. Lee, "A simple model parameter extraction methodology for an on-chip spiral inductor," *ETRI Journal*, vol. 28, no. 1, pp. 115–118, 2006.
- [14] A. M. Niknejad and R. G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF IC's," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1470–1481, 1998.
- [15] R. A. Johnson, C. E. Chang, P. M. Asbeck, M. E. Wood, G. A. Garcia, and I. Lagnado, "Comparison of microwave inductors fabricated on silicon-on-sapphire and bulk silicon," *IEEE Microwave and Guided Wave Letters*, vol. 6, no. 9, pp. 323–325, 1996.
- [16] M. C. Hsieh, D. K. Jair, and C. S. Lin, "Design and fabrication of the suspended high-Q spiral inductors with X-beams," *Microsystem Technologies*, vol. 14, no. 7, pp. 903–907, 2008.
- [17] I. J. Bahl, "High current handling capacity multilayer inductors for RF and microwave circuits," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 10, no. 2, pp. 139–146, 2000.
- [18] C. Massin, G. Boero, F. Vincent, J. Abenhaim, P. A. Besse, and R. S. Popovic, "High-Q factor RF planar microcoils for micro-scale NMR spectroscopy," *Sensors and Actuators, A*, vol. 97-98, pp. 280–288, 2002.
- [19] J. D. Jackson, *Classical Electrodynamics*, Wiley, New York, NY, USA, 1975.
- [20] Q. Li, "Stacked spiral inductor design and modeling for fully-integrated DC-DC converters," *Applied Mechanics and Materials*, vol. 135-136, pp. 918–923, 2012.



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