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Research Article

Effects of Annealing Time on the Performance of OTFT on Glass with ZrO_2 as Gate Dielectric

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Copper phthalocyanine-based organic thin-film transistors (OTFTs) with zirconium oxide (ZrO_2) as gate dielectric have been fabricated on glass substrates. The gate dielectric is annealed in N_2 at different durations (5, 15, 40, and 60 min) to investigate the effects of annealing time on the electrical properties of the OTFTs. Experimental results show that the longer the annealing time for the OTFT, the better the performance. Among the devices studied, OTFTs with gate dielectric annealed at 350°C in N_2 for 60 min exhibit the best device performance. They have a small threshold voltage of −0.58 V, a low subthreshold slope of 0.8 V/decade, and a low off-state current of 0.73 nA. These characteristics demonstrate that the fabricated device is suitable for low-voltage and low-power operations. When compared with the TFT samples annealed for 5 min, the ones annealed for 60 min have 20% higher mobility and nearly two times smaller the subthreshold slope and off-state current. The extended annealing can effectively reduce the defects in the high-k film and produces a better insulator/organic interface. This results in lower amount of carrier scattering and larger CuPc grains for carrier transport.

1. Introduction

Owing to light weight, mechanical flexibility, and low-cost fabrication, organic thin-film transistors (OTFTs) have a wide range of applications such as sensors, flat-panel displays, and RFID tags [1–3]. The first OTFT based on organic semiconductor polythiophene was reported in 1986 [4]. Heavily doped silicon substrates are generally used for the fabrication of OTFT as they are highly conductive and can act as the gate of the devices. In addition, high-quality gate dielectric SiO_2 can be thermally grown directly on the Si substrate. However, for the next generation of OTFTs and oxide TFTs fabricated on glass or plastic substrates, a metal gate electrode is necessary. By fabricating OTFTs on flexible plastic substrates, there is a potential in the future for producing roll-up displays that can be integrated into a small device such as a pen. There are three major types of dielectric used in OTFTs: inorganic dielectric, polymeric dielectric, and self-assemble layer. For inorganic dielectric materials, silicon dioxide is commonly used as the gate insulator in OTFT. However, this kind of OTFT requires a relatively high voltage (about 100 V) for operation. In order to reduce the operating voltage and hence the power consumption, high-k material is often used as a gate dielectric in OTFTs. Several high-k dielectrics have been employed to fabricate OTFT, for example, HfO_2 [5], Al_2O_3 [6], TiO_2 [7], Ta_2O_5 [8], and $BaTiO_3$ [9]. The performance of organic transistors depends largely on the quality of the gate insulator, the insulator/organic interface, the morphology of the organic thin film, and the charge injection process. It is essential to develop a suitable and high-quality gate insulator with appropriate morphology to achieve a smooth insulator/organic interface. The as-deposited high-k films are usually loosely packed and contain impurities and defects such as oxygen vacancies, oxygen interstitials, and/or oxygen deficiency [10]. These defects and impurities will cause transient charge trapping in the high-k dielectric and leakage current [11]. Various surface passivation methods have been developed in order to achieve high-quality high-k OTFTs, such as annealing in ultraviolet (UV) ozone and nitridation gases, surface

treatment with octadecyltrichlorosilane (OTS), polymethylmethacrylate (PMMA), polyvinyl acetate and ion-beam irradiation, and using stack insulator structure. In this study, one of the most promising high-k dielectric for widespread application, zirconium oxide (ZrO_2), is used as the gate dielectric. ZrO_2 is a stable metal oxide with a high dielectric constant (~15–25) [12] and a large band gap (5.8 eV). It has been reported that ZrO_2 has the lowest leakage current [13]. Moreover, it is a promising material for the fabrication of large-area flexible displays because the ZrO_2 films can be transparent and have good adhesion with plastic substrates [14]. The effects of ZrO_2 annealing treatment time in nitrogen ambient on the electrical properties of CuPc-based organic thin film transistors are investigated. The electrical and physical characteristics of the devices are presented.

2. Experimental Details

Corning 2947 glass substrates ($25 \times 25\,mm^2$) were used in this study as they are mechanical stable, low cost, and compatible with large area applications such as plasma televisions. The substrates were cleaned with a standard regiment of Alconox, acetone, methanol, and deionized water followed by UV ozone treatment for 15 min. The substrates were then loaded into a sputtering chamber with a base pressure of 2.5×10^{-6} Torr. A 150 nm thick Al gate was then deposited at room temperature with a deposition rate of 0.4 Å/sec. A 40 nm thick ZrO_2 was then deposited by sputtering from a zirconium target (99.95% purity) with an RF power of 130 W in a mixed Ar/O_2 ambient (Ar to O_2 ratio = 4 : 1). The chamber pressure during deposition was 5.67 mTorr. The samples then underwent annealing on a hotplate at 350°C in N_2 for different durations (0 min, 5 min, 15 min, 40 min, and 60 min). A layer of 40 nm *p*-type semiconductor, copper phthalocyanine (CuPc) was then deposited by vacuum evaporation through a patterned shadow mask at room temperature. CuPc is a stable and promising *p*-type organic semiconductor with the major charge carriers as holes. It can be easily obtained in large quantity and high purity and hence particularly attractive for low-cost applications in dye processing, chemical sensors, and optical data storage [15, 16]. The source and drain gold pads, 50 nm thick, were then deposited on top of the organic layer by thermal evaporation through a stainless steel mask with a channel length L of 36 μm and a channel width W of 961 μm. The cross-section of the OTFT structure is as shown in Figure 1. The current-voltage (I-V) characteristics were measured by an HP 4155A semiconductor parameter analyzer. All the measurements were taken by a probe station at room temperature in the ambient atmosphere. An atomic force microscopy (Veeco Dimension 3100) in tapping mode was employed to analyze the surface morphology, grain size, and rms roughness of the high-k ZrO_2 and CuPc films.

3. Results and Discussion

Figure 2 shows the output characteristics of the OTFTs with ZrO_2 film annealed for 0 min and 60 min. Typical I_d-V_d curves were obtained when a negative V_g was applied to the devices. At a gate voltage of −3 V and a drain voltage of −4.5 V, the device with ZrO_2 film annealed for 0 min has a drain current of 77 nA, while the one annealed for 60 min has a larger drain current of 107 nA. The operating principle of OTFT is similar to that of traditional *p*-type MOSFET. The current flowed between the source and drain electrodes is modulated by the gate voltage V_g. The carrier mobility of the devices in the saturation regime can be calculated using the following equation:

$$\mu = \frac{2L\left(\partial {I_d}^{1/2}/\partial V_g\right)^2}{WC_{ox}}, \quad (1)$$

where C_{ox} is the unit capacitance of the insulator and μ is the carrier mobility. Figure 3 shows the transfer characteristics of I_d versus V_g at a fixed V_d of −2.5 V for the devices. The subthreshold slope, *SS*, is a very important parameter for OTFTs as it can be used to evaluate the switching characteristics of the OTFTs. *SS* is defined as $\partial V_g/\partial \log_{10}(I_d)$ evaluated at the steepest slope of the plot. From *SS*, the maximum density of the surface states N_{max} at the organic semiconductor/dielectric interface can be estimated as

$$N_{max} = \left[\frac{SS\log(e)}{(kT/q)} - 1\right]\frac{C_o}{q}, \quad (2)$$

where q is the electronic charge, k the Boltzmann constant, and T the temperature in Kelvin.

The important parameters of the devices extracted from the transistor characteristics are summarized in Table 1. It is found that the performances of the OTFTs including mobility, subthreshold slope, surface states density, and off-state current I_{off} improve with annealing duration. This should be due to the fact that the OTFT annealed for longer duration can have a denser ZrO_2 film and a thicker interfacial layer [17, 18] with lower interface-trap density to suppress the leakage associated with high-k materials. In addition, longer annealing can remove more deep traps, oxide charges, and unsaturated bonds in the ZrO_2 dielectric and thus lead to a significant reduction of *S*, N_{max} and I_{off}. It has been reported that dielectric roughness can affect the performance of OTFT [19, 20]. Figure 4 shows the AFM images of the ZrO_2 films with different annealing times. It is found that extending the annealing time from 0 min to 60 min can reduce the gate-dielectric surface roughness (by 9% as measured using AFM). This can contribute to the reduction of trap states, interface defects, and surface scattering on charge carriers leading to higher mobility and smaller subthreshold slope. A smoother insulator surface is also more favorable for the growth of better quality organic film resulting in larger grains

Table 1: Device parameters of the OTFTs.

	0 min	5 min	15 min	40 min	60 min
μ ($\times 10^{-3}$ cm^2/Vs)	1.19	1.21	1.23	1.31	1.43
SS (V/decade)	1.53	1.45	1.11	1.03	0.8
I_{off} (nA)	2.59	1.73	1.39	0.76	0.73
N_{max} ($\times 10^{13}$ cm^{-2})	6.89	6.51	4.92	4.54	3.47

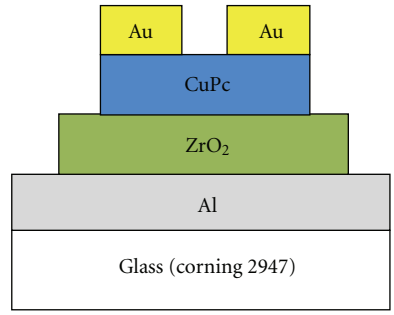

Figure 1: Schematic diagram of a CuPc transistor.

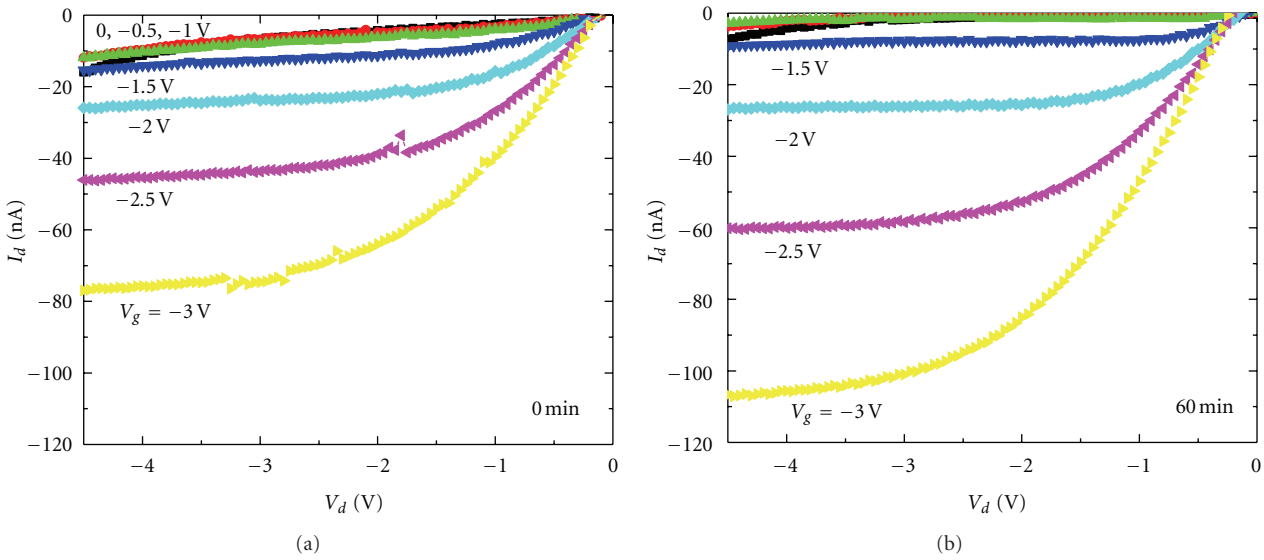

Figure 2: Output characteristic curves of OTFTs with ZrO_2 gate dielectric annealed in N_2 for (a) 0 min and (b) 60 min.

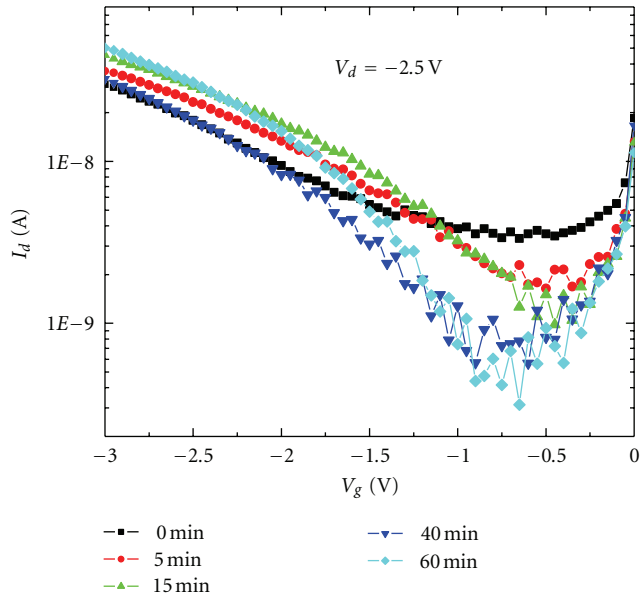

Figure 3: Transfer characteristic curves of OTFTs with ZrO_2 gate dielectric annealed for various durations.

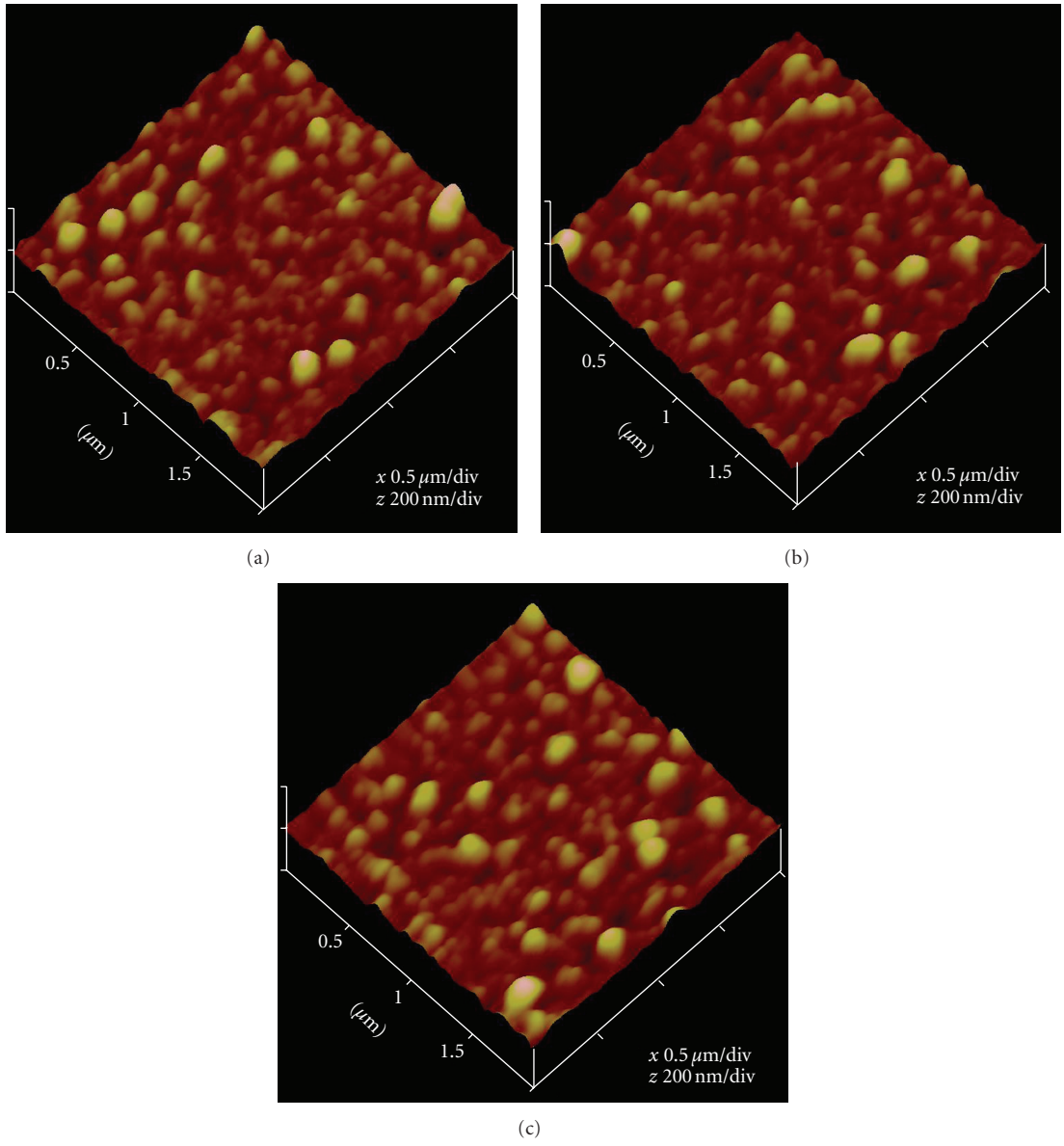

FIGURE 4: AFM images (scan area of 2 μm × 2 μm) of ZrO_2 surface with different annealing treatment times: (a) 0 min, (b) 15 min, and (c) 60 min.

CuPc film grown on the surface of ZrO_2 (~9% larger). This reduces the grain boundaries in the conduction channel for higher mobility of the device [21, 22].

4. Conclusions

In summary, CuPc-based OTFT on glass substrate with high-k ZrO_2 as gate insulator has been fabricated and studied. The effects of annealing time on the electrical properties of the devices are investigated. The study has demonstrated that ZrO_2 is a promising gate dielectric material for obtaining low operating voltage and low power consumption. Experimental results show that the OTFTs with ZrO_2 gate-dielectric annealed for 60 min have 20% higher mobility, 50% smaller subthreshold slope, 72% lower off-state current and 50% smaller maximum density of surface states than the one annealed for 0 min. The possible reasons are that longer annealing time can enhance the densification of the ZrO_2 film, the dielectric properties of the ZrO_2 film, and the quality of the CuPc/ZrO_2 interface, resulting in less carrier scattering and better grain growth.

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