Hindawi Publishing Corporation
Active and Passive Electronic Components
Volume 2013, Article ID 813518, 11 pages
http://dx.doi.org/10.1155/2013/813518

Research Article

Influence of Series Massive Resistance on Capacitance and Conductance Characteristics in Gate-Recessed Nanoscale SOI MOSFETs

Avraham Karsenty[1] and Avraham Chelly[2]

[1] *Faculty of Engineering, Jerusalem College of Technology, Jerusalem 91160, Israel*
[2] *Faculty of Engineering, Bar-Ilan University, Ramat Gan 52900, Israel*

Correspondence should be addressed to A. Karsenty; karsenty@jct.ac.il

Received 12 June 2013; Revised 30 September 2013; Accepted 1 October 2013

Academic Editor: Gerard Ghibaudo

Ultrathin body (UTB) and nanoscale body (NSB) SOI MOSFET devices, having a channel thickness (t_{SI}) ranging from 46 nm (UTB scale) down to 1.6 nm (NSB scale), were fabricated using a selective "gate recessed" process on the same silicon wafer. The gate-to-channel capacitance (C_p) and conductance (G_p) complementary characteristics, measured for NSB devices, were found to be radically different from those measured for UTBS. Consistent C_p and G_p trends are observed by varying the frequency (f), the channel length (L), and the channel thickness (t_{SI}). In this paper, we show that these trends can be analytically modeled by a massive series resistance depending on the gate voltage and on the channel thickness. The effects of leakage conductance and interface trap density are also modeled. This modeling approach may be useful to analyze and/or simulate electrical behavior of nanodevices in which series resistance is of a great concern.

1. Introduction

Planar Fully-Depleted Silicon-On-Insulator (FD-SOI) technology relies on a silicon wafer having an ultrathin layer of crystalline silicon smartly built over a Buried Oxide layer (commonly called BOX). Transistors built into this top silicon layer (which thickness ranges in the decananometer thickness) are called Ultrathin Body (UTB) devices. Such devices have unique and extremely attractive characteristics for coming technology nodes. Since performance needs are increased together with power consumption control, UTB/FD-SOI is also a key technology for addressing high speed and leakage control. In the past several years this technology has gained significant momentum in the mobile communications market space [1, 2]. FD-SOI devices were deeply analyzed across the literature, including the influence of the BOX/Si interface [3]. However, if characterization and modeling of gate-to-channel capacitance (C_p) and conductance (G_p) in FD-SOI devices were recently presented [4], the analyses were focused on devices with gate lengths down to 35 nm and channel thickness down to 8 nm. In parallel, characterization and parameter extraction methods [5, 6], including CV-based method [7], were developed to emphasize dependences between parameters.

In this paper, we report the influence of the silicon channel thickness on the C-V characteristics of Nanoscale Body (NSB) SOI MOSFET devices having a channel thickness less than 5 nm and obtained by a selective gate recessed process [8]. We present a semiquantitative model allowing to justify the influence of the series resistance and to discriminate the influence of the surface states on the C-V characteristics. A preliminary unified electrical model was recently presented in a previous work [9] in which UTB's I-V characteristics in the linear region were compared to those of NSB. The cross-sections of these device structures are, respectively, shown in Figures 1 and 2. The NSB's I-V characteristics were interpreted as the result of an extreme parasitic drain-source series resistance. Since this parameter is of major concern for modern nanoscale devices, its quantitative influence on electrical properties is important to modeling. Usually, drain-source series resistance is aimed to be minimized but design, process, or/and material related issues can generate such

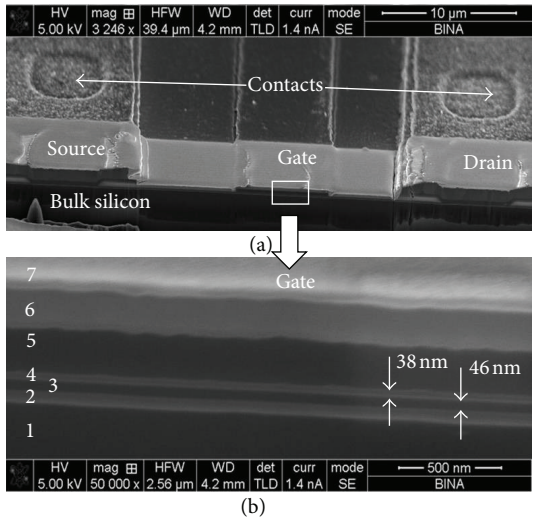


Figure 1: (a) FIB cross-section of the Ultrathin Body Device (UTB) (46 nm channel thickness) showing the device structure including the source, gate, and drain regions. (b) Zoom-in of the layers below the gate region: 1; bulk silicon, 2; buried oxide, 3; silicon channel, 4; Nitride1/Gate Oxide, 5; polysilicon, 6; Silox2/Nitride2, and 7; FIB metal deposition.

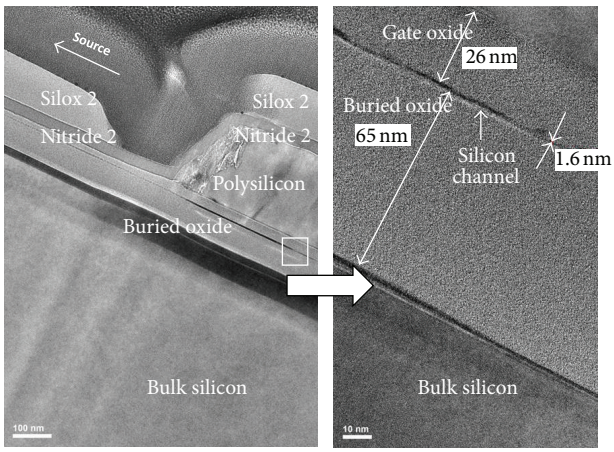


Figure 2: (a) HRTEM image of a nanoscale Body Device (NSB), showing a view of the gate's edge away from the source contact. Since the edge of the source is located 10 μm away from the Gate's edge, the source is not visible here. (b) Zoom in below the Gate region reveals details of the recessed Silicon Channel and confirms the 1.6 nm thickness value. Gate oxide thickness is 26 nm.

parasitic phenomenon that influences the electric properties [10]. In addition to last years' existing knowledge in series resistance, these novel interpretative approach and analytical model can be useful for the prediction of transport phenomena at the nanoscale.

2. Device Processing

2.1. SIMOX Preferred Wafer Processing Technology. Today, SOI wafers are mainly fabricated using the UNIBOND line of SOI wafers and the Smart Cut process technologies, patented by SOITEC Company, allowing excellent thickness uniformity [11]. However, for this research purpose, the former SOITEC technology called Separation-by-IMplanted-Oxygen (SIMOX) was chosen because of the clear advantage of presenting an initial gradient of the SOI thickness across the same wafer. This desirable gradient is conserved during the processing of the nanoscale Body devices (NSB) as shown in Figure 3, in which postthinning spectrophotometry measurements of SOI thicknesses gradient, using the gate recessed process, are presented across a 2″ diameter SIMOX test wafer. Consequently, it is now possible to study the thickness influence on the NSB electrical characteristics with a single process run. The accuracy of the critical channel thickness of 1.6 nm was confirmed by in ex situ HRTEM measurement (Figure 2).

2.2. Structural Characterization. Both representative SOI MOSFET devices having a same ratio W/L of 80/8 (μm) were analyzed using FIB and HRTEM techniques. A FIB cross-section of the Ultrathin Body Device (UTB) (46 nm channel thick) is presented in Figure 1 showing the device structure (Figure 1(a)) and the morphology of the layers forming the gate region (Figure 1(b)). A HRTEM zoom-in of the recessed silicon channel for the nanoscale Body Device (NSB) is presented in Figure 2, confirming the 1.6 nm thickness value.

2.3. Thickness Characterization. The most challenging step was the accurate controlled thinning process of the SOI layer using local oxidation in the sub 10 nm range of thickness, while the source and the drain regions remained in their original thickness. In order to check the capability of accurate thinning, preliminary tests were performed in order to reach thicknesses lower than 10 nm, when characterizing the furnace parameters such as furnace temperature, duration of the oxidation, and growth rate [12].

2.4. Gate Recessed Process. The local oxidation was performed by using a nitride mask layer of 38 nm (nitride 1) grown on a thin oxide layer (PAD OX) of 15 nm. The role of the pad oxide was to serve as an interface between the nitride and the silicon to prevent mechanical stresses. A first etching of the nitride and pad oxide layer at the extremities of the active region allowed their oxidation into a 700 nm thick Field Oxide (FOX). A second etching, performed at the center of the nitride region, allowed exposure of the channel region while the surrounding nitride capped the source and drain areas. Two steps of oxidation were then performed: First, a 75 nm thick sacrificial oxide layer, called Channel Oxide (CHAN OX), was grown in order to significantly decrease the channel's thickness to about 10 nm, before removal. The second phase of the oxidation (25 nm thick), called Gate Oxidation (GOX), was a more accurate step, making possible a final nanoscale thickness of the channel, in the range of 1.6 nm to 6.5 nm, and serving as the Gate Oxide itself. The thickness distribution uniformity and the Si-SiO_2 interface quality [14] serve as important parameters [15, 16]. In order to get reference devices, that is, having an initial silicon

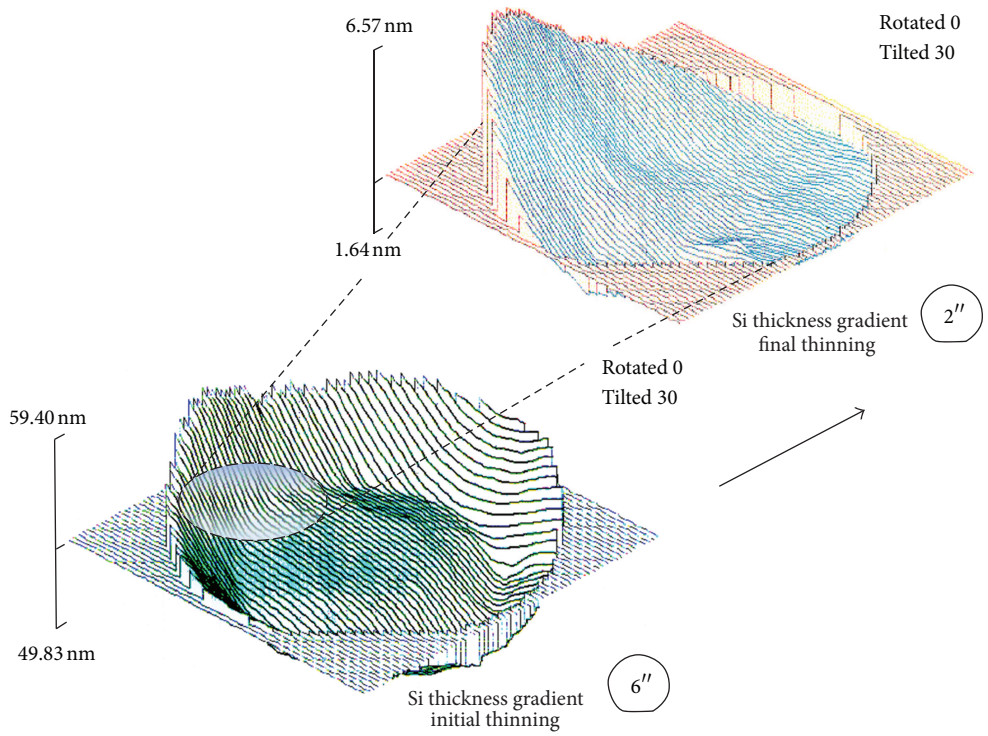


Figure 3: (a) Spectrometer (FT750) map of the initial 6″ diameter SIMOX wafer showing the variation of the SOI thickness. (b) Map of 2″ diameter wafer cut from the edge of the previous wafer showing the variation of the thinned silicon channel.

channel close to 46 nm, the nitride mask was not etched so the gate insulator layer is made of the 38 nm thick nitride layer deposited on the 15 nm PAD OX layer.

2.5. Drain-Source Contacts Fabrication. A polycrystalline silicon layer of 220 nm was deposited over the gate oxide, oxidized, and patterned to form the gate electrode. Before the source/drain/gate phosphorus implant, a thin layer nitride (nitride 2) of 30 nm was deposited in order to prevent further oxidation of the thin silicon layer during the implant's thermal annealing. A Plasma Enhanced Chemical Vapor Deposition (PECVD) oxide (silox 2) of 350 nm thickness was deposited followed by an aluminum metallization step to define the contact areas.

3. Electrical Characterizations and Analysis

3.1. Measured Resistance R_m as a Function of Channel Length (L). The measured resistance R_m is defined as the slope of the I_{DS}-V_{DS} characteristics taken in the linear domain for a given gate voltage V_{GS}. In Figure 4, R_m is plotted as a function of different gate lengths ($L = 4\,\mu$m, $6\,\mu$m, $8\,\mu$m, and $100\,\mu$m) for two NSB's devices (1.6 nm and 2.4 nm channel thick) and for two gate voltages V_{GS} (0 V and 4 V) both above the threshold voltage. For these devices, R_m is decreased by increasing V_{GS}. Surprisingly, R_m is found almost constant with L. In contrast, the UTB reference devices (46 nm channel thick, for $L = 3\,\mu$m, $8\,\mu$m, and $100\,\mu$m) exhibit a linear R_m-L trend and a decreasing trend with V_{GS} as expected from

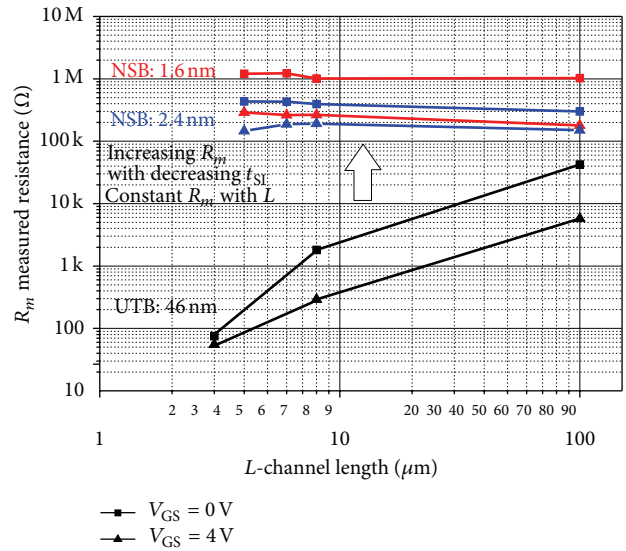


Figure 4: Comparison of the measured resistance R_m for NSBs devices having a channel thickness of 1.6 and 2.4 nm, with UTBs devices (46 nm channel thick), as a function of Channel Length (L) and several V_{GS} positive values.

the classic MOSFET's channel resistance [17, 18]. This result indicates that the contribution of the channel resistance R_{ch} may be negligible for the NSB devices. Assuming R_m is a serial association of R_{ch} with the series source-drain resistance, then R_m can be then approximated by R_{SD}. For NSB's devices, R_{SD} is ranging between 100 kΩ and 1 MΩ and is decreasing

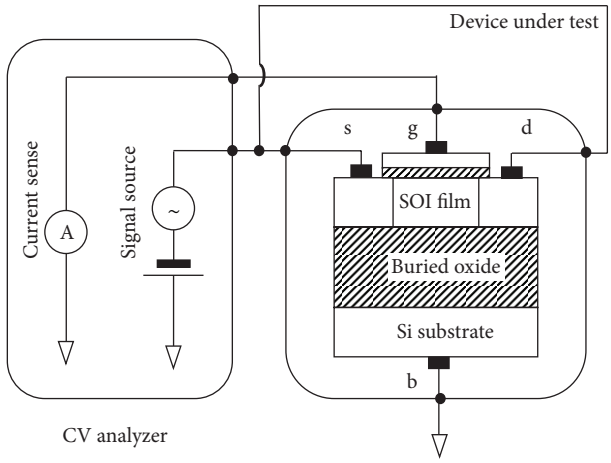


FIGURE 5: Schematic of the experimental setup for the gate to channel capacitance measurement, based on [13] setup.

with the channel thickness as already modeled in a previous work [9].

Although series resistance is usually considered as an association of contributions such as sheet contact resistance, spreading resistance, and other "wire resistance" [19, page 223–225], none of these contributions exhibits the experimental trends observed for NSB's devices here. In our case, the measures resistance should be related to another scattering phenomenon that we propose to investigate using *C-V* measurements.

3.2. Gate to Channel Capacitance and Conductance Characteristics as a Function of Channel Thickness for $L = 100\,\mu m$. The gate to channel capacitance (CGC) of the devices was measured as a function of the Gate voltage (V_{GDS}) using a dual frequency (100 kHz or 1 MHz) CV analyzer (Keithley Model 590). Source and Drain contacts are connected together while the backside (substrate) contact is kept grounded. The DC bias is applied to the drain-source contact and ac-current is collected through the gate contact. The experimental setup is the same as in [13] and shown in Figure 5.

The measured NSB devices, sharing the same W/L (80/100 μm) but different channel thicknesses (1.6 nm and 3.3 nm), are compared to UTB reference device (46 nm channel thick). For all the devices, the measurement was performed at 100 kHz and 1 MHz using the parallel extraction model. The corresponding gate-to-channel capacitance (C_p) and conductance (G_p) versus V_{GDS} are presented for 100 kHz in Figures 6(a) and 6(b), respectively. The corresponding gate-to-channel capacitance (C_p) and conductance (G_p) are presented for 1 MHz in Figures 6(c) and 6(d), respectively.

For the reference UTB device (E15: 46 nm), as seen in Figure 6(a), the negative V_{GDS} domain corresponds to the *accumulation zone* (cut-off regime) where parasitic and gate overlap capacitances are measured to be about 4 pF. Between −1 V and 0 V, the raising of the capacitance is due to the *depletion zone* below the threshold voltage V_T. In the positive V_{GS} domain, the C_p-V_{GDS} characteristic of the UTB's reference device (E15: 46 nm) saturates, which is corresponding to the *inversion zone* [20–22]. The capacitance step amplitude (8 pF), almost independent of the measurement frequency (as seen in Figure 6(c)), is found about 20% lower than the expected total gate oxide capacitance value (9.7 pF) for a WL area of 8×10^{-5} cm^2 (C_{gate} (UTB) = 121 nF/cm^2). This discrepancy may be related to a calibration or a dispersion issue. Another reason we could argue is the additive relative experimental errors we have on the dimensional parameters of the capacitance like W, L, and/or layer thicknesses. Then, by assuming a reasonable 5% error value for each parameter, it may be realistic that our capacitance is estimated with such 20% error. In Figure 6(b), the conductance G_p exhibits a double peak in the depletion zone which is characteristic of the presence of interface states distributed throughout the silicon channel band gap [19, page 337]. By increasing the frequency to 1 MHz, this double peak is enhanced near zero voltage as seen in Figure 6(d).

For the NSB's devices (E15: 1.6 nm and D04: 3.3 nm), as seen in Figure 6(a), the *C-V* characteristic is shifted relatively to the UTB's one, but the capacitance step amplitude is found a bit lower than the former one (6-7 pF). For the D04 device, a hump is observed in the depletion region near zero voltage. This is closely related to the hump of the corresponding *G-V* characteristic shown in Figure 6(b) which is in turn related to the presence of additional interface states as mentioned above. In Figure 6(b), for NSB devices, the conductance amplitude step is about four times those measured for the UTB's one. The NSB's conductance decays through the positive voltage range but with a slower rate than for UTB's.

When increasing the frequency from 100 kHz to 1 MHz, as seen in Figures 6(c) and 6(d), for NSB's, the capacitance step amplitude C_p (~10 pF) and G_p (~1 μS) is increased and decreased by one order of magnitude respectively. Moreover, at 1 MHz, in contrast to 100 kHz, both the capacitance and the conductance are increasing with positive voltage.

3.3. Gate to Channel Capacitance and Conductance Characteristics as a Function of Channel Thickness for $L = 8\,\mu m$. The measured NSB devices, sharing the same W/L (80 μm/8 μm) but different thicknesses (1.6 nm and 3.3 nm), are compared to UTB (46 nm thick). The corresponding gate-to-channel capacitance (C_p) and conductance (G_p) as a function of V_{GDS} are presented for 100 kHz in Figures 7(a) and 7(b), respectively. The corresponding gate-to-channel capacitance (C_p) and conductance (G_p) are presented for 1 MHz in Figures 7(c) and 7(d), respectively.

For the UTB reference device (E15: 46 nm), as seen in Figures 7(a) and 7(c), the capacitance step amplitude (0.4 pF) is almost independent of the measurement frequency. This amplitude is about half the expected total gate oxide capacitance value (0.77 pF), which corresponds to a WL area of 6.4×10^{-6} cm^2 (C_{gate} (UTB) = 121 nF/cm^2). This discrepancy may be related to a lack of accuracy as mentioned above and in particular for the sub-pF range. In contrast to Figure 6(a), at 100 kHz and for positive voltage, the NSB's capacitance characteristics appear strongly degraded comparatively to the UTB's ones and exhibit a maximum value near zero

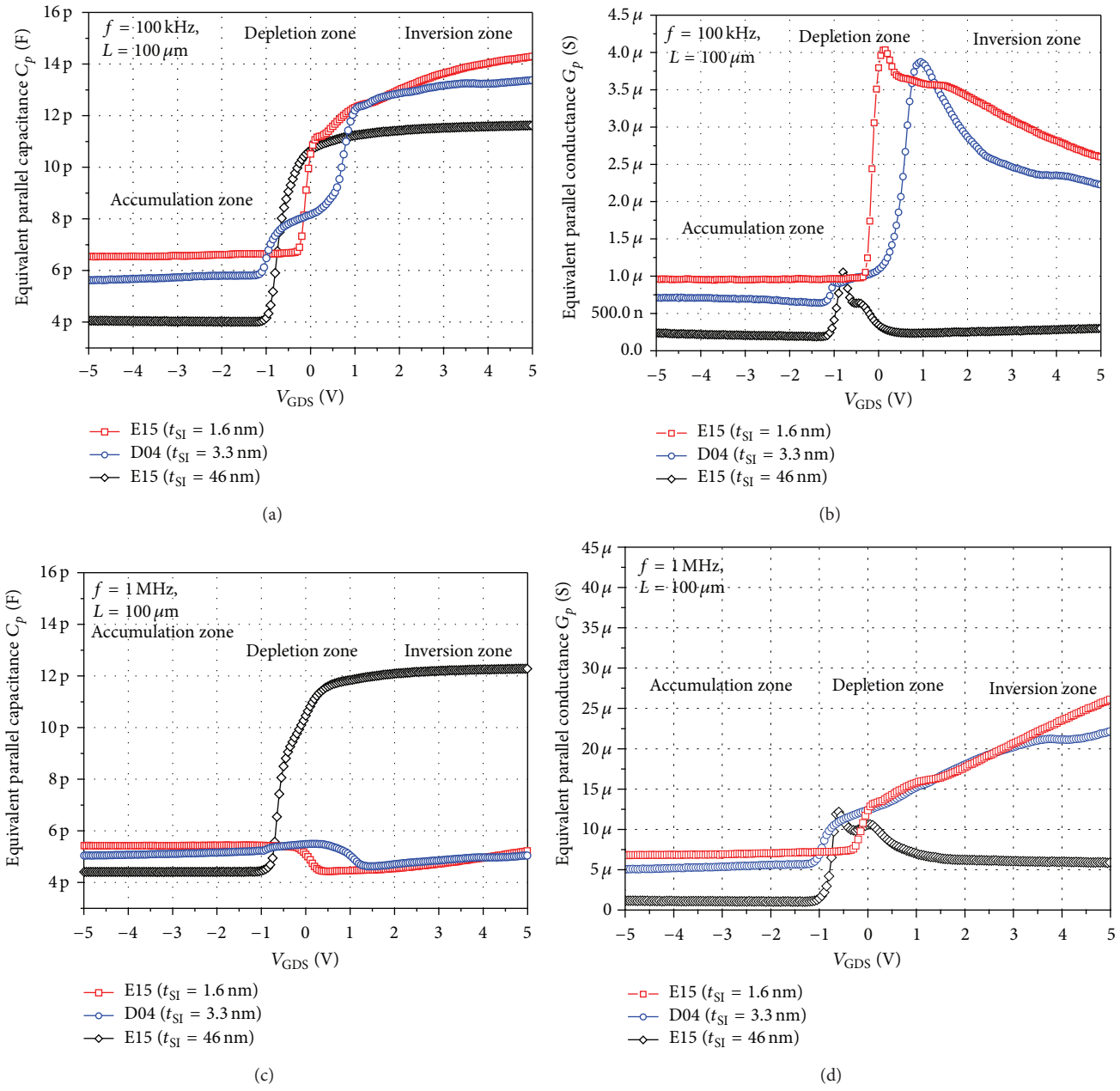


FIGURE 6: Parallel mode C_p-V_{GDS} and G_p-V_{GDS} characteristics for several channel thicknesses t_{SI}. Devices have the same gate area $W \times L$ ($80 \times 100\,\mu m^2 = 8 \times 10^{-5}$ cm^2). (a) Capacitance (C_p) measured at 100 kHz. (b) Conductance (G_p) measured at 100 kHz. (c) Capacitance (C_p) measured at 1 MHz. (d) Conductance (G_p) measured at 1 MHz.

voltage. This degradation is enhanced at higher frequency (1 MHz) and for the lowest channel thicknesses. As seen in Figure 7(b) and unlike Figure 6(b), the conductance for UTB's is found constant with V_{GDS} and insensitive to the frequency change (Figure 7(d)). This indicates a low density of interface states. However, at 1 MHz, a peak of conductance is observed for NSB's around zero voltage. By examining the order of magnitudes of the capacitance step amplitude (~1 pF) and conductance baseline G_p (~1 μS), we noticed that, by increasing the frequency from 100 kHz to 1 MHz, C_p is decreased by a factor of two while G_p is strongly increased by one order of magnitude. Comparatively to Figure 6 (for $L = 100\,\mu m$), the effect of the frequency on C_p and G_p is found weaker.

4. Modeling and Interpretation of the Results

4.1. Modeling the Gate-to-Channel Capacitance and Conductance Characteristics. In order to give a physical interpretation of the measured trends in Figures 6 and 7 and take into account the effect of a series resistance, we propose here to use a classical model of the relationships between the gate-to-channel capacitance and conductance measured in

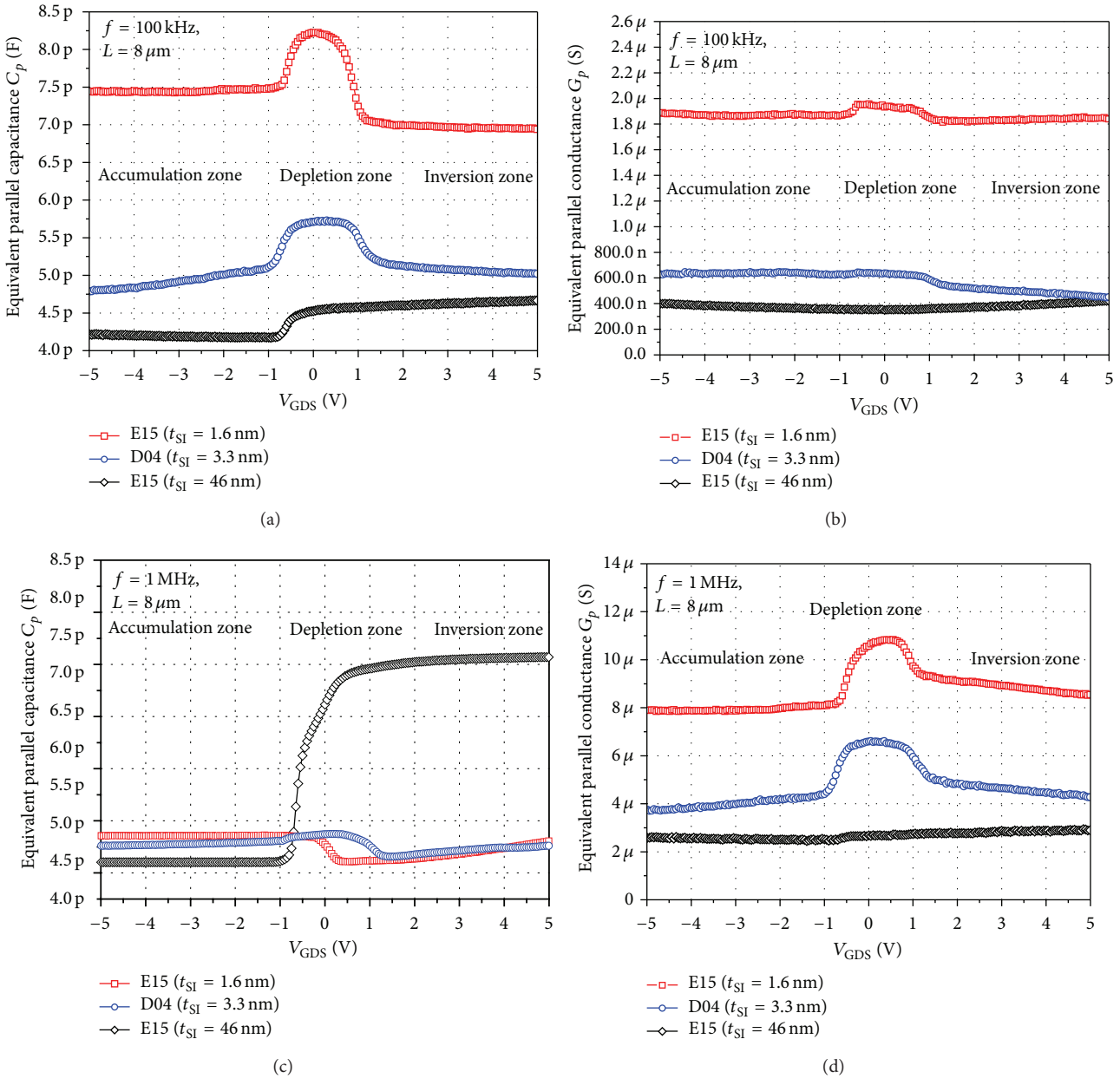


FIGURE 7: Parallel mode C_p-V_{GDS} and G_p-V_{GDS} characteristics for several channel thicknesses t_{SI}. Devices have the same gate area $W \times L$ ($80 \times 8\ \mu m^2 = 6.4 \times 10^{-6}\ cm^2$). (a) Capacitance ($C_p$) measured at 100 kHz. (b) Conductance (G_p) measured at 100 kHz. (c) Capacitance (C_p) measured at 1 MHz. (d) Conductance (G_p) measured at 1 MHz.

parallel mode. In a first analysis, we will omit the influence of interface states which will be considered in the next section. Since a series resistance effect is expected to influence our measurements, as shown above from Figure 8, we have to consider the following electrical equivalent circuits.

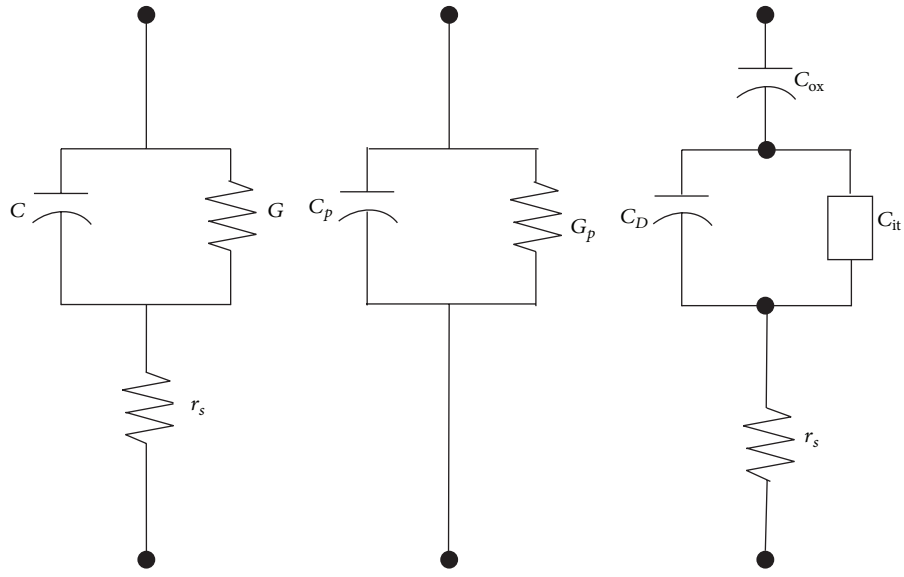
In Figure 8(a), the actual gate to channel capacitance C is coupled with a parallel conductance G, related to a leakage phenomenon, and associated with series resistance r_s.

Assuming a parallel equivalent circuit of two elements (Figure 8(b)), the measured capacitance C_p and conductance G_p are given by the following equations [19, page 89]:

$$C_p = \frac{C}{(1 + r_s G)^2 + (\omega r_s C)^2}, \quad (1)$$

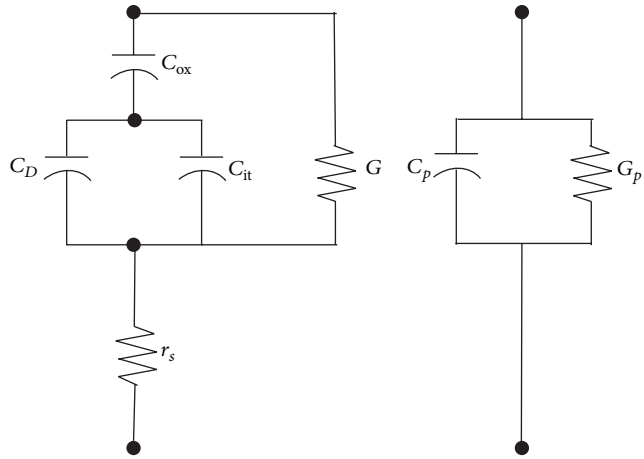
$$G_p = \frac{G(1 + r_s G) + r_s(\omega C)^2}{(1 + r_s G)^2 + (\omega r_s C)^2}, \quad (2)$$

where $\omega = 2\pi f$ (f = 100 kHz or 1 MHz).



(a) Actual circuit (b) Parallel equivalent circuit (c) Interface equivalent circuit

FIGURE 8: C_p and G_p equivalent circuits.



(a) Interface equivalent circuit (b) Parallel equivalent circuit

FIGURE 9: Parallel equivalent circuits modified for the interface trap capacitance C_{it}.

In case of a low leakage conductance and/or low series resistance ($G << 1/r_s$) we get

$$C_p \xrightarrow{r_sG\ll 1} \frac{C}{1+(\omega r_s C)^2} \leq C, \tag{3}$$

$$G_p \xrightarrow{r_sG\ll 1} \frac{G+r_s(\omega C)^2}{1+(\omega r_s C)^2} \geq G. \tag{4}$$

Note that, in this case, for a low ωC factor (low frequency and/or low C value) C_p and G_p tend, respectively, to their actual values C and G.

In case of a low leakage conductance and/or high series resistance ($G \gg 1/r_s$), (1) can be approximated by

$$C_p \xrightarrow{r_sG\gg 1} \frac{C}{{r_s}^2\left[G^2+(\omega C)^2\right]} \ll C, \tag{5}$$

$$G_p \xrightarrow{r_sG\gg 1} \frac{1}{r_s} \gg G. \tag{6}$$

Note that, in this case, for a low ωC factor (low frequency and/or low C value) C_p and G_p tend, respectively, to $C/(r_sG)^2$ and $1/r_s$.

According to the above equations, we can expect the separate influence of each of the three factors (ω, r_s, G) on the measured C_p and G_p values for a given C. Assuming

Table 1: Two-level factorial plan of the modeled values C_p and G_p for three factors: (1) frequency, (2) series resistance (according to NSB or UTB device), and (3) leak conductance. The channel length influence (100 μm versus 8 μm) is linked to the expected (actual) C value. The low and high factor levels are indicated by (−) and (+) sign.

Trial no.	Factor: Frequency f		Series resistance r_s		Leak conductance G		Expected C = 10 pF (L = 100 μm) modeled values		Expected C = 1 pF (L = 8 μm) modeled values	
	100 kHz (−)	1 MHz (+)	100 Ω UTB (−)	100 kΩ NSB (+)	0.5 μS (−)	5 μS (+)	C_p (pF)	G_p (μS)	C_p (pF)	G_p (μS)
(1)	•		•		•		**10.00**	**0.50**	**1.00**	**0.50**
(2)		•	•		•		10.00	0.90	1.00	0.50
(3)	•			•	•		**6.68**	**2.99**	**0.90**	**0.51**
(4)		•		•	•		**0.25**	**9.74**	**0.67**	**2.99**
(5)	•		•			•	10.00	5.00	1.00	5.00
(6)		•	•			•	10.00	5.39	1.00	5.00
(7)	•			•		•	3.78	4.33	0.44	3.35
(8)		•		•		•	0.24	9.64	0.37	4.33
Frequency effect (% average C_p or G_p)							**−20**	**+33**	**−5**	**+16**
Series resistance effect (% average C_p or G_p)							**−57**	**+44**	**−25**	**+22**
Leak conductance effect (% average C_p or G_p)							**−6**	**+23**	**−12**	**−4**
Measured frequency effect at inversion							−−	++	−	++
Measured series resistance effect (UTB/NSB) at inversion							−−	++	−	+

a high and low values set for each factor, we can design a two-level factorial design plan [23] including eight combinations (trials) of the three factors (see Table 1). The expected orders of magnitude (actual value) are C = 10 pF (for L = 100 μm) and C = 1 pF (for L = 8 μm). These values are estimated from the respective oxide gate capacitance of the devices as measured in the inversion zone. The orders of magnitude of the factor series resistance r_s are 100 Ω (low value for UTB device) and 100 kΩ (high value for NSB device) as expected from Figure 4. Considering that we have low leakage devices, as checked from I_g-V_g characteristics (not shown here), the low and high values of G are chosen to 0.5 μS and 5 μS, respectively. These values are matched with those measured for the shorter devices at low frequency and high frequencies in Figures 7(b) and 7(d), respectively. Then, the modeled values of C_p and G_p are presented in Table 1.

In a factorial design plan it is usual to define the *factor effect* (frequency, series resistance, and leak conductance) on the modeled C_p or G_p values as follows:

$$\text{Factor\_Effect\_}C_p = \frac{1}{N_{\text{trials}}} \sum_{i=1}^{N_{\text{trials}}} \text{sign}\,(\text{Factor},i) * C_p\,(i)\,, \tag{7}$$

where

$$\text{sign}\,(\text{Factor}) = \{-\,(\text{if low\_value})\,, +\,(\text{if high\_value})\}\,. \tag{8}$$

In order to highlight the expected trends according to (1), the respective factor effects are calculated and normalized to the average value of C_p and G_p, respectively, and given in percent units as presented in Table 1.

The semiquantitative effects of the frequency and the series resistance on C_p and G_p in the inversion zone (positive gate voltage), as observed from Figures 6 and 7, are indicated for comparison in the last rows of Table 1.

In Figures 6(a) and 6(b) (L = 100 μm, f = 100 kHz), the measured capacitance C_p was weakly decreased while G_p was increased by a factor of four between UTB and NSB devices.

Moreover, we noticed that while increasing the frequency from 100 kHz to 1 MHz the measured capacitance C_p for NSB's was strongly decreased by one order of magnitude while G_p is increased also by one order of magnitude. From Table 1 we can see that this trend is simulated for the modeled values when the r_s factor is at its high value and almost independently of the G (leak) values (rows 3 and 4 and rows 7 and 8). This confirms the detrimental influence of series resistance on the C-V characteristics in particular for thinner channels (NSB) for which the r_s values are increased. Moreover, the increasing of the NSB's conductance with gate voltage at high frequency (Figure 6(b)) can be related to the decreasing of the R_{SD} with gate voltage as seen in Figure 4. From (4), we can see the analytical link between G_p and the $r_s(\omega C)^2$ factor.

For shorter devices having L = 8 μm (and then lower C) Table 1 confirms the weaker influence of series resistance on the C-V characteristics independently of the G (leak), in particular for the thinnest channels (1.6 nm) for which the r_s is enhanced. Indeed, the influence of the frequency on

Table 2: Summarizing table of the interface trap capacitance C_{it} values.

C_{it} (pF) (ratio to expected C value in %)	Interface trap density D_{it} ($cm^{-2}eV^{-1}$)	
	10^{10}	10^{12}
$L = 100\,\mu m$	0.13 (1.3%)	12.80 (130%)
$L = 8\,\mu m$	0.01 (1%)	1.02 (102%)

modeled C_p is lower (see small change between rows 3 and 4 and between rows 3 and 4) than for $L = 100\,\mu m$.

4.2. Influence of the Interface Trap Capacitance on the Gate to Channel Capacitance and Conductance Characteristics. In order to interpret the peak of conductance G_p observed in the depletion zone in Figures 6 and 7, we need to modify the actual circuit to take into account the effect of the interface states [19, page 373–375] as shown in Figure 9. Here we assume the effect of interface trap to a pure capacitance effect though it is usual to associate another parallel resistance r_{it} in order to take into account the time response of the trapping process. However, this approximation is valid for high enough frequencies (above 10 kHz).

Assuming a parallel equivalent circuit of two elements (Figure 9(b)), the measured capacitance C_p and conductance G_p given by (1) can be modified to get the following equations:

$$C_p = \frac{C + C_{it}}{\left(1 + r_s G\right)^2 + \left[\omega r_s \left(C + C_{it}\right)\right]^2}, \tag{9}$$

$$G_p = \frac{G\left(1 + r_s G\right) + r_s\left[\omega\left(C + C_{it}\right)\right]^2}{\left(1 + r_s G\right)^2 + \left[\omega r_s \left(C + C_{it}\right)\right]^2}, \tag{10}$$

where

$$C_{it} = WL\left(qD_{it}\right), \tag{11}$$

and D_{it} is the interface trap densities.

Considering that we have low leakage devices and since G is not an influent factor in this range, G is fixed to 0.5 μS. Then, according to the above equations, we can check the separate influence of each of the three factors (ω, r_s, D_{it}) on the measured C_p and G_p values for a given C. Assuming a high and low values set for each factor, we can design a two-level factorial chart including eight combinations (trials) of the three factors like that in Table 1. The low and high levels of D_{it} are $10^{10}\,cm^{-2}eV^{-1}$ and $10^{12}\,cm^{-2}eV^{-1}$ which are the standard range of detection of interface traps in silicon using the conductance method [19, page 373]. The corresponding parallel capacitance C_{it} values are calculated according to (6) and shown in Table 2. Then, the modeled values of C_p and G_p are presented in Table 3.

We can notice from Table 3 that for UTB ($L = 100\,\mu m$) the introduction of a large D_{it} value should imply an increasing of the capacitance by a factor of two, and an increasing of the conductance by a factor of ten for all measured curves at 100 kHz. By increasing the frequency to 1 MHz, the capacitance should not be increased anymore, but the conductance should be increased by a factor of five. These trends are observed in Figure 6 near zero gate voltage (depletion zone) as a hump in the capacitance step and as an additional conductance peak, respectively.

For NSB ($L = 100\,\mu m$), the introduction a large D_{it} value should imply is a very small increase of the capacitance and of the conductance measured at 100 kHz. By increasing the frequency to 1 MHz, the capacitance should be strongly decreased by a factor of 65 but the conductance should be increased only by a factor of 1.5. These trends are observed in Figure 6 near zero gate voltage (depletion zone) as a degradation of the capacitance step and as an increasing of conductance peak, respectively.

According to Table 3, for UTB ($L = 8\,\mu m$) the introduction of a large D_{it} value should imply an increasing of the capacitance by a factor of two, but the conductance should keep constant. An increasing of the frequency (100 kHz to 1 MHz) should not increase anymore the capacitance or the conductance. These trends are not observed in Figure 7 near zero gate voltage. Indeed the flat conductance characteristics of UTD's show the absence of interface traps for these devices.

For NSB ($L = 8\,\mu m$), the introduction of a large D_{it} value should imply a very small increasing of the capacitance and of the conductance, all measured at 100 kHz. By increasing the frequency to 1 MHz, the capacitance should be strongly decreased by a factor of two; however, the conductance should be increased only by a factor of ten. These trends are observed in Figure 7, near zero gate voltage. However, these effects compete with those from the series resistance as seen in Table 2. In these devices, the influence of the interface traps cannot be clearly resolved from the series resistance effect.

5. Conclusions

Nanoscale (NSB) and Ultrathin (UTB) SOI MOSFET devices were fabricated using a selective gate-recessed thinning process in order to obtain channel thicknesses varying from 1.6 nm to 46 nm. Their respective gate-to-channel capacitance (C_p) and conductance (G_p) characteristics were found to be different and presented different trends as a function of the frequency (f), the channel length (L), and the channel thickness (t_{SI}). In particular the frequency increasing has a positive effect on G_p but a negative on C_p for NSB devices but almost no effect for UTB's. We show that these influences can be analytically and consistently modeled by the presence of a massive series resistance (in the 100 kΩ range) depending on the channel thickness and on the gate voltage. Moreover, in the depletion region of long devices ($L = 100\,\mu m$), near zero gate voltage, the additional peak of C_p and G_p observed in UTB and NSB can be attributed and modeled by an additional capacitance related to the presence of a large interface trap density at low frequency. This effect was not observed for NSB at high frequency nor for shorter devices ($L = 8\,\mu m$). This can be interpreted by the influence of the massive series resistance which screens the effect of the interface traps at high frequency. Finally, the interest of this study for the FD-SOI community is to provide a semiquantitative model that may be useful to interpret the non-classical electrical characteristics of such nanoscale devices.

Table 3: Two-level factorial plan of the modeled values C_p and G_p for three factors: (1) frequency, (2) series resistance (according to NSB or UTB device), and (3) interface trap densities. The channel length influence (100 μm versus 8 μm) is linked to the expected (actual) C value. Leakage conductance G is fixed to its low (actual) value 0.5 μS.

Trial no.	Factor: Frequency f		Trial series resistance r_s		Interface trap density D_{it}		Expected C = 10 pF (L = 100 μm) simulated values		Expected C = 1 pF (L = 8 μm) simulated values	
	100 kHz (−)	1 MHz (+)	100 Ω UTB (−)	100 kΩ NSB (+)	10^{10} $cm^{-2}eV^{-1}$ (−)	10^{12} $cm^{-2}eV^{-1}$ (+)	C_p (pF)	G_p (μS)	C_p (pF)	G_p (μS)
(1)	•		•		•		10.00	0.50	1.01	0.50
(2)		•	•		•		10.00	0.90	1.01	0.50
(3)	•			•	•		6.72	3.03	0.91	0.51
(4)		•		•	•		0.24	9.75	0.67	3.03
(5)	•		•			•	**22.80**	**5.20**	**2.02**	**0.50**
(6)		•	•			•	**22.80**	**25.5**	**2.02**	**0.52**
(7)	•			•		•	**7.23**	**6.67**	**1.81**	**0.61**
(8)		•		•		•	**0.11**	**9.95**	**0.74**	**6.14**
D_{it} = 10^{10} $cm^{-2}eV^{-1}$										
Frequency effect (% average C_p or G_p)							**−17**	**+67**	**−1**	**+32**
Series resistance effect (% average C_p or G_p)							**−50**	**+77**	**−4**	**+2**
Leak conductance effect (% average C_p or G_p)							**−5**	**+195**	**−2**	**+191**
D_{it} = 10^{12} $cm^{-2}eV^{-1}$										
Frequency effect (% average C_p or G_p)							**−14**	**+56**	**−4**	**+75**
Series resistance effect (% average C_p or G_p)							**−92**	**+93**	**−11**	**+47**
Leak conductance effect (% average C_p or G_p)							**−3**	**+46**	**−3**	**+106**
Measured frequency effect at peak (0 V)							−−	++	−	++
Measured series resistance effect (UTB/NSB) at peak (0 V)							−−	++	**0**	+

Conflict of Interests

The authors have no conflict of interest is associated with this paper.

References

[1] T. Skotnick, F. Arnauld, and O. Faynot, "UTBB SOI: a wolf in sheep's clothing," *Future Fab International*, vol. 42, pp. 72–79, 2012.

[2] W. Schwarzenbach, N. Daval, V. Barec et al., "Atomic scale thickness control of SOI wafers for fully depleted applications," *Electronic Clearing Service Transactions*, vol. 53, no. 5, pp. 39–46, 2013.

[3] L. Zafari, J. Jomaah, and G. Ghibaudo, "Impact of BOX/substrate interface on low frequency noise in FD-SOI devices," in *Noise and Fluctuations in Circuits, Devices, and Materials*, vol. 6600 of *Proceedings of SPIE*, Florence, Italy, May 2007.

[4] I. B. Akkez, A. Cros, C. Fenouillet-Beranger et al., "Characterization and modeling of capacitances in FD-SOI devices," *Solid-State Electronics*, vol. 71, pp. 53–57, 2012.

[5] G. Ghibaudo, "Mobility characterization in advanced FD-SOI CMOS devices," in *Semiconductor-on-Insulator Materials for Nanoelectronics Applications*, Engineering Materials Series, pp. 307–322, Springer, Berlin, Germany, 2011.

[6] J. W. Lee, *Caractérisation électrique et modélisation des transistors à effet de champ de faible dimensionnalité [Ph.D. thesis]*, Université de Grenoble, 2006.

[7] I. B. Akkez, A. Cros, C. Fenouillet-Beranger et al., "New parameter extraction method based on split C-V for FDSOI MOSFETs," in *Proceedings of the European Solid-State Device Research Conference (ESSDERC '12)*, pp. 217–220, Bordeaux, France, September 2012.

[8] M. Chan, F. Assaderaghi, S. A. Parke, S. S. Yuen, C. Hu, and P. K. Ko, "Recess channel structure for reducing source/drain series resistance in ultra-thin SOI MOSFET," in *Proceedings of the IEEE International SOI Conference*, pp. 172–173, October 1993.

[9] A. Karsenty and A. Chelly, "Modeling of the channel thickness influence on electrical characteristics and series resistance in gate-recessed nanoscale SOI MOSFETs," *Active and Passive Electronic Components*, vol. 2013, Article ID 801634, 2013.

[10] D. Fleury, A. Cros, G. Bidal, J. Rosa, and G. Ghibaudo, "A new technique to extract the source/drain series resistance of MOSFETs," *IEEE Electron Device Letters*, vol. 30, no. 9, pp. 975–977, 2009.

[11] M. Bruel, B. Aspar, B. Charlet et al., "'Smart cut': a promising new SOI material technology," in *Proceedings of the IEEE International Conference*, pp. 178–179, October 1995.

[12] A. Karsenty, *Study of the electrical and electro-optical phenomena in thin SOI MOS transistors [Ph.D. thesis]*, Hebrew University of Jerusalem, The Fredy & Nadine Hermann Graduate School of Applied Science, Microelectronics & Electro-Optics Divisions, 2003.

[13] D. Flandre and B. Gentinne, "Characterization of SOI MOSFETs by gate capacitance measurements," in *Proceedings of the IEEE International Conference on Microelectronic Test Structures (ICMTS '93)*, vol. 6, pp. 283–287, March 1993.

[14] L. Do Thanh and P. Balk, "Elimination and generation of Si-SiO_2 interface traps by low temperature hydrogen annealing," *Journal of the Electrochemical Society*, vol. 135, no. 7, pp. 1797–1801, 1988.

[15] S. Cristoloveanu and T. Ouisse, *The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface 2*, Plenum Press, New York, NY, USA, 1993, edited by C. R. Helms and B. E. Deal.

[16] V. V. Afanos'ev, A. G. Revesz, and H. L. Hughes, "Confinement phenomena in buried oxides of SIMOX structures as affected by processing," *Journal of the Electrochemical Society*, vol. 143, no. 2, pp. 695–700, 1996.

[17] J. G. J. Chern, P. Chang, R. F. Motta, and N. Godinho, "A new method to determine MOSFET channel length," *IEEE Electron Device Letters*, vol. 1, pp. 170–173, 1980.

[18] C. Hao, B. Cabon-Till, S. Cristoloveanu, and G. Ghibaudo, "Experimental determination of short-channel MOSFET parameters," *Solid State Electronics*, vol. 28, no. 10, pp. 1025–1030, 1985.

[19] D. K. Schroder, *Semiconductor Material and Device Characterization*, chapter 8, John Wiley & Sons, Hoboken, NJ, USA, 2nd edition edition, 1998.

[20] J. Chen, R. Solomon, T. Y. Chan, P. K. Ko, and C. Hu, "A CV technique for measuring thin SOI film thickness," *IEEE Electron Device Letters*, vol. 12, no. 8, pp. 453–455, 1991.

[21] J. Chen, R. Solomon, T. Y. Chan, P. K. Ko, and C. Hu, "Threshold voltage and C-V characteristics of SOI MOSFET's related to Si film thickness variation on SIMOX wafers," *IEEE Transactions on Electron Devices*, vol. 39, no. 10, pp. 2346–2353, 1992.

[22] A. Cros, K. Romanjek, D. Fleury et al., "Unexpected mobility degradation for very short devices: a new challenge for CMOS scaling," in *Proceedings of the International Electron Devices Meeting (IEDM '06)*, pp. 1–4, San Francisco, Calif, USA, December 2006.

[23] G. Box, E. P. Hunter, and W. G. Hunter, *Statistics for Experimenters*, Wiley Series in Probability and Statistics, John Wiley & Sons, Hoboken, NJ, USA, 2nd edition, 2005.