Research Article

A Structural Based Thermal Model Description for Vertical SiC Power MOSFETs under Fault Conditions

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The accurate prediction of the SiC MOSFET withstanding time for single fault events greatly influences the requirements for device protection circuits for these devices in power converter applications, like voltage source inverters or power electronic transformers. For this reason, a thermal model, based on the structural design and the physical dimensions of the chip as well as material properties of 4H-SiC, is proposed. This article gives a general description of the thermal behaviour of vertical SiC MOSFET under various driving and boundary conditions in case of a short-circuit event. The thermal model substitutes destructive tests of a device for an individual set of boundary conditions of an occurring fault event. The validity of the analytically parametrised thermal model is verified by experimental short-circuit tests of state-of-the-art vertical SiC MOSFETs for a set of various boundary conditions. The investigated thermal model can furthermore be used to standardise different gate-oxide degradation values from the literature for means of lifetime prediction of the gate oxide for an individual application under repetitive occurring fault or overload conditions. These manufacturer specific reported values measured with no standardised testing procedures can be translated into a maximum junction temperature, which is repeatedly reached. The thermal model therefore provides a unifying parameter for the gate-oxide lifetime calculation for an individual chip and application.

1. Introduction

Due to their superior material characteristics over silicon, like higher breakdown field strength, increased operating temperature, fast switching speed, and higher thermal conductivity, vertical SiC power MOSFETs are gaining more and more attention for use in voltage source inverters or electronic transformers for highly efficient, high frequency energy conversion in electric vehicles, trains, and more electric aircraft. These devices, packaged as discrete chips in a standard industrial housing or many in parallel in a power module, enable an increase in power density in converters compared to converters equipped with conventional IGBTs based on silicon [1]. Over the last 5 years, the number of manufacturers for vertical SiC MOSFETs has drastically increased. This has resulted in a decline in prices for such devices. For this reason, the use of SiC MOSFETs in industry applications like electric drivetrains or energy conversion applications is steadily increasing.

At the same time, reliability of these devices under harsh operating conditions is still an issue [2–8]. One of its most important issues is the short-circuit (SC) robustness against single or repetitive faults events and overcurrent conditions. Both cannot entirely be eliminated in an electrical system.

For this reason, short-circuit measurements on commercially available SiC MOSFETs [9] have been conducted in order to determine the critical short-circuit energy E_{crit} of these devices. For IGBTs, this is a parameter for the short-circuit capability from which the short-circuit withstanding time for different points of operation can be calculated. This is not the case for today's SiC MOSFETs.

For this reason, a structural based 1D-thermal model of a thermal transmission line that describes the thermal behaviour inside the SiC MOSFET during a short-circuit pulse has been developed. This provides a simplified thermal model for users to determine the short-circuit withstanding time of SiC MOSFETs for a specific application, which can be fed with parameters which are accessible to the user. These are

FIGURE 1: (a) Test circuit configuration; (b) characteristic short-circuit waveform of a 1.7 kV/50 A SiC MOSFET.

current and voltage, measured at the terminal of the devices during a short-circuit event.

2. Short-Circuit Behaviour of SiC MOSFETs

To test the behaviour of a state-of-the-art SiC MOSFET, a setup in buck converter configuration with reduced load inductance is used, referring to Figure 1(a). In order to test the device under hard switching fault (HSF), the diode D1 can be short circuited in order to achieve a minimum short-circuit inductance $L_{SC} = 60$ nH.

Generally, there are three established failure mechanisms for the drain source connection of semiconductor power devices (A–C). These appear at different points of a typical SC waveform (see Figure 1(b)): (A) thermal failure due to high dissipated losses; (B) overvoltage during turn-off; and finally (C) thermal runaway due to high leakage current (see Figure 1(b)). Regarding failure B, if the overvoltage at turn-off exceeds the breakdown voltage, the device eventually goes into avalanche; this results in a combination of high dissipated power loss and high electric field [10]. In this article, all short-circuit tests have been conducted in a

FIGURE 2: Comparing SC behaviour of 1.7 kV/50 A devices SiC MOSFET and IGBT @ $U_{DC} = 1000$ V; $U_{GS} = 20$ V; $U_{GE} = 15$ V; $R_{g,ext} = 6.8$ Ω; $L_{SC} = 60$ nH; and $T_C = 25^\circ$ C.

way, so that the device stays within its safe-operating area. Consequently, this failure mode was not observed.

Regarding the gate source and gate drain connection, which is enclosed by the gate oxide, there is also the effect of the gate-oxide degradation and final breakdown due to high temperature and high electric field stress during a short circuit; this will be addressed in Section 6. Figure 15 illustrates a failure of the gate.

In Figure 1(b), the power loss together with the energy during a HSF is depicted. Even though the SC current could be turned off at $t_{crit} = 4.7$ μs, the chip failed shortly afterwards due to thermal runaway at $t = 6.2$ μs leading to a sharp rise in I_D only limited by L_{SC} , until the chip blows up.

The level of energy dissipated within the chip until failure, by failure mechanism A or C, marks the value of the critical energy E_{crit} . To avoid a failure due to overvoltage (referring to failure mechanism C), $R_{g,ext}$ is set to a higher value and then normally used for hard switching operation. This setup is to provide results of $E_{crit} = f(U_{DC}, T_C, U_{GS})$ to establish a rule to determine the short-circuit withstanding capability of SiC MOSFETs.

3. Experimental Results

The first comparison is shown in Figure 2, where the SC behaviour of a SiC MOSFET with a planar gate structure is compared to that of an IGBT with the same current rating and voltage class according to the datasheet. It can be seen that the MOSFET fails at 6 μs whereas the IGBT can withstand a SC pulse at the same DC-link voltage for almost 20 μs, which is an extraordinary long time and much more than the 10 μs guaranteed by the manufacturer. The second major difference between the two devices is the desaturation limit which is a lot higher for the SiC MOSFET compared to the IGBT.

FIGURE 3: Impact of the temperature at the beginning of a HSF on the waveform of I_D (a) and the critical energy and short-circuit withstanding time (b). Impact of the desaturation level on I_D (c), E_{crit} , and t_{crit} (d). Impact of the DC-link voltage on the waveform of I_D (e) and critical short-circuit energy and time (f).

As a result, the maximum current peak during HSF of the SiC MOSFET reaches about 14 times the rated current of the device I_N , while the IGBT desaturates already at about $8.4 \cdot I_N$. Both higher desaturation current and smaller chip volume lead to a short-circuit withstanding time which is far less than what is common with IGBTs. This is true for any SiC power MOSFET.

There are two reasons why the SC-withstanding time of the IGBT is higher than that of the MOSFET: first, the IGBT limits its SC current to less than 10 times the rated current, reducing the power loss dissipation inside the chip. Secondly, the thermal capacity of the IGBT is higher than that of the MOSFET. The lower current density of the silicon based IGBT results in about twice the chip area for a rated current of $I_N = 50\text{ A}$. It has to be noted that current 2nd-generation SiC MOSFETs are much thicker in the n^- region than what would be required to withstand the electric field in the depletion layer for maximum voltage between drain and source. The same applies to the substrate which is the connection to the drain metallisation. This results in the fact that 2nd-generation SiC MOSFET chips are thicker than

silicon IGBT chips of the same voltage class. 3rd-generation SiC MOSFET chips are already thinner than equivalent IGBT chips. As thin-wafer handling and processing improve further thinning, which is expected for future SiC chip generations, this will decrease the thermal capacity of the chip and might affect short-circuit capability and power module lifetime as will be shown in Section 4.

In Figures 3(a), 3(c), and 3(e), some measurement results of a commercially available SiC MOSFET [9] of the same batch are shown for different operating points under HSF. In Figures 3(b), 3(d), and 3(f), the corresponding critical energies as well as SC-withstanding times until failure are depicted.

As can be seen, the values of E_{crit} of the SiC MOSFET for different operating points are not constant but depend on the conditions of the HSF. The small decrease of E_{crit} because of an increased case temperature suggests that the critical temperature of this device at failure can be found at around $T_{crit} \sim 800^\circ\text{C}$. A bigger effect on E_{crit} can be found when varying U_{GS} . This changes the desaturation level of the channel and by that the level of the SC energy heating up

the chip. On the one hand, a high gate-source voltage of $U_{GS} = 20$ V, E_{crit} , and t_{crit} is a lot lower than at $U_{GS} = 15$ V. On the other hand, a high gate-source voltage, if permitted by the manufacturer, is very desirable for the user because it has a big effect on the electric performance of the device: it increases the switching speed and leads to higher inversion in the channel resulting in a lower channel resistance of the device. At room temperature, the resistance of the channel makes up most of the total $R_{DS,on}$ of a SiC MOSFET with a planar gate structure.

But the biggest effect is the influence of the DC-link voltage (see Figures 3(e) and 3(f)). Changing the DC-link voltage from $U_{DC} = 800$ V to $U_{DC} = 400$ V will more than double the measured critical energy and increase t_{crit} by nearly a factor of 5.

These last two observations are very different to the IGBT where the value of E_{crit} , except for different case temperatures, stays constant [11]. For example, with the IGBT, a 50% reduction of the DC-link voltage leads roughly to a doubling of the short-circuit withstanding time t_{crit} . This SC behaviour of the SiC MOSFET is due to heat conduction effects inside the chip and can be explained by an appropriate equivalent thermal model of the chip, which is described in Section 4.

In the literature, some values of E_{crit} at specific boundary conditions can also be found in [2–8] with devices of the same chip generations and manufacturer. They are in accordance with the displayed results in this article but often there is only one value of E_{crit} at completely different operating points or without concrete testing conditions given. In this case, they are not comparable posing the need for a universal description of SiC MOSFETs in short-circuit mode.

4. Equivalent Thermal Model of the Drain Source Connection

The Cauer network, which describes the thermal behaviour of a power module together with its cooling system, represents the actual physical layers of the system from the heat source of the chip to the ambient area. This network is usually made up by four to five RC elements, namely, $R_{th,1-5}$ and $C_{th,1-5}$; the elements represent the semiconductor chip, the DCB substrate, the baseplate, and the last two elements, items four and five, the cooling system. Regarding the description of the behaviour of an IGBT in short-circuit conditions, only the time constant of the first RC element $\tau_1 = C_{th,1} \cdot R_{th,1}$ is in the time frame in which the short-circuit occurs and therefore can describe the behaviour of the chip.

Because short-circuit withstanding time of the SiC MOSFETs is shorter compared to the IGBT and a SC appears at only a fraction of the volume of the chip, that first RC element τ_1 of the total Cauer network has a big effect on the junction temperature T_j . In order to describe the behaviour of vertical SiC MOSFETs in short-circuit mode, a thermal model is derived from the physical structure of the device which is shown in Figure 4(a). This structure is the result of the manufacturing process of the device which is done by epitaxial growth of the n -layer on a sanded but still rather thick wafer made from 4H-SiC material.

The short-circuit energy is dissipated in the thermal capacitance of the electrically relevant depletion layer of the SiC MOSFET $C_{th,J-SiC}$. This is also called the space charge region, because it takes up the electric field during the blocking state of the device. Due to the high electrical field strength of the 4H-SiC crystal, its volume is a fraction of the volume required in silicon and because 2nd-generation SiC MOSFET chips and state-of-the-art silicon IGBTs of the same voltage class show roughly the same chip thickness, the volume of the space charger region is only a fraction of the total volume of the chip.

The rest of the chip volume is made of a highly doped n^+ substrate, which has no electrical use. It is therefore modelled by a thermal chain of n RC elements representing equally thick layers of the n^+ substrate (see Figure 4(a)). In essence, this leads to a Cauer thermal equivalent network of the chip itself. For reference, three thermal models are parameterised and compared to each other.

Model A. The total chip volume acts as thermal capacitance $C_{th,1}$, which absorbs the SC energy with only one thermal resistance $R_{th,12}$ from the chip to the solder. This standard thermal model describes the behaviour of the IGBT where almost all of the chip volume is consumed by the space charge region [11, 12].

Model B. The short-circuit energy is dissipated in the thermal capacitance of the depletion layer of the SiC MOSFET $C_{th,J-SiC}$. The rest of the chip is modelled by a thermal chain of n RC elements representing equally thick layers of the n^+ substrate (see Figure 4(b)). This is a Cauer thermal equivalent network of the chip itself.

Model C. Only the volume of the depletion layer acts as thermal capacitance $C_{th,J}$ for E_{SC} .

This model is parameterised with data from the material properties of 4H-SiC, like specific thermal capacity, density, and thermal conductivity, as well as the physical dimensions of the SiC MOSFET chip under test. These are the total chip area A_{chip} and thickness d_{chip} , which can be derived from the datasheet of the bare die [9].

One can calculate the thermal resistance between junction and the first layer and thermal capacitance of the junction in (1) using the width of the space charge region (SCR) by assuming a triangular electrical field in the space charge region of the SiC MOSFET. It has to be noted that the real breakdown voltages of today's 2nd- and 3rd-generation SiC MOSFETs of all voltage classes are much higher than the datasheet values of $U_{DS,max}$ [13]. As a result, the value of the real width of the space charger region d_{SCR} is wider than the minimum value which would be theoretically possible.

$$R_{th,J-11} = \frac{1}{\lambda} \cdot \frac{d_{SCR}}{A_{chip}}, \quad (1)$$

$$C_{th,J} = c_{4H-SiC} \cdot \rho_{4H-SiC} \cdot d_{SCR} \cdot A_{chip}.$$

The values of $R_{th,Jn-l-n+1}$ and $C_{th,Jn}$ for the number of n -layers of the substrate can be calculated using (2). For the later

FIGURE 4: (a) Structure of the cross section: a planar vertical SiC MOSFET chip with its 1D-equivalent thermal model. A picture of device destroyed by a hard switching fault (b) and a new device in a TO-247 package (c). The cross section of a TO-247 package (d) with the chip and its connections.

simulation results, a model with a total of ten layers was used, where one layer represents the junction and the other nine represent the substrate (see Figure 4(a)).

$$R_{th,ln-ln+1} = \frac{1}{\lambda} \cdot \frac{d_{chip} - d_{SCR}}{(n-1) \cdot A_{chip}}, \quad (2)$$

$$C_{th,ln} = c_{4H-SiC} \cdot \rho_{4H-SiC} \cdot A_{chip} \cdot \frac{d_{chip} - d_{SCR}}{n-1}.$$

5. Simulation Results

In order to compare the response of the thermal models described, a Heaviside power loss function and real measurement data are used to excite all three models (see Figure 5). From both diagrams in Figure 5, one can see that IGBT model A is delivering the lowest T_j and model C is delivering a value which is unrealistically high. Model B in Figure 5(b) shows that the critical temperature $T_{J,crit}$ at failure is around

800°C, which is in line with numerical calculations on the SC capability of SiC MOSFETs in [3].

Looking at the behaviour of the SiC MOSFET chip during a SC pulse, one can see in Figure 5 in both cases that, within the first 1-2 μs, after the SC event takes place, all short-circuit energy is absorbed by the thermal capacitance of the junction, referring to models B and C which both deliver the same results in that time frame. As the power loss dissipation is continuing, T_j of the chip is rising, which leads to heat conduction into the substrate which can be seen in the difference of both models (B and C) as time progresses.

With Heaviside excitation, model B is responding with $\sqrt{t}$ -temperature profile of the junction temperature. This temperature profile is due to heat conduction effects within the SiC MOSFET chip, from hot to colder layers according to (3), in essence from the junction through the substrate to drain.

$$\dot{Q}_{ln \rightarrow ln+1} = \frac{\lambda \cdot A}{d} (T_n - T_{n+1}). \quad (3)$$

FIGURE 5: Model response to (a) Heaviside power loss excitation and (b) excitation with real $P_{d,SC}(t)$ data at HSF.

For silicon based semiconductors, this $\sqrt{t}$ -temperature profile inside the chip is described in [12] and verified, through measurements of a cooling curve of a standard IGBT using the $R_{g,i}$ -method (see [14] for times from 80 μ s until 500 μ s in [15]). The same behaviour of T_J can be found in SiC devices, as shown with model B. The only difference in 4H-SiC is that, due to heat conductivity with $\lambda_{4H-SiC} = 3.9$ W/cmK which is more than 2.5 times higher than in silicon with $\lambda_{Si} = 1.5$ W/cmK at $T = 300$ K, the short-circuit withstanding time is strongly influenced by the good heat conduction properties of 4H-SiC.

In order to validate the newly proposed and analytically parametrised thermal model B of the SiC MOSFET, measured short-circuit data of different operating points are used to that of the standard thermal model of the IGBT; refer to model A. In Figure 6, one can see the response of models A and B to the measured dissipated power losses $P_{d,SC}(t)$ at $U_{DC} = 800$ V and $U_{DC} = 400$ V from Figure 3(e).

Even though E_{crit} at these two DC-link voltages is very different (see Figure 3(f)), the junction temperatures at failure $T_{J,crit}$ determined with model B are the same. But it has to be noted that, at $U_{DC} = 400$ V, the increase in leakage current leads to a rather soft failure compared to $U_{DC} = 800$ V. This makes it more difficult to determine the exact critical junction temperature.

Two further parameters can be varied. In Figure 7(a), the measured short-circuit data with different case temperatures T_C are applied to both models A and B. In Figure 7(b), the measured short-circuit data with different gate-source voltages are used to excite the models. At all operation points,

FIGURE 6: IGBT and SiC MOSFET model, excited with measured SC data at different DC-link voltages.

it can be seen that model B delivers the same critical junction temperature $T_{J,crit} \approx 760^\circ\text{C}$, while, with standard model A, none of the final destruction temperatures obtained are equal.

FIGURE 7: IGBT and SiC MOSFET model, excited with measured SC data (a) at different case temperatures and (b) at different gate-source voltages.

The standard IGBT model A shows big deviations both in the absolute value of $T_{j,crit}$ and also between the two short-circuit events $\Delta T_{j,crit}$. As a consequence, it is not suitable to describe the behaviour of SiC MOSFETs in short-circuit conditions but it is still valid for IGBTs with trapezoidal electric field.

With heat conduction being a diffusion process within the device, one can obtain T_j by solving the differential equation of the heat conduction or by using a RC network instead. This shows that the 10-layer model of a thermal transmission line is the best fitting 1D model when it comes to explaining the short-circuit capability of SiC MOSFETs.

Based on the thermal model of a transmission line, one can also derive a temperature profile of the different layers inside the chip during a short-circuit event. In Figures 8(a) and 8(b), this has been done for the measured short-circuit power losses at $U_{DC} = 800\text{ V}$ and $U_{DC} = 400\text{ V}$ (refer to Figure 3(e)).

It has been shown in Figure 6 that even though the values of E_{crit} for both short-circuit events are very different, both critical temperatures at failure delivered by model B are the same. Looking at the simulated temperature profile over time of the virtual temperature sensors in each layer, one can see the differences in heat penetration depth into the different layers of the chip. In Figure 8(b), one can see that, under harsh short-circuit conditions, as they appear at high

DC-link voltages, the dissipated power is heating up the junction of the device until the critical chip temperature is reached. However, this happens so fast that little thermal energy is transferred into adjacent layers via heat conduction (see (3)). In this case, the drain connection, where the chip is soldered to the substrate, stays at case temperature and not even half of the total chip volume acts as relevant thermal capacitance to absorb E_{SC} .

In the case of a softer short-circuit event (lower dT_j/dt), referring to Figure 8(b), there is more time to transfer heat to the substrate; one can see that the dissipated heat reaches the bottom layer of the chip and increases the temperature of the drain connection by a few degrees. This can also be seen in the temperature profile inside the chip from source (left) to drain (right) in Figure 9. In this case, more of the chip volume acts as relevant thermal capacitance. But it can also be seen that the thermal capacitance of the solder, or the DCB, below the chip has no influence on the SC robustness for the investigated devices.

In Figure 10, it is shown that the thermal transmission-line model can be parametrised for SiC MOSFETs of different voltage classes and rated current as well as different chip generations and deliver very good results regarding $T_{j,crit}$. Looking at the model response of a 1700 V SiC MOSFET that is turned off after a SC at $t = 4.7\text{ μs}$ but failed at $t = 6.1\text{ μs}$ due to thermal runaway, one can see that the basic

FIGURE 8: Depth of short-circuit energy penetration of a ten-layer thermal transmission-line model (a) at $U_{DC} = 800$ V and (b) $U_{DC} = 400$ V @ $U_{GS} = 20$ V; $T_C = 25^\circ\text{C}$; $L_{SC} = 60$ nH; note that time-base is different.

FIGURE 9: Temperature profile from source to drain inside the SiC MOSFET chip [6] at t_{crit} .

model of a transmission line does not include the leakage current effects. In order to improve the thermal model,

several possible extensions to the 1D model of a thermal chain are discussed.

The first extension is the replication of the power dissipation caused by the leakage current i_R together with the full DC-link voltage, which further heats up the device until it reaches the critical temperature and fails. According to [3], the leakage current consists of three physical parts: thermal generation current, diffusion current, and avalanche multiplication current. These are summarised and together with the DC-link voltage lead to one additional power source parallel to the original one (see Figure 11).

The amount of the leakage current, which leads to a permanent positive temperature gradient over time, as seen in the trend of the temperature of the 1700 V SiC MOSFET in Figure 10, was determined through curve fitting. If this current value would represent homogeneous leakage leading to this trend, i_R would be unreasonably high. Also, the approach shown in [3] to derive i_R from the extrapolation of the current tail of a SiC MOSFET, also seen in Figure 2, turned off out of a short circuit is physically not feasible. As a result, it can be concluded that the leakage current is mainly an inhomogeneous effect which appears locally at the edges or at defects of the chip. This cannot be replicated using a homogenous thermal transmission-line model.

Further refinement of the thermal model could be made by replicating temperature-dependent material parameters of 4H-SiC for each layer, according to Figure 12. With increasing

FIGURE 10: Application of the thermal model for SiC MOSFETs of one technology but different voltage classes 1200 V/20 A (gen. 2) @ $U_{GS} = 20$ V, $U_{DC} = 800$ V, $T_C = 25^\circ\text{C}$, and $L_{SC} = 60$ nH; 900 V/20 A (gen. 3) @ $U_{GS} = 15$ V, $U_{DC} = 400$ V, $T_C = 25^\circ\text{C}$, and $L_{SC} = 60$ nH; 1700 V/50 A (gen. 2) @ $U_{GS} = 20$ V, $U_{DC} = 1000$ V, $T_C = 25^\circ\text{C}$, and $L_{SC} = 60$ nH.

FIGURE 11: Block diagram of the leakage current extension of the thermal model.

temperature, the thermal capacitance increases, improving the robustness in SC mode; however, in the same way also thermal resistance increases. The latter fuels the tendency of thermal runaway of the SiC MOSFET.

It has to be noted that, besides the temperature dependency of λ and c , both parameters are also strongly dependent on the doping concentration of the individual layer. Implementing this for each individual layer is extremely difficult without precise doping values from the chip manufacturers. For this reason, this model extension is not implemented. It can also be considered unnecessary as the basic thermal model of a transmission line with constant R_{th} and C_{th} elements already delivers very good results.

Another model extension may be the simulation of the top-side metallisation of the chip. This means adding another thermal capacitance together with $R_{th, J\text{-metallisation}}$ parallel to the thermal capacitance of the junction, with C_{th} of the $4\text{ }\mu\text{m}$

FIGURE 12: Block diagram of model refinement for temperature dependency of 4H-SiC material parameters.

FIGURE 13: Block diagram of model extension for the top-side metallisation of the chip.

thin aluminium metallisation of the source contact for the bondwires [9] being only one-tenth of $C_{th, J1}$ or $C_{th, J2}$ in case of a 10-layer thermal model of a 1200 V SiC MOSFET together with an additional $R_{th} = 7.6 \cdot R_{th, J-12}$ between 4H-SiC material and the aluminium metallisation, which does not influence the SC robustness of today's SiC MOSFETs. But if measures are taken to improve the short-circuit robustness of SiC MOSFETs by using copper metallisation modelling, the top-side metallisation of the chip becomes increasingly important. In this case, the good match of R_{th} between copper and 4H-SiC would result in larger effective thermal capacitance and as a result longer SC-withstanding time.

A thermal effect of the top-side Al metallisation of the chip on the critical energy is negligible and is not needed to accurately model the SC-measurement results, since the proposed simplified thermal model for the SiC MOSFET already delivers very high accuracy (Figure 13). The recognisable error of critical temperature is below 3%. This is very likely due to the imitation of a 3D device onto a 1D-thermal model of the device as well as process variation within the tested devices. A simple thermal transmission-line model made up of ten RC elements is sufficient enough for power converter designers to describe and predict the short-circuit withstanding time of a SiC MOSFET for various operating points and to calculate the remaining safety margin when fast short-circuit detection is implemented.

In the literature, also other approaches to determine the junction temperature can be found. These are first numerical calculations based on equations which describe semiconductor physics [3, 16]. For the SiC MOSFET in short-circuit mode, this is shown in [3] achieving comparable values for the critical temperature at destruction. The second approach is to use FEM simulations of the device in short-circuit mode. This is proposed in [17] for the IGBT and for SiC MOSFETs in [18, 19]. Simulation with an elaborate inhomogeneous 3D FEM model of the chip in [19] shows the same temperature profile inside the chip in short-circuit mode. The additional benefit of such approach is the value and the location of

FIGURE 14: Comparing SC behaviour of two 1.2 kV/80 mΩ SiC MOSFETs from different manufacturers @ $U_{DC} = 800$ V; $U_{GS} = 18$ V; $R_{g,ext,ManA} = 24$ Ω; $R_{g,ext,ManB} = 6.8$ Ω; $L_{SC} = 60$ nH; $T_C = 25^\circ$ C.

the peak hotspot temperature inside the chip, which is the JFET region of the planar SiC MOSFETs according to [18, 19]. However, it has to be noted that such simulation is lot more time-consuming and requires a lot of parameters of the chip, which are not accessible for the user.

Another third measurement approach in [20] is to use an IR camera to measure the average surface temperature of SiC MOSFETs during SC operation. However, this requires special preparation of the chip or the module and is limited to only a few hundred volts of the DC-link voltage. Even if triggered, this is associated with a high level of uncertainty and is very challenging with short SC times of $t_{crit} < 10$ μs of the SiC MOSFET.

6. Degradation and Failure Mechanism of the Gate Oxide

Between the different manufacturers of SiC MOSFETs, there are substantial differences in short-circuit behaviour even within the same chip generation. This can be seen in Figure 14, where two devices of the same voltage class, current rating I_N , and housing (TO-247) are compared in the same test setup under equal conditions regarding U_{GS} and T_C .

Little differences in I_{peak} can be observed between the two but the major distinction is the different withstanding time of the two regarded chips. At a DC-link voltage of $U_{DC} = 800$ V, one chip fails at drain source after about 5 μs with $E_{crit} = 0.6$ J, resulting in an explosion of the top side of the chip. This event also leads to a lift-off of all bondwires connecting the chip to source while the gate connection is still in place (see Figure 4(b)). This leads to a clear fail-open state of the chip.

The other chip from manufacturer B can withstand a SC pulse of $t_{crit} = 9$ μs and is turned off before the device fails at the gate. So its robustness energy calculated for this event $E_{crit} = 1.16$ J. This is almost twice the value of the first device. After failing at the gate, the device is no longer controllable and remains in an undefined state.

Again, the short-circuit time of both devices under these conditions does not reach $t = 10$ μs which is commonly required for IGBTs. This requires fast short-circuit detection.

A description of the gate-oxide failure mechanism can be seen in three successive diagrams in Figure 15. The first diagram shows an increase of the gate leakage current which flows into the gate right before the device is turned off. This is an indication of degrading gate oxide due to high temperature and high electric field [21–23]. After a number of SC pulses, with the pulse duration of 17 μs from Figure 15(a), the gate oxide is partially breaking through at Figure 15(b) leading to a continuous current flowing into the gate in the on-state; this can be seen in the voltage difference between the driver-output voltage U_{ST} and the gate-source voltage U_{GS} . This marks the number of pulses to failure of the oxide $N_{f,OX}$. Further short-circuit pulses, as seen in Figure 15(c), lead to further degradation of the gate oxide and eventually overloading of the gate driver, which has to provide this increased gate current i_G .

Gate-oxide degradation phenomenon is caused by thermoelectrical stress inside the gate oxide itself. Instead, the value for stable, long-term operation $T_{ox,limit} = f(\vec{E}_{OX}, T_J, d_{OX})$ is implemented by the gate design of the manufacturer. In order to reach a low level of on-state resistance for SiC MOSFETs, the channel resistance must be low. For planar SiC MOSFETs of the 1200 V voltage class, the channel makes up for 2/3 of the total $R_{DS,on}$ at room temperature. In order to have higher carrier mobility in the channel, the gate voltage (electrical field strength) for 2nd-generation SiC MOSFETs was chosen higher than for conventional IGBTs. This high level of inversion together with a thinner oxide layer d_{OX} results in a rather high electric field in the gate oxide $\vec{E}_{OX}$ [21, 22]. This is imposing a lot of stress for the gate oxide especially at high temperatures, like in short-circuit mode. As a result, even if the device is not failing during a short circuit, the gate oxide will be damaged substantially due to a temperature increase in the space charge region right below the gate, thus reducing the number $N_{f,OX}$ of sustainable short circuits. In the literature [4, 21–23], it is shown that the longer the duration of the short-circuit pulse is, the lower the number of accomplishable short circuits and thus the lifetime of the gate oxide will be.

7. Conclusion

It has been shown that the model of the thermal chain is the best fitting one-dimensional model describing the robustness of the drain source connection of SiC MOSFETs in short-circuit mode. This is verified by comparing the thermal calculative results to experimentally achieved results.

A model of a thermal transmission line can easily be parameterised using datasheet values of the SiC MOSFET chips as well as material parameters of the 4H-SiC crystal. Together with operating and circuit parameters of the device, this model can predict the time to failure very accurately, giving designers of high power converters a tool to derive requirements for the short-circuit detection circuit and to

FIGURE 15: (a) Increase of gate-current leakage of a 650 V/20 A SiC MOSFET shortly before turn-off at 18 μ s, (b) partial breakthrough of the gate oxide, and (c) operation with degraded gate oxide @ $U_{DS} = 400$ V; $U_{GS} = 18$ V; $T_C = 25^\circ\text{C}$; $L_{SC} = 60$ nH.

evaluate safety margins for their individual set of operating conditions.

Future generations of SiC MOSFETs with reduced substrate thickness compared to today's SiC MOSFETs do not necessarily have lower short-circuit robustness, since this depends largely on the operating and circuit parameters of these devices, affecting the level of heat conduction through these devices during a fault event.

With today's SiC MOSFETs with a planar gate structure, there are still issues with long-term gate-oxide stability under harsh operating conditions. With future generations of SiC MOSFETs with a trench-gate structure, reliability issues due to the gate oxide might be eliminated, leaving the drain source connection as the single limiting issue for the robustness of these devices. SiC MOSFETs with a trench-gate structure can be designed with a much lower critical electrical field in the gate oxide $\vec{E}_{OX}$ [24], potentially making them less vulnerable to degradation under extreme operating conditions like in short-circuit mode. This still has to be confirmed by further dynamic short-circuit tests which stress the gate oxide of such devices.

Competing Interests

The authors declare that they have no competing interests.

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